به نام خدا

پیش گزارش آزمایش٤

بردیا برائی نژاد(۹۲۱۰۱٦٦۹)

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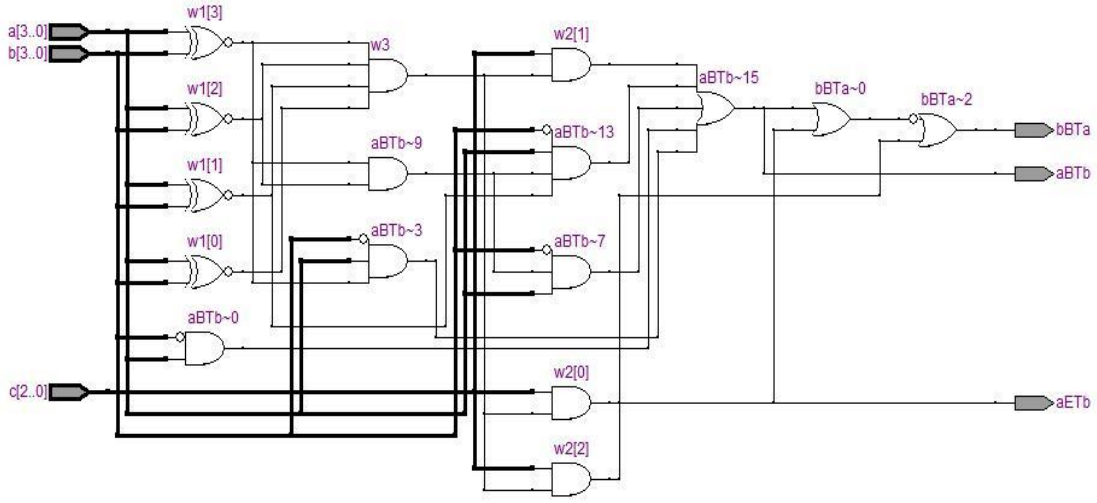
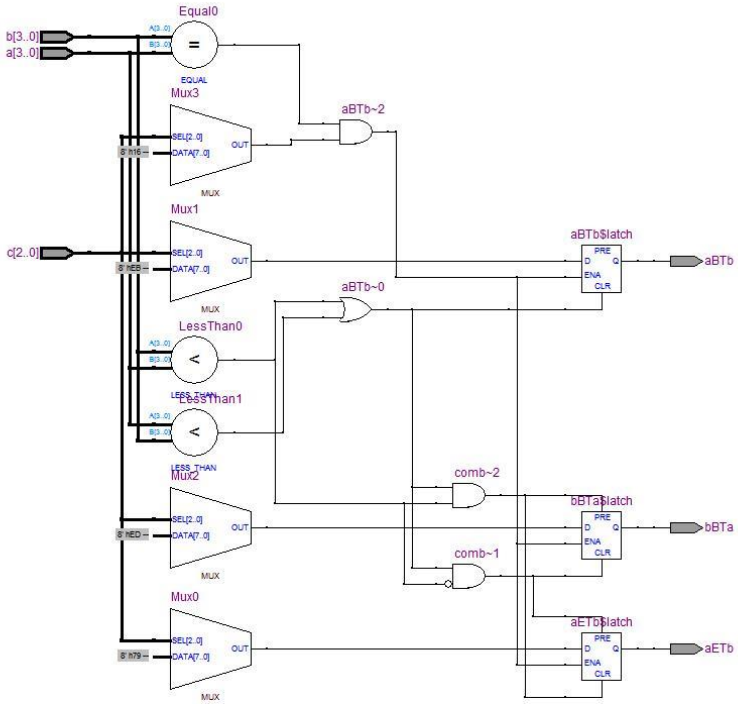
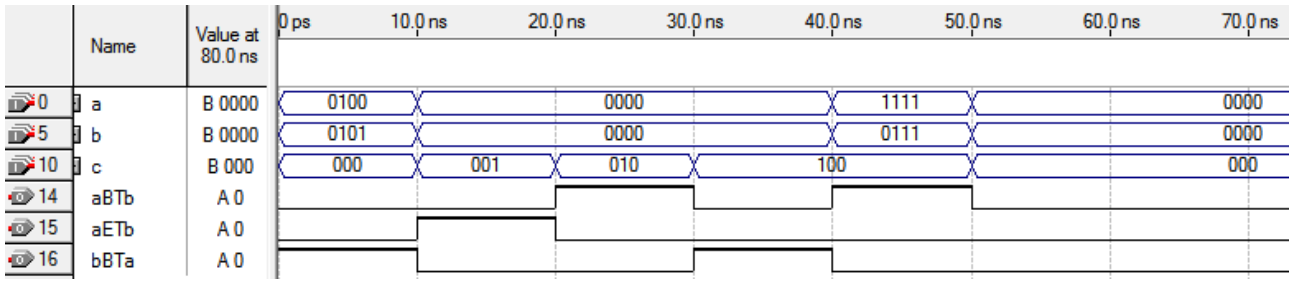
```
module com(a,b,c,aBTb,bBTa,aETb);
    //a , b are 4bit numbers and c is cascade
    //aBTb means a>b,bBTa means b>a,aETb means a=b
    input [3:0] a,b;
    input [2:0] c;
    output aBTb, bBTa, aETb;
    wire [3:0] w1;
    wire [2:0] w2;
    wire w3;
    assign w1[0] = a[0] ~^ b[0],
    w1[1] = a[1] ~^ b[1],
    w1[2] = a[2] ~^ b[2],
    w1[3] = a[3] ~^ b[3],
    w3 = w1[0] & w1[1] & w1[2] & w1[3],
    w2[0] = w3 & c[0],
    w2[1] = w3 & c[1],
    w2[2] = w3 & c[2];
    assign aETb = w2[0],
    aBTb =  (a[3] & ~b[3]) | (w1[3] & a[2] & ~b[2]) | (w1[3] & w1[2] & a[1] & ~b[1]) | (w1[3] & w1[2] & w1[1] & a[3] & ~b[3]) | w2[1],
    bBTa = w2[2] | (~(aETb|aBTb));
endmodule
```



```
module com(a,b,c,aBTb,bBTa,aETb);
    //a , b are 4bit numbers and c is cascade
    //aBTb means a>b,bBTa means b>a,aETb means a=b
    input [3:0] a,b;
    input [2:0] c;
    output reg aBTb, bBTa, aETb;
    always @(*)
    begin
        if (a>b)
            {aETb, aBTb, bBTa} = 3'b010;
        else if (a<b)
            {aETb, aBTb, bBTa} = 3'b001;
        else if (a==b)
        begin
            case(c)
            1: {aETb, aBTb, bBTa} = 4;
            2: {aETb, aBTb, bBTa} = 2;
            4: {aETb, aBTb, bBTa} = 1;
            endcase
        end
    end
endmodule
```





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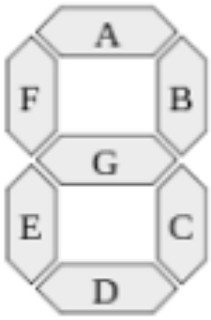
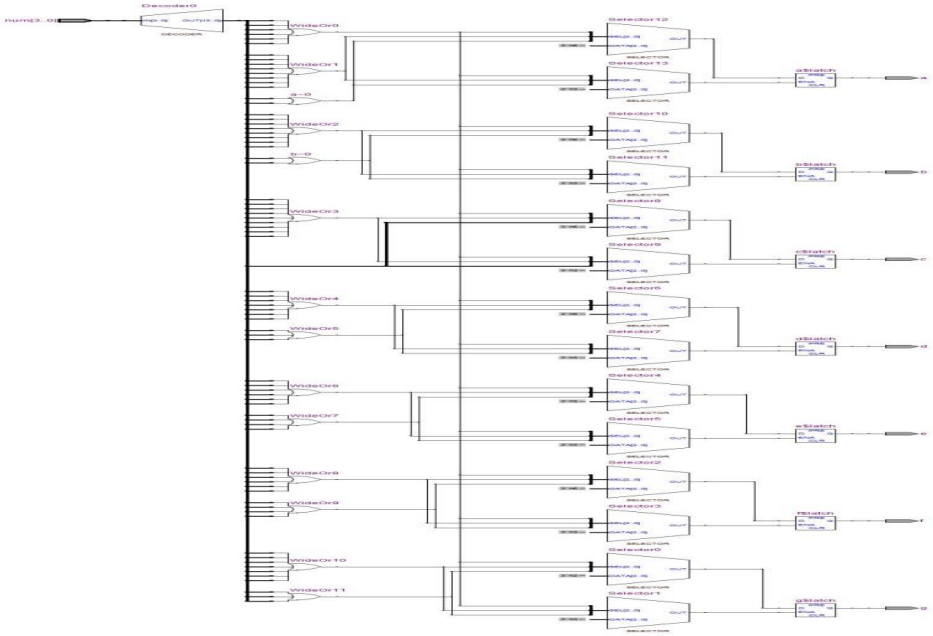
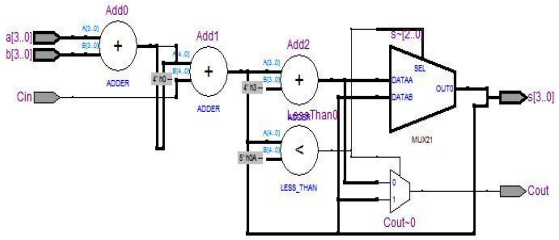



```
module com(num,a,b,c,d,e,f,g);
    //num is the input number
    //a,...,g are names of 7seg LED's
    input [3:0] num;
    output reg a,b,c,d,e,f,g;
    always @(*)
    begin
        case(num)
        0: {a,b,c,d,e,f,g} = 7'b1111110;//g is off
        1: {a,b,c,d,e,f,g} = 7'b0110000;//b,c are on
        2: {a,b,c,d,e,f,g} = 7'b1101101;//c,f are off
        3: {a,b,c,d,e,f,g} = 7'b1111001;//f,e are off
        4: {a,b,c,d,e,f,g} = 7'b0110011;//a,d,e are off
        5: {a,b,c,d,e,f,g} = 7'b1011011;//b,e are off
        6: {a,b,c,d,e,f,g} = 7'b1011111;//b is off
        7: {a,b,c,d,e,f,g} = 7'b1110000;//a,b,c are on
        8: {a,b,c,d,e,f,g} = 7'b1111111;//nothing is off
        9: {a,b,c,d,e,f,g} = 7'b1111011;//just e is off
        endcase
    end
endmodule
```



```
module com(a,b,Cin,Cout,s);
    //a,b are numbers
    //Cin is carry in
    //Cout is carry out
    //s is sum
    input [3:0] a,b;
    input Cin;
    output reg [3:0] s;
    output reg Cout;
    reg [4:0] x;
    always @(*)
    begin
        x = a+b+Cin;
        if (x<10)
            {Cout,s}=x;
        else
            {Cout,s}=x+6;
    end
endmodule
```



۵.آی سی 74LS85 یک مقایسه گر ٤ بیتی است. ورودی های ٤ بیتی به A و B وارد می شوند. (A3 و B3، MSB هستند.) ورودی های Cascading inputs برای استفاده از چند آی سی متوالی هستند تا بتوانیم اعداد بزرگتر از ٤ بیت را مقایسه کنیم.(خروجی های less-significant باید به ورودی های cascade دیگری (more-significant متصل شوند.