به نام خدا

پیش گزارش آزمایش ۸

بردیا برائی نژاد(۹۲۱۰۱۶۶۹)

۱.

```
module jk_ff(clk,aclear,j,k,q,qbar)
    input clk,j,k,aclear;
    output reg q,qbar;
    always@(negedge clk,negedge aclear) begin
        if (!aclear)
        begin
                q<=0;
                qbar<=1;
        end
        else if (j==1 && k==0)
        begin
                q<=1;
                qbar<=0;
        end
        else if (j==0 && k==1)
        begin
                q<=0;
                qbar<=1;
        end
        else if (j==1 && k==1)
        begin
                q<= qbar;
                qbar<=q;
        end
        else
        begin
            q<=q;
            qbar<=qbar;
        end
    end
endmodule
```

٢.

```
module bcd_counter(clk,load,up_down,A,B,a,b,c,d,e,f,g);
    input [3:0]A;
    output reg a,b,c,d,e,f,g;
    output reg [3:0]B;
    always@(posedge clk) begin
        if(!load)
            B<=A;
        else if (up_down)
        begin
            if (B>8)
                B<=4'b0000;
            else
                B<=B+1;
        end
        else if (!up_down)
        begin
            if(B>9||B==0)
                B<=4'b1001;
            else
                B<=B-1;
        end
        case (B)
            0:{a,b,c,d,e,f,g}=7'b1111110;
            1:{a,b,c,d,e,f,g}=7'b0110000;
            2:{a,b,c,d,e,f,g}=7'b1101101;
            3:{a,b,c,d,e,f,g}=7'b1111001;
            4:{a,b,c,d,e,f,g}=7'b0110011;
            5:{a,b,c,d,e,f,g}=7'b1011011;
            6:{a,b,c,d,e,f,g}=7'b1011111;
            7:{a,b,c,d,e,f,g}=7'b1110000;
            8:{a,b,c,d,e,f,g}=7'b1111111;
            9:{a,b,c,d,e,f,g}=7'b1111011;
            default:{a,b,c,d,e,f,g}=7'b0000000;
        endcase
    end
endmodule
```

۳.

```
module shift_reg(clk,A,Q,serialin,sload,asclear,shift);
    input clk,serialin,sload,asclear,shift;
    input [7:0]A;
    output reg [7:0]Q;
    always@(posedge clk, negedge asclear)begin
        if (!asclear)
            q<=0;
        else if (!sload)
            Q<=A;
        else if (!shift)
            Q<=Q;
        else if (shift)
        begin
            Q<=Q<<1;
            Q[0]<=serialin;
        end
    end
endmodule
```

٤.

```
module crossroad_counter(clk,load,A,B,rLED,gLED,a1,b1,c1,d1,e1,f1,g1,a2,b2,c2,d2,e2,f2,g2);
    input clk,load;
    output reg [3:0]A,B;
    output reg a1,b1,c1,d1,e1,f1,g1,a2,b2,c2,d2,e2,f2,g2,rLED,gLED;
    always@(posedge clk,negedge load)begin
        if (!load)
        begin
            rLED<=0;
            gLED<=1;
            A<=1;
            B<=4;
        end
        else if (B)
            B<=B_1;
        else if (A!=0 && B==0)
        begin
            A<=A-1;
            B<=9;
        end
        else if (A==0 && B==0)
        begin
            rLED<=!rLED;
            gLED<=!gLED;
            if (rLED)
            begin
                A<=8;
                B<=4;
            end
            else
            begin
                A<=1;
                B<=4;
            end
        end
    end
    crossroad_BCD_7seg block1(A,a1,b1,c1,d1,e1,f1,g1);
    crossroad_BCD_7seg block2(B,a2,b2,c2,d2,e2,f2,g2);
endmodule
```

```
module crossroad_BCD_7seg(A,a,b,c,d,e,f,g);
    input [3:0]A;
    output reg a,b,c,d,e,f,g;
    always@(A) begin
        case (A)
            0:{a,b,c,d,e,f,g}=7'b1111110;
            1:{a,b,c,d,e,f,g}=7'b0110000;
            2:{a,b,c,d,e,f,g}=7'b1101101;
            3:{a,b,c,d,e,f,g}=7'b1111001;
            4:{a,b,c,d,e,f,g}=7'b0110011;
            5:{a,b,c,d,e,f,g}=7'b1011011;
            6:{a,b,c,d,e,f,g}=7'b1011111;
            7:{a,b,c,d,e,f,g}=7'b1110000;
            8:{a,b,c,d,e,f,g}=7'b1111111;
            9:{a,b,c,d,e,f,g}=7'b1111011;
            default:{a,b,c,d,e,f,g}=7'b0000000;
        endcase
    end
endmodule
```