

به نام خدا

پیش گزارش آزمایش ۸

بردیا برائی نژاد (۹۲۱۰۱۶۶۹)

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```
1  module jk_ff(clk,aclear,j,k,q,qbar)
2      input clk,j,k,aclear;
3      output reg q,qbar;
4      always@(negedge clk,negedge aclear) begin
5          if (!aclear)
6              begin
7                  q<=0;
8                  qbar<=1;
9              end
10         else if (j==1 && k==0)
11             begin
12                 q<=1;
13                 qbar<=0;
14             end
15         else if (j==0 && k==1)
16             begin
17                 q<=0;
18                 qbar<=1;
19             end
20         else if (j==1 && k==1)
21             begin
22                 q<= qbar;
23                 qbar<=q;
24             end
25         else
26             begin
27                 q<=q;
28                 qbar<=qbar;
29             end
30         end
31     endmodule
```

```

1  module bcd_counter(clk,load,up_down,A,B,a,b,c,d,e,f,g);
2      input [3:0]A;
3      output reg a,b,c,d,e,f,g;
4      output reg [3:0]B;
5      always@(posedge clk) begin
6          if(!load)
7              B<=A;
8          else if (up_down)
9              begin
10                 if (B>8)
11                     B<=4'b0000;
12                 else
13                     B<=B+1;
14             end
15          else if (!up_down)
16              begin
17                 if (B>9 || B==0)
18                     B<=4'b1001;
19                 else
20                     B<=B-1;
21             end
22          case (B)
23              0:{a,b,c,d,e,f,g}=7'b1111110;
24              1:{a,b,c,d,e,f,g}=7'b0110000;
25              2:{a,b,c,d,e,f,g}=7'b1101101;
26              3:{a,b,c,d,e,f,g}=7'b1111001;
27              4:{a,b,c,d,e,f,g}=7'b0110011;
28              5:{a,b,c,d,e,f,g}=7'b1011011;
29              6:{a,b,c,d,e,f,g}=7'b1011111;
30              7:{a,b,c,d,e,f,g}=7'b1110000;
31              8:{a,b,c,d,e,f,g}=7'b1111111;
32              9:{a,b,c,d,e,f,g}=7'b1111011;
33              default:{a,b,c,d,e,f,g}=7'b0000000;
34          endcase
35      end
36  endmodule

```

```
1  module shift_reg(clk,A,Q,serialin,sload,asclear,shift);
2      input clk,serialin,sload,asclear,shift;
3      input [7:0]A;
4      output reg [7:0]Q;
5      always@(posedge clk, negedge asclear)begin
6          if (!asclear)
7              q<=0;
8          else if (!sload)
9              Q<=A;
10         else if (!shift)
11             Q<=Q;
12         else if (shift)
13             begin
14                 Q<=Q<<1;
15                 Q[0]<=serialin;
16             end
17         end
18     endmodule
```

```

1  module crossroad_counter(clk,load,A,B,rLED,gLED,a1,b1,c1,d1,e1,f1,g1,a2,b2,c2,d2,e2,f2,g2);
2      input clk,load;
3      output reg [3:0]A,B;
4      output reg a1,b1,c1,d1,e1,f1,g1,a2,b2,c2,d2,e2,f2,g2,rLED,gLED;
5      always@(posedge clk,negedge load)begin
6          if (!load)
7              begin
8                  rLED<=0;
9                  gLED<=1;
10                 A<=1;
11                 B<=4;
12             end
13         else if (B)
14             B<=B_1;
15         else if (A!=0 && B==0)
16             begin
17                 A<=A-1;
18                 B<=9;
19             end
20         else if (A==0 && B==0)
21             begin
22                 rLED<=!rLED;
23                 gLED<=!gLED;
24                 if (rLED)
25                     begin
26                         A<=8;
27                         B<=4;
28                     end
29                 else
30                     begin
31                         A<=1;
32                         B<=4;
33                     end
34             end
35         end
36         crossroad_BCD_7seg block1(A,a1,b1,c1,d1,e1,f1,g1);
37         crossroad_BCD_7seg block2(B,a2,b2,c2,d2,e2,f2,g2);
38     endmodule

```

```

1  module crossroad_BCD_7seg(A,a,b,c,d,e,f,g);
2      input [3:0]A;
3      output reg a,b,c,d,e,f,g;
4      always@(A) begin
5          case (A)
6              0:{a,b,c,d,e,f,g}=7'b1111110;
7              1:{a,b,c,d,e,f,g}=7'b0110000;
8              2:{a,b,c,d,e,f,g}=7'b1101101;
9              3:{a,b,c,d,e,f,g}=7'b1111001;
10             4:{a,b,c,d,e,f,g}=7'b0110011;
11             5:{a,b,c,d,e,f,g}=7'b1011011;
12             6:{a,b,c,d,e,f,g}=7'b1011111;
13             7:{a,b,c,d,e,f,g}=7'b1110000;
14             8:{a,b,c,d,e,f,g}=7'b1111111;
15             9:{a,b,c,d,e,f,g}=7'b1111011;
16             default:{a,b,c,d,e,f,g}=7'b0000000;
17         endcase
18     end
19 endmodule

```