**Logic Course Assignment #6**

1- By using an 8 output Multiplexer IC, and an IC containing 4 two input XOR gates implement the logical function shown below (minterms are purposefully not shown in order, see Hints below):

$F(A,B,C,D,E) = \sum m(16,24,\ 1,9,\ 10,26,\ 3,19,\ 5,13,21,29,\ 14,22,\ 7,31)$

Hints:
a) connect C,D,E signals to the S2, S1, S0 of the Mux, respectively.
b) pay close attention to the shown grouping of minterms!
c) remember that an XOR gate can be used in place of an inverter!

Construct a 5 to 32 decoder using four 3 to 8 decoders with enables, and a 2 to 4 decoder.

2- For the function $F(A,B,C,D) = \sum m(0,1,7,8,9,12,13) + d(5)$ :

a) if it is implemented as SOP,
1) show the possible hazard conditions by drawing the timing diagram
2) show all the hazard free implementations and choose the best one

b) if it is implemented as POS,
1) show the possible hazard conditions by drawing the timing diagram
2) show all the hazard free implementations and choose the best one.

3- Design a **BCD** add/subtract circuit. The circuit inputs are two BCD numbers(A3..A0 and B3..B0), a carry/borrow in (Xi), and a select signal (S: 0=add, 1=subtract) and the outputs are a BCD number (Y3..Y0) and a carry/borrow (Xo). You can use simple gates, full adders, and MUX blocks in your design.

4- Write the Verilog code for the following circuits:

a) A half adder circuit with inputs A, and B, and outputs Sum, and Carry.

b) A 4-bit comparator. The inputs are: A3…A0, and B3…B0,
and the outputs are: X ( = 0 for A>B), Y ( = 0 for A=B), Z ( = 0 for A>B).

c) The BCD add/subtract of Problem 3 above