Verilog HW

Due Date : 93/8/17

1- **(a).** Write a Verilog code to implement $f_1$using the Verilog operators:

$$f_1 = (x_1\&x_3)|(\overline{x_1}\&\overline{x_3})|(x_2\&x_4)|(\overline{x_2}\&\overline{x_4})$$

(b). Write a Verilog code to implement $f_2$using gate instantiation:

$$f_2 = (x_1\&x_2\&\overline{x_3}\&\overline{x_4})|(\overline{x_1}\&\overline{x_2}\&x_3\&x_4)|(x_1\&\overline{x_2}\&\overline{x_3}\&x_4)|(\overline{x_1}\&x_2\&x_3\&\overline{x_4})$$

(c). Perform the functional simulation for f_1 and f_2 in the Quartus and find the relation between f_1 and f_2. Show the output waveforms.

2- (a). Write a Verilog code to implement a 2-to-4 binary decoder using an if-else statement.

(b). Write a Verilog code to implement a 3-to-8 binary decoder using two instances of the 2-to-4 decoder of part (a).

(c). Write a Verilog code to implement a 6-to-64 binary decoder using nine instances of the 3-to-8 decoder of part (b).

(d). Perform the functional simulation for part (b) in the Quartus and verify your design using the waveforms.

3- ***Barrel Shifter*** is an useful core, which can shift the input signal in multiple positions. The following Verilog code is used to describe a 32-bit Barrel Shifter.

```
module BarrelShifter ( input [31:0]
A, output [31:0] B, input [4:0] S);
wire [31:0] A, B;
wire [4:0] S;
        assign B=A<<S;
endmodule
```

Fig. 1. Barrel Shifter.

(a). According to the functionality of the Barrel Shifter, draw the corresponding architecture using some multiplexers.

(b). Write a Verilog code for the above architecture in part (a).