Logic Course Assignment #5 **Due Date: 89/2/6, 7**

1- Describe the behavior of the latch circuit in Fig.1 and write its function table.

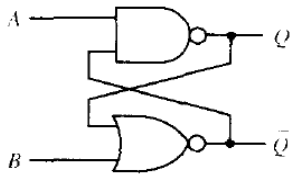

Fig.1

2- Given the JK flip-flop of Fig.2a, complete the timing diagram of Fig.2b by determining the waveform of the output Q.

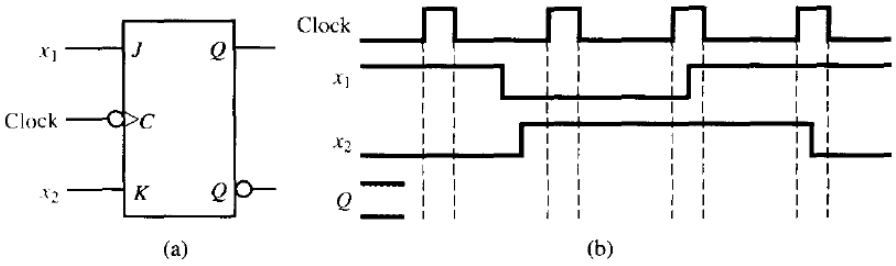

Fig.2

2- The waveforms of Fig.3 are applied to the inputs of an SN7476JK flip-flop. Complete the timing diagram by drawing the waveforms of flip-flop outputs Q and Q'.

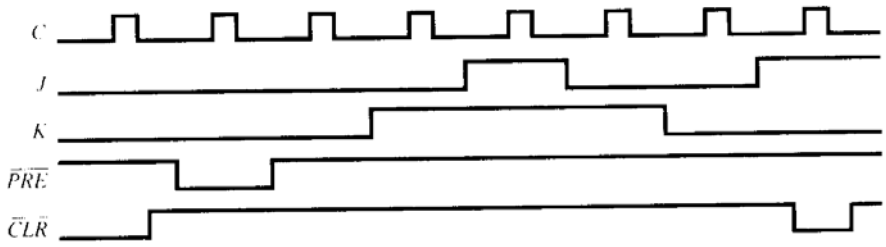

Fig.3

3- The circuit of Fig. 4a contains a D latch, a positive-edge-triggered D flipflop, and a negative-edge-triggered D flip-flop. Complete the timing diagram of Fig.4b by drawing the waveforms of signals y_1, y_2 and y_3.

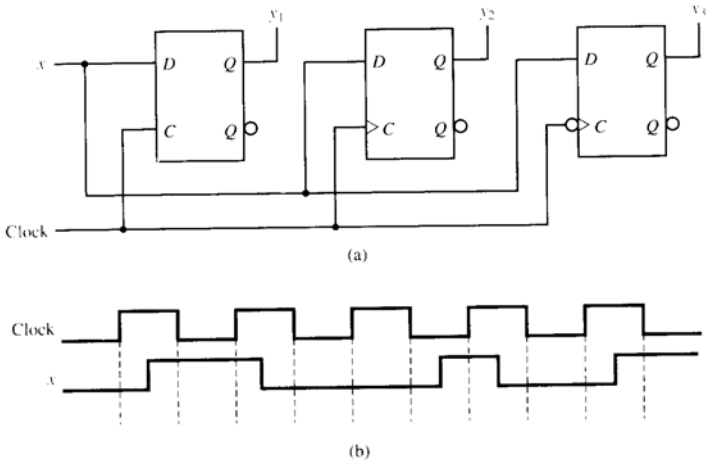

Fig.4

4- With the aid of external logic, show that a D-type flip-flop can be converted to a JK flip-flop.

5- Design a master- slave JK flip flop with asynchronous preset and clear inputs using only NOR gates.

6- Show how to build a D flip flop using a T flip flop and combinational logic.

7- Show how to build a JK flip flop using a T flip flop and combinational logic.

8- Draw the outputs Q and Q' of an SR latch (NOR latch) for the inputs shown in Fig. 5. Assume that the input and output rise and fall times are zero, the propagation delay of a NOR gate is 10ns, and each time division is 10ns.

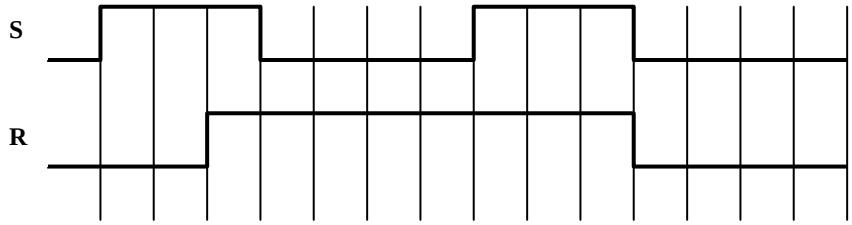

Fig. 5