Iterative Receiver with a Lattice-Reduction-Aided MIMO Detector for IEEE 802.11ax

Yao-Pin Wang[1], Chi-Chih Wen[1], Chen-Chien Kao[1], Chung-Jung Huang[2], Der-Zheng Liu[2], Chia-Hsiang Yang[1]
[1]Graduate Institute of Electronics Engineering, National Taiwan University [2]Realtek Semiconductor Corp.

GLOBECOM 2020 - 2020 IEEE Global Communications Conference | 978-1-7281-8298-8/20/$31.00 ©2020 IEEE | DOI: 10.1109/GLOBECOM42002.2020.9322225

***Abstract*—This paper presents the first 802.11ax compliant iterative detection and decoding (IDD) receiver that supports up to 4×4 1024-QAM MIMO detection in the open literature. Soft-input-soft-output (SISO) MIMO detection is implemented with a lattice reduction aided (LRA) *K*-best searcher and a max-log list demapper. A hardware-efficient IDD receiver is proposed to achieve the required packet-rate (PER) with a feasible latency. The extrinsic information transfer (EXIT) chart is utilized to reduce the number of iterations for IDD. Given the 802.11ax latency constraint, the performance, power, area (PPA) design space is explored to identify the optimal IDD receiver architecture. 50% of IDD inner iterations are reduced with only a 0.05dB loss in PER. The proposed IDD receiver achieves a 1dB improvement in PER with 3.6× smaller area and 3.0× lower power consumption when compared to the best non-IDD receiver.**

I. Introduction

IEEE 802.11 based WLANs are currently the most popular indoor wireless solution. Data rates of WLANs usually exceed those of cellular communications. The IEEE 802.11ax emerges to provide more powerful connectivity [1], [2] for the future development of intelligent infrastructure and the internet of things. As adopted in the modern wireless communication systems, multi-input-multi-output (MIMO) technology and error correction code (ECC) are included in 802.11ax, in which low-density parity-check (LDPC) code is used for high data rate error correction. The MIMO detector and LDPC decoders are the most compute-intensive building blocks in the WLAN baseband receiver.

In IEEE 802.11ax, high-order modulations, such as 1024-QAM, is used to further enhance the data rate. Design of an efficient MIMO detector for 1024-QAM systems with low complexity and high performance is challenging. There have been several detectors for high-dimensional detection. For example, the maximum *a posteriori* (MAP) detector provides the optimal error rate performance in coded-MIMO systems [3]. The maximum-likelihood detector based on differential metric (DM) [4] changes the metric into a differential metric used in the sphere decoder (SD) to generate soft-output efficiently. However, their complexities grow exponentially with the modulation size, which makes them impractical for hardware implementation. Semi-definite relaxation (SDR) [5], [6] is an optimization method for solving detection problems with low complexity and near-ML performance. However, SDR with high order modulation results in poor performance.

In this work, lattice reduction (LR) is utilized to deal with 1024-QAM MIMO detection. Soft-input-soft-output (SISO) LR-aided (LRA) K-best detector with a candidate list max-log soft demapper [7], [8] is used to achieve the near-optimal performance with relatively low complexity. To further improve the error performance, iterative detection and decoding (IDD) is carried out. This work proposes a rule of thumb to reduce the number of iterations by leveraging the extrinsic information transfer (EXIT) chart. A feasible MIMO detector architecture is presented and used to explore the performance, power, area (PPA) design space of the 802.11ax compliant IDD receiver. Based on a reference design of an LDPC decoder, the levels of parallelism of MIMO detectors and LDPC decoders are analysed based on the 802.11ax specifications.

The paper is organized as follows. Section II provides an overview of the LRA max-log list demapper for MIMO detection. Characteristics of the IDD receiver and the EXIT chart are presented in Section III. Hardware architecture of a 1024-QAM MIMO detector is described in Section IV. Section V shows the analysis results for parallel processing of an 802.11ax compliant IDD receiver in the PPA design space. Finally, Section VI concludes the paper.

II. Lattice-Reduction-Aided List Demapper

A MIMO-OFDM (orthogonal frequency-division multiplexing, OFDM) system with N_T transmit antennas and N_R receive antennas, as specified in 802.11ax, is considered in this work. It can be modelled as

$$\mathbf{y} = \mathbf{H}\mathbf{s} + \mathbf{n}, \tag{1}$$

where $\mathbf{s} \in \Omega^{N_T}$ is the transmit vectors mapped onto the constellation set Ω. $\mathbf{y} \in \mathbb{C}^{N_R}$ is a received symbol vector. $\mathbf{H}$ is a $N_R \times N_T$ complex-valued WLAN channel matrix and $\mathbf{n}$ is the vector of additive white Gaussian noise (AWGN) with power σ_n^2. Modulation coding scheme (MCS) from MCS-0 to MCS-11 and channel models B, D, and E of WLANs are considered for simulations. See [2] for the details of the 802.11ax specifications.

A. Lattice-Reduction

Lattice reduction (LR) is a preprocessing technique to improve the MIMO detection performance. A MIMO system with lattice reduction can be expressed as

$$\bar{\mathbf{y}} = \mathbf{H}\bar{\mathbf{s}} + \mathbf{n} = \mathbf{H}\mathbf{T}\mathbf{T}^{-1}\bar{\mathbf{s}} + \mathbf{n} = \tilde{\mathbf{H}}\tilde{\mathbf{s}} + \mathbf{n} = \tilde{\mathbf{Q}}\mathbf{R}\tilde{\mathbf{s}} + \mathbf{n}, \tag{2}$$

where $\bar{\mathbf{y}}$ is the received signal, $\tilde{\mathbf{H}} = \mathbf{H}\mathbf{T}$ is the lattice-reduced channel matrix, and $\mathbf{T}$ is a uni-modular matrix. QR

978-1-7281-8298-8/20/$31.00 ©2020 IEEE

decomposition is applied to $\tilde{\mathbf{H}}$, resulting in an unitary matrix $\tilde{\mathbf{Q}}$ and an upper triangular matrix $\mathbf{R}$. $\tilde{\mathbf{s}} = \mathbf{T}^{-1}\bar{\mathbf{s}}$ is symbol vector in the lattice reduction domain. The MIMO detection is performed on $\tilde{\mathbf{z}}$ by multiplying $\bar{\mathbf{y}}$ with $\tilde{\mathbf{Q}}^{\mathbf{H}}$, given by

$$\tilde{\mathbf{z}} = \tilde{\mathbf{Q}}^{\mathbf{H}}\bar{\mathbf{y}} = \mathbf{R}\tilde{\mathbf{s}} + \tilde{\mathbf{n}}. \tag{3}$$

The Lenstra-Lenstra-Lovász (LLL) algorithm has been known as one of the effective LR algorithms to find reduced basis in a polynomial time [9]. The enhanced-Constant-Throughput LLL (ECTLLL) algorithm with Siegel condition [10] improves the throughput with predictable processing time. ECTLLL deals with size reduction and LLL reduction iteratively. Size reduction can be calculated by

$$\mu = \lceil \tilde{\mathbf{R}}(i-1,i)/\tilde{\mathbf{R}}(i-1,i-1) \rfloor. \tag{4}$$

If the Siegel condition is violated, LLL reduction is then conducted by swapping two columns of $\tilde{\mathbf{R}}$:

$$\tilde{\mathbf{R}}(1:i,i) \leftarrow \tilde{\mathbf{R}}(1:i,i) - \mu\tilde{\mathbf{R}}(1:i,i-1). \tag{5}$$

B. Lattice-Reduction-Aided-K-Best Search

The LR-aided K-best MIMO detection algorithm presented in [11] is adopted in this work. On-demand expansion is applied to reduce the number of the child nodes needed to be expand and sorted. The best child nodes of each parent node are enumerated first without enumerating all the other nodes. The best child node of the k-th parent node in the i-th layer is given by

$$sc_i^{k,1} = \frac{\tilde{z}_i - \sum_{m=i+1}^{N_T} \tilde{R}_{i,m}\tilde{s}_m^k}{\tilde{R}_{i,i}}, \tag{6}$$

where $\tilde{R}_{i,m}$ is the (i,m)-th element of $\tilde{\mathbf{R}}$. After the best child nodes of each parent node are sorted, the one with the smallest partial distance (PD) is selected as the candidate in this layer. PD is calculated as

$$PD_i = \|\tilde{z}_i - \tilde{\mathbf{R}}_\mathbf{i}\tilde{\mathbf{sc}}_\mathbf{i}^{\mathbf{k},\mathbf{N_C}}\|^2 + PD_{i+1}, \tag{7}$$

where N_C is the number of child nodes of the k-th parent node in the $(i+1)$-th layer and $\tilde{R}_i$ is the i-th row of $\tilde{\mathbf{R}}$. Once a child node is selected as one of K candidates, its parent node enumerates the next best child node. This sorting scheme only needs to expand $2K$ child nodes in one layer, making it a promising method for high-order modulation scheme.

C. Max-Log List Demapper

In a coded MIMO system, log-likelihood ratio (LLR) is often used in a soft-output detector to improve the error rate performance. The *a posteriori* LLR generated by the MIMO detector is calculated by

$$L_O(x_i|\mathbf{y}) = \ln \frac{\sum_{\mathbf{x}:x_i=+1} e^{-\frac{\|\mathbf{y}-\mathbf{Hs}\|^2}{2\sigma_n^2} + \frac{1}{2}\mathbf{x}^\mathbf{T}\mathbf{L_A}}}{\sum_{\mathbf{x}:x_i=-1} e^{-\frac{\|\mathbf{y}-\mathbf{Hs}\|^2}{2\sigma_n^2} + \frac{1}{2}\mathbf{x}^\mathbf{T}\mathbf{L_A}}}, \tag{8}$$

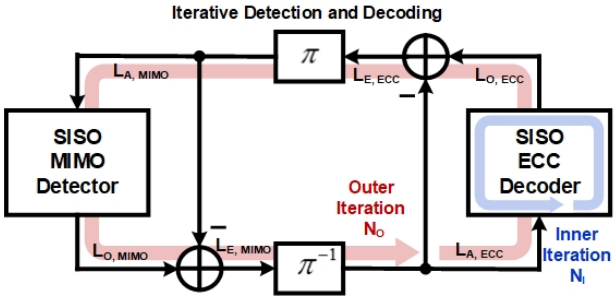

Fig. 1. Illustration of an IDD system.

where $\mathbf{L_A}$ is the soft-input LLR. Calculation for $\mathbf{L_A}$ is realized by max-log approximation with a list demapper:

$$\begin{aligned} L_O(x_i|\mathbf{y}) \approx \frac{1}{2}\max_{\mathbf{x}\in X_c, x_i=+1}\{-\frac{\|\mathbf{y}-\mathbf{Hs}\|^2}{\sigma_n^2} + \mathbf{x}^\mathbf{T}\mathbf{L_A}\} \\ -\frac{1}{2}\max_{\mathbf{x}\in X_c, x_i=-1}\{-\frac{\|\mathbf{y}-\mathbf{Hs}\|^2}{\sigma_n^2} + \mathbf{x}^\mathbf{T}\mathbf{L_A}\}, \end{aligned} \tag{9}$$

where X_c is a list of candidates. List demapper is favored because of its reduced tree search complexity. Te LRA-K-best search scheme is used to generate the candidate list, which is then used for the demapper and LLR calculation.

III. Iterative Detection and Decoding

IDD is based on the concept of turbo decoding [12]. Fig. 1 shows the information exchange in an IDD system, where N_o is the number of outer iterations and N_i is the number of inner iterations. IDD iteratively exchanges extrinsic LLRs $\mathbf{L_E}$, as given by

$$\mathbf{L_E} = \mathbf{L_O} - \mathbf{L_A}, \tag{10}$$

where $\mathbf{L_O}$ is the output LLRs, exchanged between the SISO MIMO detector and the SISO ECC decoder to improve the error rate performance. Typically, the same number of inner iterations is applied for all outer iterations. Under this situation, the processing latency is proportional to the number of outer iterations.

A. Extrinsic Information Transfer (EXIT) Chart

The EXIT chart is an effective tool for analyzing iterative decoding schemes, such as serial concatenation code and parallel concatenation code [13]. In our system, MIMO detection and LDPC decoding can be viewed as a serial concatenation code, so the EXIT chart can be used to analyze the convergence behavior of the detector and decoder. The number of inner and outer iterations can be seleted properly to minimize the overall latency for iterative processing.

The mutual information can be extracted by

$$I \approx 1 - \frac{1}{N}\sum_{n=1}^{N}\log_2(1+e^{-x_n L_n}), \tag{11}$$

where N is the number of bits, $x_n \in \{+1,-1\}$ is the value of the n-th bit mapped from $\{0,1\}$, and L_n is the associated LLR value. The EXIT chart can be used to estimate the extrinsic

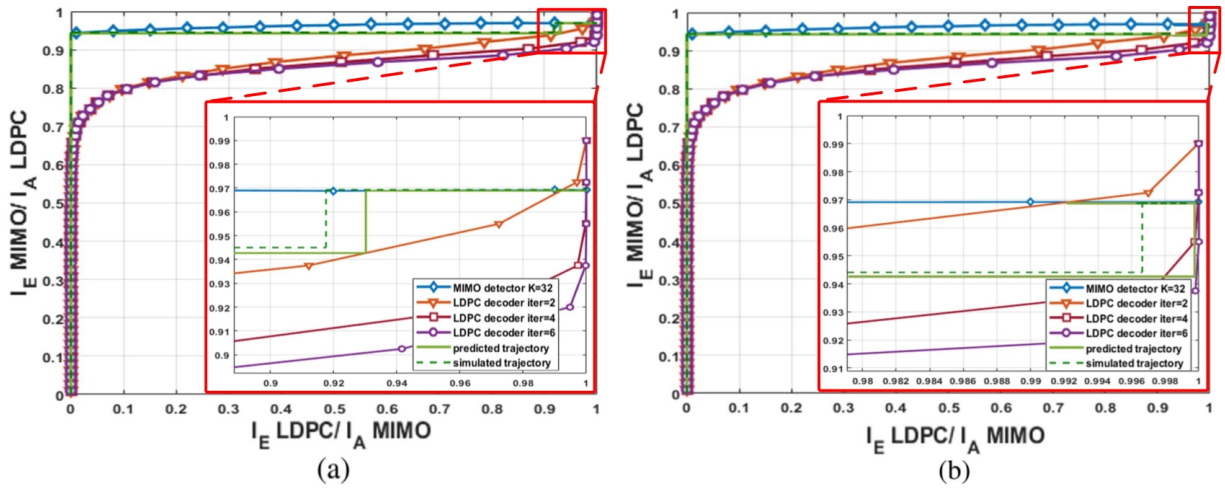

Fig. 2. EXIT chart of MIMO detector and LDPC decoder, and trajectory of (a) IDD with (3, 2/4/6) iterations and (b) IDD with (3, 6/4/2) iterations.

information and *a priori* information, as described in [14]. The mutual information I ranges from 0 to 1, which can be viewed as a quality indicator of LLRs. The relation between the *a priori* mutual information I_A and the extrinsic information I_E is used to find the transfer characteristic of the detector and decoder. The mutual information of the output extrinsic LLR corresponding to the input LLR can be found with this transfer characteristic. The roles of the detector and decoder exchange in the EXIT chart after each detection or decoding. The exchange of extrinsic information can be visualized as decoding on a zig-zag trajectory in the EXIT chart.

B. EXIT-Based IDD Strategy

The overall processing latency is a critical issue for implementation of a practical IDD receiver. The EXIT chart can be leveraged to design the IDD strategy. Fig. 2 shows the transfer characteristics of the MIMO detector and LDPC decoder with feasible numbers of inner iterations given possible numbers of outer iterations. Fig. 2 (a) shows the EXIT chart with 3 outer iterations and respective 2, 4, and 6 inner iterations, as denoted by (3, 2/4/6). The simulations are performed at SNR = 40dB for channel model B. It is noted that the predicted trajectory is slightly different from the simulated trajectory since interleaving with an infinite length is assumed to be applied in the EXIT chart. The transfer characteristics of the LDPC decoder with 2, 4, and 6 inner iterations diverge when the I_A of MIMO is close to 1. This indicates that performance degradation due to a reduction in the number of LDPC inner iterations is more evident when the input information is higher in the later outer iterations. Fig. 2 (b) shows the EXIT chart of IDD with decreasing inner iteration numbers. As can be seen, the transfer characteristic of the LDPC decoder with 2 iterations intersects the transfer characteristic of the MIMO detector at a smaller I_A. Thus, the trajectory turns back and the performance in the third outer iteration is actually worse than that in the second outer iterations. This finding suggests that the the number of inner iterations needs to be arranged in an increasing order.

Fig. 3 shows the PER with various combinations of inner and outer iterations. A 4×4 MIMO system with K-best detection (K = 32, 64) is used here. LDPC with a code rate of 5/6 is adopted to meet the specification of 802.11 ax. Fig. 3(a) shows that the PER performance with three outer iterations (3, 6/4/2) is even worse than the case with two outer iterations (2, 6/4). Fig. 3(b) shows that the IDD with increasing N_I performs best given the same number of total inner iterations. The error performance difference between the (3, 2/4/6) and (3, 6/6/6) IDD configurations is smaller than 0.05dB. The difference between (3, 2/4/12) and (3, 12/12/12) IDD configurations is also smaller than 0.05dB at PER = 0.1, reducing the total number of total iterations by 50%. This verifies our speculation that arranging N_I in an increasing order achieves a better performance. This strategy enables a practical IDD design with a minimized processing latency, which is not proportional to the number of outer iterations.

IV. Architecture of MIMO Detector

The MIMO detector includes a preprocessing engine and a SISO LRA-K-Best detector for 4×4 systems, as shown in Fig. 4. 6-bit LLR is used for soft information exchange. Pipelined architecture is applied to all the processing units to achieve a high throughput, as specified in the 802.11ax specification. Hardware parallelism is also applied to the MIMO detector based on the 802.11ax latency requirement. The clock frequency is set to 320 MHz.

A. Preprocessing Engine

The preprocessing engine is used to perform QR-decomposition and lattice reduction. For QR-decomposition, The channel matrix $\mathbf{H}$ is decomposed into an unitary matrix $\mathbf{Q^H}$ and an upper-triangle matrix $\mathbf{R}$. The Givens rotation (GR) algorithm is adopted. A pipelined coordinate rotation digital

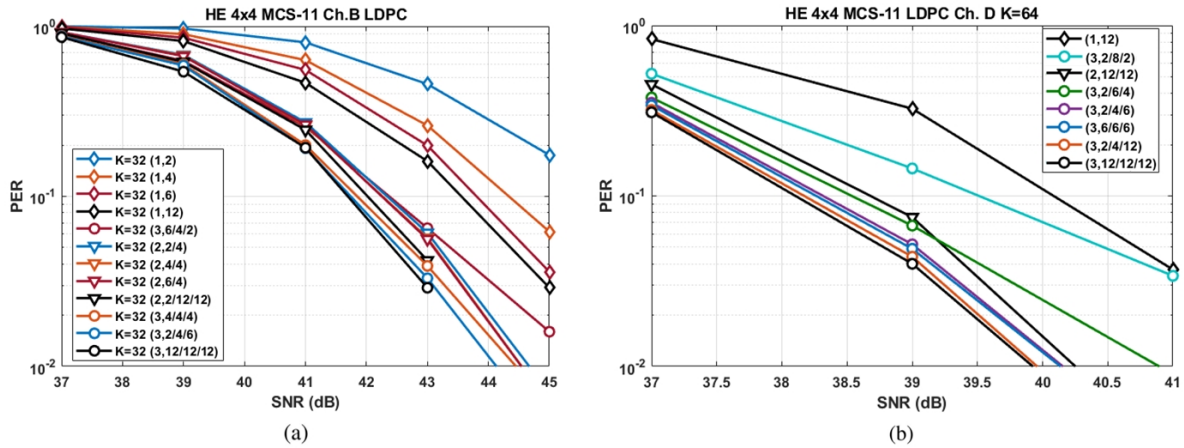

Fig. 3. PER performance of IDD with LDPC with different combinations of inner iterations for channel models (a) B and (b) D.

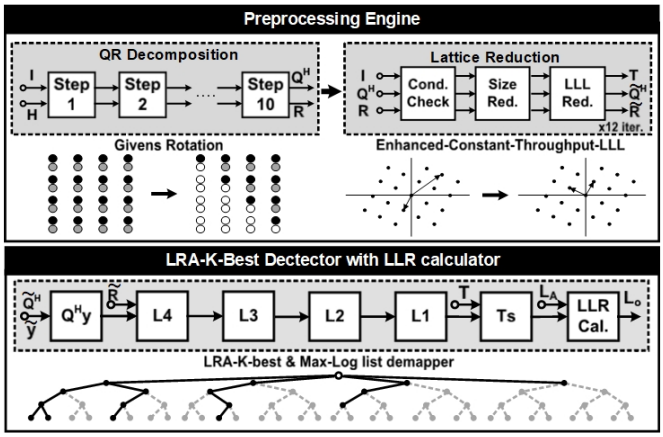

Fig. 4. Hardware architecture for the MIMO detector.

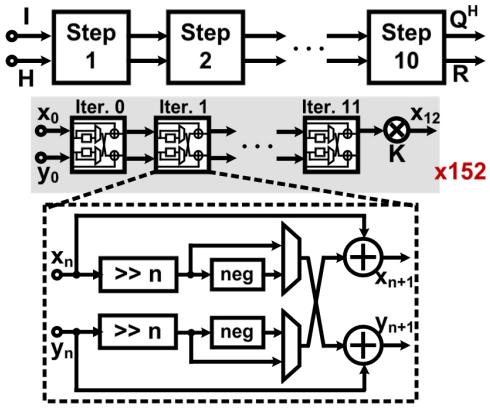

Fig. 5. Implementation of Givens rotation by CORDIC.

computer (CORDIC) is utilized to implement Givens rotation, shown in Fig. 5. Vectors in the same rows are simultaneously rotated using respective CORDICs.

Regarding lattice reduction, size reduction and LLL reduction are processed iteratively, for performing the ECTLLL algorithm. The pipelined architecture is applied to our LR

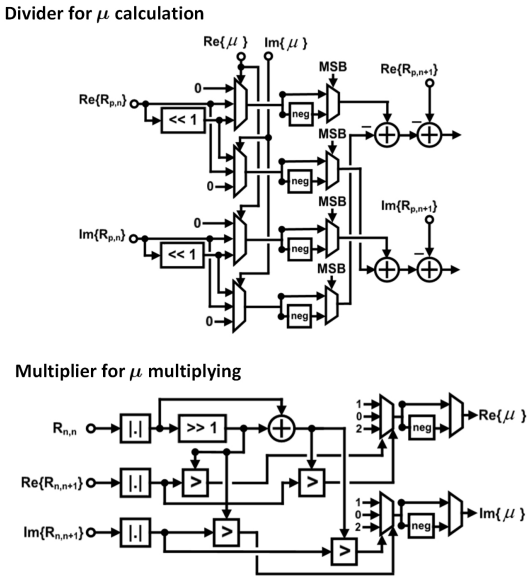

Fig. 6. μ calculation for the LR calculator.

engine. The divider and multiplier for operations associated with μ (described in (4) and (5)) can be simplified since over 99% values of μ range from $+2$ to -2, based on the simulation result in [10]. Fig. 6 illustrate divider and multiplier can be simplified by a few multiplexers, comparators and adders. CORDICs are also applied to lattice reduction since LLL reduction may swap columns of $\tilde{\mathbf{R}}$ and GR is needed to maintain $\tilde{\mathbf{R}}$ as an upper triangular matrix.

B. LRA-K-Best Detector with LLR calculator

Fig. 7 shows the architecture for the LRA-K-best detector that includes two matrix-vector multiplier arrays for computing $\tilde{\mathbf{Q}}^{\mathbf{H}}\tilde{\mathbf{y}}$ and $\mathbf{T}\tilde{\mathbf{s}}$, four processing elements (L4 to L1) for K-best search, and one LLR calculator for generating soft output. Multiply-accumulate operations for matrix-vector multiplication are performed in parallel to achieve the highest

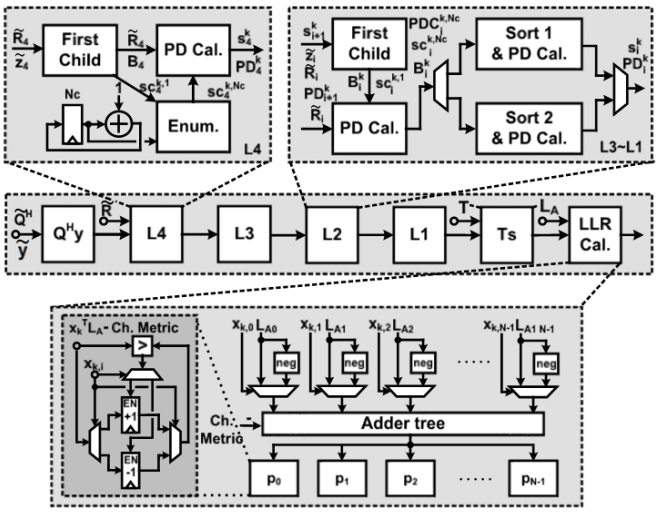

Fig. 7. LRA-*K*-Best detector with an LLR calculator.

throughput. For *K*-best search, only the first child node for the fourth layer needs to be found while other candidates are enumerated by an enumerator. For each of the third to first layers, the result is passed to a sorting unit after the first child node and its PD is generated. Two sorting units are needed in each layer to maximize the throughput, since $2K$ nodes are need to enumerate for each layer. A boundary check is performed after $\tilde{\mathbf{s}}$ is converted back to the origin domain.

The LLR calculator computes the channel metric and *a priori* metric and update the values for all bits. The LLR calculator uses the bit value corresponding to the candidate to decide whether to change the sign of LLR input or not to calculate the *a priori* metric.

V. Design Space Exploration

For the 802.11ax system, the most challenging case with 160MHz channel bandwidth and MCS-11 is considered here. 1960 sub-carriers for the OFDM are used for the 160MHz channel. Table I shows the hardware mapping estimates in a 28nm technology. The area, power, and the latency of the K-best detector is positively correlated to the value of K. The data related to the LDPC decoder are extracted from an in-house IP. The latency of LDPC decoder is proportional to the number of inner iterations N_I. The PER = 0.1 is set here as the error performance specification, as specified in the standard. Table II shows the required SNR to achieve PER = 0.1 for the WLAN channels B, D, and E. As can be seen, the PER performance of the IDD receiver can be further improved without introducing an overall latency proportional to the N_O, given the same value of *K*.

A short inter frame space (SIFS) of 16μs and a 16μs packet extension (PE) are considered. Medium access control (MAC) and FFT (including reordering) take 2μs and 4μs, respectively, so the overall processing time needs to be shorter than 26μs. The data rate of MCS-11 with 4 spatial streams for a 160MHz bandwidth is 4.8Gbps (or 5.76Gbps for code bits). The total processing time for IDD can be estimated by considering the

TABLE I
Hardware Mapping for IDD Configurations

	Area (mm^2)	Power (mW)	Latency (μs)	Data Rate (Gbps)
QRD engine	0.312	122	0.16	6.4
LR engine	1.1	427	0.64	6.4
K-best detector (K=16)	0.338	121	0.32	0.8
K-best detector (K=32)	0.5	178	0.52	0.4
K-best detector (K=64)	0.825	294	0.92	0.2
LLR calculator	0.012	4.3	0.206	0.2
LDPC decoder (N_I=2)	0.245	170	0.279	6.954
LDPC decoder (N_I=4)	0.245	170	0.559	3.477
LDPC decoder (N_I=6)	0.245	170	0.838	2.318
LDPC decoder (N_I=10)	0.245	170	1.397	1.391
LDPC decoder (N_I=12)	0.245	170	1.677	1.159

TABLE II
PER Performance of IDD Receiver

Parameters	Required SNR (dB) for PER = 0.1		
(N_O, N_I, K)	Channel B	Channel D	Channel E
(1, 12, 16)	43.6	40.4	41.59
(1, 12, 32)	43.54	40.2	41.37
(1, 12, 64)	43.51	40.1	41.29
(2, 2/10, 16)	42.4	39.5	40.4
(2, 2/10, 32)	42.1	39.0	39.94
(2, 2/10, 64)	41.96	38.8	39.63
(3, 2/4/6, 16)	42.22	39.5	40.35
(3, 2/4/6, 32)	41.75	38.8	39.56
(3, 2/4/6, 64)	41.55	38.4	39.32
(3, 2/4/12, 16)	42.17	39.1	39.99
(3, 2/4/12, 32)	41.7	38.5	39.38
(3, 2/4/12, 64)	41.5	38.2	39.07

latencies of the MIMO detector and the LDPC decoder. For the MIMO detector, the LRA-*K*-Best detector is only executed in the first outer iteration and the selected *K* candidates are reused in the following iterations. The LLR calculator is executed for every outer iteration. For the LDPC decoder, the latency is proportional to the total number of inner iterations. The preprocessing engines, detector and decoder need to be parallelized to achieve the required data rate of 5.76Gbps. The levels of parallelism of the MIMO detector and the LDPC decoder increase throughput proportionally without decreasing the latency. The tone demapper is used when LDPC is applied, but tone demapping can be done as the reordering of FFT is exeuted. Thus, the LDPC decoder can be parallelized to make its throughput slightly higher than the MIMO detector and only its latency is concerned.

Table III shows the required levels of parallelism for the MIMO detector and the LDPC decoder to meet the processing time constraint, where *P* stands for the level of parallelism. Fig. 8 visualizes the performance of the IDD configurations in terms of area, power, and required SNR for PER = 0.1. A non-IDD receiver (with N_O = 1) with a higher *K* value still cannot effectively improve the PER performance, but this results in considerable cost in area and energy. An IDD receiver with a higher *K* also has an marginal performance improvement at the cost of significant power and area overheads. Compared to the best non-IDD receiver, the IDD reciver with *K* = 16 and configuration (3, 2/4/12) achieves an 1dB improvement in

TABLE III
HARDWARE COST EVALUATION OF IDD RECEIVER

Parameters (N_O, N_I, K)	MIMO* (P)	LDPC (P)	Area (mm^2)	Power (W)
(1, 12, 16)	8×	5×	5.4	2.4
(1, 12, 32)	15×	5×	10.2	4.1
(1, 12, 64)	29×	5×	26.6	9.9
(2, 2/10, 16)	8×	6×	6.4	2.8
(2, 2/10, 32)	15×	6×	11.8	4.8
(2, 2/10, 64)	29×	6×	29.3	10.9
(3, 2/4/6, 16)	8×	6×	6.9	3.0
(3, 2/4/6, 32)	15×	6×	12.6	5.0
(3, 2/4/6, 64)	29×	6×	30.9	11.5
(3, 2/4/12, 16)	8×	8×	7.4	3.3
(3, 2/4/12, 32)	15×	8×	13.1	5.3
(3, 2/4/12, 64)	29×	8×	31.4	11.8

* Preprocessing engine is only executed once before IDD

PER with 3.6× less area and 3.0× less power.

VI. CONCLUSION

This work presents the first 802.11ax compliant IDD receiver in the open literature that supports up to 1024-QAM modulation. Latice reduction is adopted to deal with such a high-order modulation. The EXIT chart is used to analyze the convergence behavior of the IDD receiver to identify proper combinations of inner and outer iterations. According to the analysis, the number of inner iterations needs to be arranged in an increasing order. This reduces the computational complexity while achieving nearly the same PER. Given the parameters of hardware modules, a design methodology is presented to explore the design space in terms of area, power, and error performance. Extensive simulations are conduced to verify the performance in the required WLAN channels. The proposed IDD receiver with the iteration configuration (3, 2/4/12) and K = 16 achieves even better PER performance with much lower area and power costs when compared to the non-IDD one with (1, 12) and K = 64. This provides a promising solution for IDD receiver for low-latency, energy-constrained systems.

ACKNOWLEDGMENT

This work was supported by Realtek Semiconductor Corp. The authors also thank Taiwan Semiconductor Research Institute (TSRI) for technical support on EDA infrastructure.

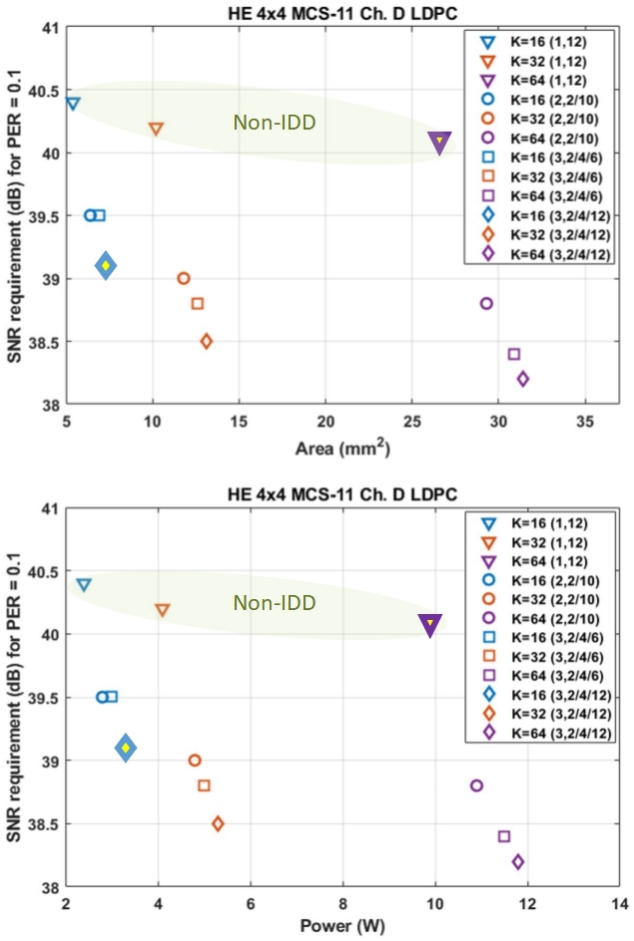

Fig. 8. Design space exploration with respect to area, power, and required SNR to achieve PER = 0.1.

REFERENCES

[1] D.-J. Deng, K.-C. Chen and R.-S. Cheng, "IEEE 802.11ax: Next generation wireless local area networks," *International Conference on Heterogeneous Networking for Quality, Reliability, Security and Robustness*, Aug. 2014.

[2] B. Bellalta, "IEEE 802.11ax: High-efficiency WLANS," *IEEE Wireless Communications*, vol. 23, pp. 38-46, March 2016.

[3] M. Tuchler, R. Koetter and A.C. Singer, "Turbo equalization: principles and new results," *IEEE Transaction on Communications*, vol. 50, pp. 754-767, May 2002.

[4] M.-X. Chang and W.-Y. Chang, "Maximum-Likelihood Detection for MIMO Systems Based on Differential Metrics," *IEEE Transactions on Signal Processing*, vol. 65, pp. 3718-3732, July 2017.

[5] A. Wiesel, Y.C. Eldar and S. Shamai, "Semidefinite relaxation for detection of 16-QAM signaling in MIMO channels," *IEEE Signal Processing Letters*, vol. 12, pp. 653-656, Sep. 2005.

[6] Z.-Q. Luo, W.K. Ma, A. M.-C. So, Y. Ye and S. Zhang, "Semidefinite Relaxation of Quadratic Optimization Problems," *IEEE Signal Processing Magazine*, vol. 27, pp. 20-34, May 2010.

[7] W. Zhang, and X. Ma, "Low-Complexity Soft-Output Decoding with Lattice-Reduction-Aided Detectors," *IEEE Transactions on Communications*, vol. 58, pp. 2621-2629, Sep. 2010.

[8] T.-J. Hsieh and W.-H. Sheen, "A Lattice-Reduction-Aided Max-Log List Demapper for Coded MIMO Receivers," *IEEE Transactions on Vehicular Technology*, vol. 63, pp. 664-673, Feb. 2014.

[9] K. Lenstra, W. Lenstra, Jr., and L. Lovász, "Factoring polynomials with rational coefficients," *Math. Ann. Proc*, vol. 261, pp. 515-534, Dec. 1982.

[10] A. Youssef, M. Shabany, and P. G. Gulak, "VLSI implementation of a hardware-optimized lattice reduction algorithm for WiMAX/LTE MIMO detection," *In Proceedings of IEEE International Symposium on Circuits and Systems*, June 2010.

[11] M. Shabany and P. G. Gulak, "The application of lattice-reduction to the K-best algorithm for near-optimal MIMO detection," *IEEE International Symposium on Circuits and Systems*, pp. 316–319, May 2008.

[12] C. Berrou, A. Glavieux and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: Turbo-codes. 1," *IEEE International Conference on Communications*, pp. 1064-1070, May 1993.

[13] J. Hagenauer, "The EXIT chart - introduction to extrinsic information transfer in iterative processing," *European Signal Processing Conference*, pp. 1541-1548, Sep. 2004.

[14] M. El-Hajjar and L. Hanzo, "EXIT Charts for System Design and Analysis," *IEEE Communications Surveys & Tutorials*, vol. 16, pp. 127-153, May 2013.