Chen-Chien Kao

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Research Interests

Energy-efficient hardware accelerator for digital signal processing, machine learning, and baseband communication

Education

M.S. in Electronics Engineering, National Taiwan University Feb. 2019 - Jan. 2022

- Thesis: Design and Implementation of a Hybrid Precoding Processor for mmWave Massive MIMO System
- Advisor: Prof. Chia-Hsiang Yang
- Cumulative GPA: 4.19/4.30

B.S. in Electrical Engineering, National Taiwan University Sep. 2015 - Jan. 2019

- Cumulative GPA: 4.19/4.30 (Rank: **9th**/190)

Honor and Award

IEEE CASS Student Travel Grant July 2022

Dialog Award (Given to excellent students for outstanding research) 2020, 2022

Excellence Award, Macronix Golden Silicon Contest (300+ teams) Aug. 2020

Second Place, 2019 Artificial Intelligence Cup, Ministry of Education, Taiwan (70+ teams) Apr. 2020

Presidential Award, 2 times, National Taiwan University (Ranked top 5% in academy) 2015-2019

College Student Research Creativity Award, July 2019
Ministry of Science and Technology, Taiwan (Ranked top 10 % in 2000 projects)

Excellence Award, CAD Contest, Ministry of Education, Taiwan Dec. 2018

Publications

- **C.-C. Kao**, C.-E. Chen, C.-H. Yang, "Hybrid Precoding Baseband Processor for 64x64 Millimeter Wave MIMO Systems," *IEEE Trans. Circuits & Systems I (TCAS-I)*, vol. 69, no. 4, pp. 1765-1773, Apr. 2022.
- **C.-C. Kao**, Y.-Y Hsieh, C.-H. Chen, and C.-H. Yang, "Hardware Acceleration in Large-Scale Tensor Decomposition for Neural Network Compression," *Int. Midwest Symposium on Circuits and Systems (MWSCAS)* Aug. 2022.
- Y.-P. Wang, C.-C. Wen, **C.-C. Kao**, C.-J. Huang, D.-Z. Liu, and C.-H. Yang, "Iterative Receiver with a Lattice-Reduction-Aided MIMO Detector for IEEE 802.11ax," *Global Communications Conference (GLOBECOM)*, Dec. 2020.
- C.-C. Wen, Y.-C. Lee, Y.-C. Wu, **C.-C. Kao**, C.-H. Yang, "A 1.96 Gb/s Massive MU-MIMO Detector for Next-Generation Cellular Systems," *Int. Symposium on VLSI Circuits (VLSI Circuits)*, June 2020.
- S.-J. Yu, **C.-C. Kao**, C.-H. Huang and I.H.-R. Jiang, "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability," *2020 25th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2020. (**Best Paper Award**)

Research and Work Experience

Research Assistant Feb. 2022 - present
Digital Circuits and Systems Lab, National Taiwan University

- Advisor: Prof. Chia-Hsiang Yang
- Optimized the algorithm for tensor decomposition to reduce its computational complexity
- Developed an accelerator for corresponding optimized tensor decomposition algorithm

Intern Dec. 2020 - present
Tron Future Tech

- Supervisor: Dr. Borching Su
- Designed IP for direct digital synthesizer and analyzed its performance
- Implemented IPs for various radar systems

Graduate Student Researcher Feb. 2019 - Jan. 2022
Digital Circuits and Systems Lab, National Taiwan University

- Advisor: Prof. Chia-Hsiang Yang
- Analyzed various hybrid precoding algorithms in mmWave systems
- Designed an efficient processor for hybrid precoding in mmWave systems with cell-based design flow
- Participated in MIMO detector projects for massive MU-MIMO and IEEE 802.11ax

Undergraduate Student Researcher Sep. 2017 - Jan. 2019
Digital Circuits and Systems Lab, National Taiwan University

- Advisor: Prof. Chia-Hsiang Yang
- Conducted tensor decomposition algorithms on neural network for weight compression
- Designed a tensor decomposition processor for neural network compression

Teaching Experience

Teaching Assistant, National Taiwan University Sep. 2020 - Jan. 2021
Computer-aided VLSI System Design

- Gave lectures and graded exams for 100+ students
- Answered students' questions about the content in lectures off the course

Teaching Assistant, National Taiwan University Sep. 2018 - Jan. 2019
Digital Circuit Lab

- Assisted 30 students in 10 groups about circuit design on FPGA platform
- Helped solving students' problems during labs in the course

Skills

Programming Language: Verilog, MATLAB, Python, C/C++
Circuit Design Tools: NC-Verilog, Verdi/nWave, Design Compiler, Innovus, Calibre
FPGA Design Tools: Altera Quartus, Vivado (Xilinx)

References

- **Prof. Chia-Hsiang Yang** (M.S. advisor)
  Professor, Department of Electrical Engineering
  National Taiwan University
  chyee@ntu.edu.tw
- **Dr. Borching Su** (Supervisor at Tron Future)
  Chief Technology Officer
  Tron Future Tech
  borching@ntu.edu.tw
- **Prof. Chiao-En Chen** (Committee member of oral defense)
  Professor, Department of Electrical Engineering
  National Chung Hsing University
  chiaoenchen@nchu.edu.tw