Hybrid Precoding Baseband Processor for 64 × 64 Millimeter Wave MIMO Systems

Chen-Chien Kao, Chiao-En Chen, *Senior Member, IEEE*, and Chia-Hsiang Yang, *Senior Member, IEEE*

***Abstract*— This paper presents a hybrid precoding processor for millimeter wave (mmWave) multiple-input-multiple-output (MIMO) communication systems. The proposed architecture supports 64 antennas with 4-to-8 RF chains, and 4-bit phase resolution for each phase shifter in the analog beamformer. A polar decomposition (PD) engine is designed to achieve a 2.4-to-8.6× lower latency with 1.5-to-1.7× less normalized gate count compared to the singular value decomposition (SVD)-based implementation for the same functionality. Multiplicands are combined to reduce 55% area by utilizing the distributive property. Approximate phase extraction and low-precision multiplication for quantized phase extraction are adopted, which leads to 43% and 41% area reductions, respectively. The proposed hybrid precoding processor is designed in a 40-nm CMOS technology. It delivers a throughput of up to 10,288 kMat/s and consumes 170.9 mW at 278 MHz. It outperforms the state-of-the-art hybrid precoding processors with 5.5-13.7× higher normalized area efficiency and 6.9-38.4× lower normalized energy.**

***Index Terms*— Millimeter wave (mmWave), multiple-input multiple-output (MIMO), hybrid precoding, integrated circuits.**

I. Introduction

DUE to the exponentially increasing mobile traffic from the data-hungry smart phones, tablets, and other mobile devices, it is projected that the next-generation networks will have to provide 1,000 times capacity increase compared to what we have today [1]. In order to achieve this goal, a number of promising technologies have been proposed [2]–[4]. Millimeter wave (mmWave) communication as one of these enabling technologies, allows the access of additional tens of gigahertz bandwidth within the 3 to 300 GHz bands [5] for data communications, and hence has drawn intense research attention lately.

One major obstacle that hinders the feasibility of millimeter wave communications is the high path loss characteristic resulting from the increase of carrier frequency [6]–[8].

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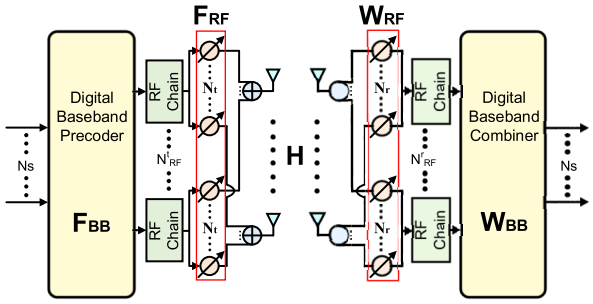

Fig. 1. Hybrid transceiver architecture for mmWave systems.

Fortunately, when combined with massive multiple-input-multiple-output (MIMO) technology, the small wavelength of mmWave signals allows large antenna arrays to be packed into a small area/volume so that sufficient beamforming gain can be harvested to compensate for the path loss. From the hardware perspective, cost-effective CMOS technologies for mmWave communication have also started to mature [9]–[11]. These facts suggest that the combination of mmWave communication with massive MIMO is expected to be a viable solution in future wireless systems.

In order to achieve the high data rates promised by the capacity of mmWave MIMO, multi-stream transmission via precoding and combining should be adopted. Conventionally, the precoders and combiners are implemented at the baseband where a dedicated RF chain is required for each antenna element. In mmWave MIMO where the number of antennas to be deployed is often massive, full baseband processing can be very expensive. Consequently, under the assumption that the number of antenna elements is much larger than the number of RF chains, a more practical way to implement the precoding/combining in mmWave MIMO is through hybrid precoding/combining. Fig. 1 shows the transceiver architecture of a mmWave system employing hybrid precoder at the transmitter and hybrid combiner at the receiver. The hybrid precoder/combiner consists of a two-stage concatenated structure, where an analog precoder/combiner is performed at the RF front-end using phase-shifters while a dimension-reduced digital precoder/combiner is performed at baseband. With some careful design, the above hybrid transceiver is shown to achieve a spectral efficiency very close to that of the full digital transceiver but with much lower hardware complexity. A number of hybrid transceiver designs have been proposed in the literature (see [12]–[14] and references therein).

While there have been a large number hybrid precoding/combining algorithms presented over the last few years, only a few research efforts have been contributed to their hardware implementation. In [15], a parallel-index-selection matrix-inverse-bypass simultaneous orthogonal matching pursuit (PIS-MIB-SOMP) algorithm as well as its hardware architecture was proposed. The PIS-MIB-SOMP algorithm not only eliminates the need of direct matrix inversion, but also enables more efficient basis selection and update procedure. Consequently the PIS-MIB-SOMP admits much lower computational complexity compared to the original SOMP counterpart [13]. Motivated by the orthogonal matching and local search (OM + LS) method proposed in [16], a low complexity hybrid precoding algorithm and its hardware architecture is proposed in [17]. Reference [17] developed an efficient local search algorithm that performs array response vector selection among multiple orthogonal codebooks, and was shown to achieve better hardware efficiency compared to [15]. In [18], a high-throughput hybrid precoder design was proposed based on a modification of the orthogonal matching pursuit (OMP) algorithm and a new least-square computing algorithm. The new least-square computing algorithm proposed in [18] is based on the QR decomposition, making it very suitable to be implemented using efficient Coordinate Rotation Digital Computer (CORDIC).

In contrast to existing hybrid precoding processors which are mostly based on the OMP algorithm [19], [20], we choose to develop our hybrid precoding processor based on the phase extraction alternating minimization (PE-AltMin) algorithm [21]. Compared to the existing OMP algorithm, the PE-AltMin algorithm is known to achieve higher spectral efficiency while exhibiting lower computational complexity than the manifold optimization based AltMin (MO-AltMin) one, and hence is very suitable for hardware implementation [21]. To avoid performing computationally intensive singular value decomposition (SVD) required in each iteration of the PE-AltMin algorithm, a low-complexity algorithm based on polar decomposition (PD) is proposed. This work represents our research efforts in proposing the world's first PE-AltMin algorithm-based processor. The proposed processor supports 4-to-8 data streams with feasible 4-to-8 RF chains. It is able to achieve better area and energy efficiency than the state-of-the-art designs. The contributions of this work are as follows:

- This work is the first hybrid precoding processor that implements the PE-AltMin precoding algorithm. Better spectral efficiency performance is exhibited compared to its OMP-based counterparts.
- We replace the direct-mapped SVD processor with multipliers that originally required in the PE-AltMin precoding algorithm by the proposed PD engine, which achieves a 2.4-to-8.6× lower latency with 1.5-to-1.7× less normalized gate count compared to the similar configuration of SVD processor without the multipliers for matrix multiplication of singular vectors.
- Low-precision arithmetic is leveraged to approximate the matrix multiplication in the phase extractor, which saves 41% of area. Additionally, the proposed approximate phase extractor extracts quantized phase through shift-and-add operations, further saving 43% of area.
- The proposed multiplicand combiner in the correlation engine reduces the number of constant multipliers by utilizing the distributive property of multiplication, saving 55% of area.
- The proposed PE-AltMin-based hybrid precoding processor achieves a 5.5-to-13.7× higher area efficiency with 6.9-to-38.4× lower energy than prior arts.

The remainder of this work is organized as follows. Section II describes the system model of the considered mmWave MIMO system. Section III introduces the proposed PD-based PE-AltMin algorithm. Section IV shows the system architecture of the proposed hybrid precoding processor. Section V presents the implementation results in comparison to the state-of-the-art designs. Finally, Section VI concludes this paper.

II. System Model and PE-AltMin Algorithm

A. System Model and Problem Formulation

Consider a single user mmWave MIMO system as shown in Fig. 1, where N_s data streams are sent and the transmitter and the receiver are equipped with N_t and N_r antennas. N_{RF}^t and N_{RF}^r indicate the number of the RF chains at the transmitter and receiver, respectively. We assume $N_{RF}^t = N_{RF}^r$ in this work and use N_{RF} to represent either of them for simplicity. Following the standard flat fading channel assumption, the transmitted signal and received signal can be expressed as:

$$\mathbf{y} = \sqrt{\rho}\mathbf{W}_{BB}^H\mathbf{W}_{RF}^H\mathbf{H}\mathbf{F}_{RF}\mathbf{F}_{BB}\mathbf{s} + \mathbf{W}_{BB}^H\mathbf{W}_{RF}^H\mathbf{n}, \tag{1}$$

where $\mathbf{y}$ is an $N_r \times 1$ received signal, ρ is the received power, $\mathbf{H}$ is an $N_r \times N_t$ channel matrix, $\mathbf{s}$ is an $N_s \times 1$ symbol vector with covariance matrix $\mathbb{E}[\mathbf{s}\mathbf{s}^H] = \frac{1}{N_s}\mathbf{I}_{N_s}$, and $\mathbf{n}$ is the noise vector. $\mathbf{F}_{RF}$ and $\mathbf{F}_{BB}$ denote the analog RF precoding matrix and the digital baseband precoding matrix, respectively, while $\mathbf{W}_{RF}$ and $\mathbf{W}_{BB}$ denote the analog RF combining matrix and the digital baseband combining matrix, respectively. To capture the fading characteristic of a mmWave MIMO channel, the extended Saleh-Valenzuela model (S-V model) [22] is assumed in this paper.

The hybrid transceiver design problem can be divided into two parts: the precoder design and the combiner design. In [20], [23], it is shown that when the spectral efficiency is to be maximized, the precoder and combiner design problems can be formulated in a unified mathematical form. Consequently, this work only focuses on the precoder design problem, while the same design methodology can be applied to the combiner design problem. The hybrid precoder design problem can be mathematically formulated as [20], [23]:

$$\begin{aligned} \min_{\mathbf{F}_{RF},\mathbf{F}_{BB}} \quad & \|\mathbf{F}_{opt} - \mathbf{F}_{RF}\mathbf{F}_{BB}\|_F^2 \\ \text{subject to} \quad & \mathbf{F}_{RF} \in \mathcal{A} \\ & \|\mathbf{F}_{RF}\mathbf{F}_{BB}\|_F^2 = N_s \end{aligned} \tag{2}$$

where

$$\mathcal{A} \triangleq \left\{ \left| [\mathbf{F}_{RF}]_{p,q} \right| = 1,\ \forall\ p = 1, \ldots, N_t,\ q = 1, \ldots, N_{RF} \right\},$$

and $\mathbf{F}_{opt}$ is the optimal precoder in the fully digital design that can be obtained from the SVD of $\mathbf{H}$ [24]. Here, N_{RF} RF chains are deployed at the transmitter. Since the objective function is jointly non-convex in $\mathbf{F}_{RF}$ and $\mathbf{F}_{BB}$, the optimization problem in (2) requires optimizing a non-convex objective function over a discrete (and hence non-convex) constraint set and hence is known to be a challenging design problem.

Due to the difficulty of solving (2), a number of algorithms have been proposed to obtain a suboptimal solution. In [20], [23], a hybrid precoder design is proposed based on the OMP algorithm [19]. The OMP-based hybrid precoding algorithm iteratively constructs the analog RF precoder in a column-by-column fashion by finding the basis vector in the dictionary with the highest correlation. Once $\mathbf{F}_{RF}$ is obtained, the algorithm constructs the digital precoder using least square method. Finally, the digital precoder is scaled such that $\mathbf{F}_{RF}\mathbf{F}_{BB}$ satisfies the total power constraint. Due to the success of this algorithm, almost all the existing papers focusing on hardware implementation aspects of hybrid precoding [15], [17], [18] are established from some modifications or variants of the OMP algorithm [19], [20], [25].

B. Review on the PE-AltMin Hybrid Precoding Algorithm

In contrast to the widely adopted OMP-based hybrid precoding, an innovative design methodology was recently proposed based on the principle of alternative minimization (AltMin) [21]. For hybrid precoding design problems with fully-connected transceiver structure, the MO-AltMin algorithm was first proposed to solve the design problem over the Riemannian manifold. The MO-AltMin algorithm directly solves the hybrid precoder problem under the unit modulus constraints and is exhibited to achieve the best spectral efficiency at the expense of the highest computational complexity [21]. The update of the analog precoder in the MO-AltMin algorithm involves computations of the matrix dimension of $N_{RF}N_t \times N_sN_t$. A low-complexity counterpart of the MO-AltMin algorithm, namely, the PE-AltMin was also proposed in [21]. The PE-AltMin algorithm imposes an additional orthogonal property on the digital precoder design. The update of the analog precoder in PE-AltMin is performed on the matrix dimension of $N_t \times N_{RF}$. PE-AltMin algorithm is observed to achieve higher spectral efficiency compared to the OMP-based hybrid precoding algorithms.

To simplify the precoder design problem, an orthogonal property is additionally imposed on the digital precoding matrix in the problem formulation of (2). Specifically, $\mathbf{F}_{BB}$ is assumed to have the structure $\mathbf{F}_{BB} = \alpha\mathbf{F}_{DD}$, where $\mathbf{F}_{DD} \in \mathbb{C}^{N_{RF}\times N_s}$ is a semi-unitary matrix, and $\alpha \in \mathbb{R}$. Substituting $\mathbf{F}_{BB}$ by $\alpha\mathbf{F}_{DD}$, the objective function in (2) is shown to be upper bounded by $\|\mathbf{F}_{opt}\mathbf{F}_{DD}^H - \mathbf{F}_{RF}\|_F^2$. A new hybrid precoder design problem can then by formulated by minimizing this newly derived upper bound over the constraints on $\mathbf{F}_{RF}$ and $\mathbf{F}_{BB}$. The overall mathematical formulation can be expressed as follows [21]:

$$\begin{aligned} \min_{\mathbf{F}_{RF},\mathbf{F}_{DD}} \quad & \|\mathbf{F}_{opt}\mathbf{F}_{DD}^H - \mathbf{F}_{RF}\|_F^2 \\ \text{subject to} \quad & \mathbf{F}_{RF} \in \mathcal{A}, \\ & \mathbf{F}_{DD}^H\mathbf{F}_{DD} = \mathbf{I}_{N_s}. \end{aligned} \tag{3}$$

Algorithm 1 PE-AltMin Algorithm With Phase Quantization

Input: $\mathbf{F}_{opt}$
Output: $\mathbf{F}_{RF}$, $\mathbf{F}_{BB}$
Construct $\mathbf{F}_{RF}^{(0)} \in \mathcal{A}$ with random quantized phases and set $k = 0$
repeat
Compute the SVD: $\mathbf{F}_{opt}^H\mathbf{F}_{RF}^{(k)} = \mathbf{U}^{(k)}\mathbf{S}^{(k)}\mathbf{V}_{:,1:N_s}^{(k)H}$
$\mathbf{F}_{DD}^{(k)} = \mathbf{V}_{:,1:N_s}^{(k)}\mathbf{U}^{(k)H}$
$\arg\{\mathbf{F}_{RF}^{(k+1)}\} = \mathrm{Q}(\arg\{\mathbf{F}_{opt}\mathbf{F}_{DD}^{(k)H}\})$
$k \leftarrow k + 1$
until a stopping criterion triggers
For the digital precoder at the transmit end, normalize $\mathbf{F}_{BB} = \frac{\sqrt{N_s}}{\|\mathbf{F}_{RF}\mathbf{F}_{DD}\|_F}\mathbf{F}_{DD}$

Notably, the constraints in the newly formulated design problem (3) are naturally decoupled in the design variables. With $\mathbf{F}_{RF}$ is fixed, the subproblem regarding to the digital precoder design problem is obtained as:

$$\begin{aligned} \min_{\mathbf{F}_{DD}} \quad & \|\mathbf{F}_{opt}\mathbf{F}_{DD}^H - \mathbf{F}_{RF}\|_F^2 \\ \text{subject to} \quad & \mathbf{F}_{DD}^H\mathbf{F}_{DD} = \mathbf{I}_{N_s}. \end{aligned} \tag{4}$$

With some mathematical derivations, the optimal solution to (4) is shown to be [21]

$$\mathbf{F}_{DD} = \mathbf{V}_{:,1:N_s}\mathbf{U}^H \tag{5}$$

where $\mathbf{F}_{opt}^H\mathbf{F}_{RF} = \mathbf{USV}^H$ is the SVD of $\mathbf{F}_{opt}^H\mathbf{F}_{RF}$. Here $\mathbf{U}$ and $\mathbf{V}$ are both unitary matrices, and $\mathbf{S}$ is a diagonal matrix consisting singular values of $\mathbf{F}_{opt}^H\mathbf{F}_{RF}$ on the diagonal, sorted in descending order.

On the other hand, the analog precoder design problem associated to (3) with $\mathbf{F}_{DD}$ fixed can be obtained in closed as

$$\arg(\mathbf{F}_{RF}) = \arg(\mathbf{F}_{opt}\mathbf{F}_{DD}^H), \tag{6}$$

where $\arg(\cdot)$ is the element-wise phase extraction operator. The PE-AltMin algorithm alternatively optimizing over $\mathbf{F}_{RF}$ and $\mathbf{F}_{DD}$ by (5) and (6) until the algorithm converges. Finally, the digital precoder is given by scaling $\mathbf{F}_{DD}$ to satisfy the power constraint.

C. Phase Quantization for Phase Shifters

The $\mathbf{F}_{RF}$ in the original PE-AltMin algorithm is assumed to be implemented with phase shifters with infinite resolution. However, as the power consumption of phase shifters increases as the resolution increases [26], low-resolution phase shifters are often implemented in practical systems. The phases of phase shifters in each element of $\mathbf{F}_{RF}$ is quantized to 2^B levels, where B is the resolution bit for phase shifters. Consequently, the (p, q)-th element in $\mathbf{F}_{RF}$ can be explicitly expressed as

$$[\mathbf{F}_{RF}]_{p,q} = e^{j\delta}, \tag{7}$$

Algorithm 2 Proposed PE-AltMin Algorithm

Input: $\mathbf{F}_{opt}$
Output: $\mathbf{F}_{RF}$, $\mathbf{F}_{BB}$
1 Construct $\mathbf{F}_{RF}^{(0)} \in \mathcal{A}$ with random quantized phases and set $k = 0$
2 **repeat**
3 $\mathbf{X}^0 = {\mathbf{F}_{RF}^{H}}^{(k)} \mathbf{F}_{opt}/\beta$
4 **for** $n = 0$ **to** $N - 1$
5 $\mathbf{G}^{(n)} = {\mathbf{X}^{(n)}}^H \mathbf{X}^{(n)}$
6 $\mathbf{Q}^{(n)} = \frac{3}{2}\mathbf{I} - \frac{1}{2}\mathbf{G}^{(n)}$
7 $\mathbf{X}^{(n+1)} = \mathbf{X}^{(n)}\mathbf{Q}^{(n)}$
8 **endfor**
9 $\mathbf{F}_{DD}^{(k)} = \mathbf{X}^{(N)}$
10 $arg\{\mathbf{F}_{RF}^{(k+1)}\} = Q(arg\{\mathbf{F}_{opt}{\mathbf{F}_{DD}^{(k)}}^H\})$
11 $k \leftarrow k + 1$
12 **until** a stopping criterion triggers
13 For the digital precoder at the transmit end, normalize $\mathbf{F}_{BB} = \frac{\sqrt{N_s}}{\|\mathbf{F}_{RF}\mathbf{F}_{DD}\|_F}\mathbf{F}_{DD}$

where $\delta = \frac{2n\pi}{2^B}$ for some $n \in \{0, 1, \ldots, 2^B - 1\}$. With the above consideration of finite-resolution phase shifters, we modify the $\mathbf{F}_{RF}$ obtained in PE-AltMin algorithm (6) to the following quantized solution:

$$\arg(\mathbf{F}_{RF}) = \mathrm{Q}(\arg(\mathbf{F}_{opt}\mathbf{F}_{DD}^{H})) \tag{8}$$

where $\mathrm{Q}(\cdot)$ is the quantization operation that quantizes the phase in each element to the nearest quantized angle. The PE-AltMin algorithm with phase-quantization is summarized in Algorithm 1.

III. Proposed PE-AltMin Algorithm

In the PE-AltMin algorithm presented in [21], SVD is the most compute-intensive part. In this work, PD is utilized to eliminate SVD. The proposed PD-based PE-AltMin algorithm enables parallel processing without performance degradation.

According to (5), it is clear that SVD is required to obtain $\mathbf{F}_{DD}$ in each iteration of the original PE-AltMin algorithm. However, SVD is known to be the most computationally intensive operation that dominates the complexity of the overall algorithm. Designs in [28], [29] have proposed hardware architecture for computing SVD, but the computational latency of them is still the bottleneck of the whole architecture. Here, we show that an equivalent implementation can be obtained using PD. Let the PD of $(\mathbf{F}_{opt}^{H}\mathbf{F}_{RF})^H$ be given as

$$(\mathbf{F}_{opt}^{H}\mathbf{F}_{RF})^H = \mathbf{\Theta}\mathbf{P}, \tag{9}$$

where $\mathbf{\Theta} \in \mathbb{C}^{N_{RF} \times N_s}$ is semi-unitary, and $\mathbf{P} \in \mathbb{C}^{N_s \times N_s}$ is a positive-semi-definite Hermitian matrix. Given $\mathbf{F}_{opt}^{H}\mathbf{F}_{RF} = \mathbf{U}\mathbf{S}\mathbf{V}^H$ is the SVD of $\mathbf{F}_{opt}^{H}\mathbf{F}_{RF}$, it is known that $\mathbf{\Theta}$ and $\mathbf{P}$ can be related to $\mathbf{U}$, $\mathbf{S}$, and $\mathbf{V}$ via [27]

$$\mathbf{\Theta} = \mathbf{V}_{:,1:N_s}\mathbf{U}^H, \tag{10}$$

$$\mathbf{P} = \mathbf{U}[\mathbf{S}]_{1:N_s,1:N_s}\mathbf{U}^H. \tag{11}$$

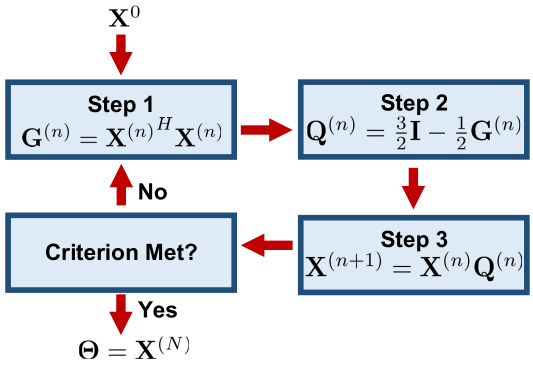

Fig. 2. Flowchart of iterative algorithm for computing PD.

According to (5) and (10), it is clear that $\mathbf{F}_{DD}$ can be equivalently implemented as $\mathbf{\Theta}$ in the PD.

Iterative algorithms can be utilized to compute the unitary matrix $\mathbf{\Theta}$ more efficiently based on binomial expansion [30], [31]. Fig. 2 shows the workflow of the iterative PD algorithm proposed in [31]. Since only the matrix multiplication and addition operations are required, it can be implemented in a highly parallel manner. Algorithm 2 summarizes the proposed PD-based PE-AltMin algorithm. The SVD and matrix multiplication in Algorithm 1 (Lines 2-3) are implemented efficiently by PD in an iterative way in Algorithm 2 (Lines 4-8). The value of β is set to 32/3 for efficient hardware implementation by simulations. Thus, multiplication by $1/\beta$, which is equal to 1/16 + 1/32, can be realized efficiently by shift-and-add operations. It is noted that the output value is not unique. The constraints, such as under the unit modulus of $\mathbf{F}_{RF}$, have been set in the proposed algorithm. The output that meets the constraints is regarded a valid solution.

The simulations are conducted for 64×64 mmWave MIMO systems. The parameters of the channel, including the number of clusters and the number of rays, are the same as the settings in [21]. Under the configuration of 4-to-8 RF chains and 4-to-8 data streams, the PE-AltMin generally converges within 3 to 5 iterations, according to the simulations on spectral efficiency. Fig. 3 shows the performance for phase quantization, when compared to the infinite resolution. When the resolution of phase shifters is 4 bits, the performance degradation is about 0.1dB. Thus, the resolution of the phase shifters is set to 4 bits in this work. Fig. 4 shows the bit error rate (BER) comparison between the SVD-based PE-AltMin algorithm and the OMP algorithm. As can be seen, the PE-AltMin algorithm outperforms the OMP algorithm by over 8 dB at BER $= 10^{-2}$. Fig. 5 shows the spectral efficiency of both the proposed PD-based and the SVD-based PE-AltMin algorithms for 64×64 mmWave MIMO systems under the configurations of $(N_{RF}, N_s) = (4, 4)$, (8, 4) and (8, 8). It can be seen that the proposed PD-based algorithm achieves the same performance as the SVD-based one. The number of iterations for computing PD (N in Algorithm 2) ranges from 5 to 8 under the configurations.

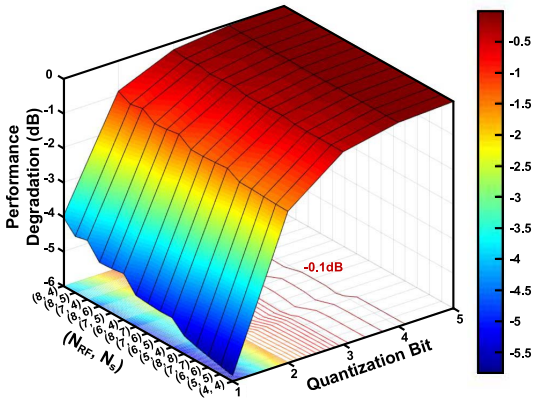

Fig. 3. Performance impact caused by phase quantization for 64 × 64 mmWave MIMO systems.

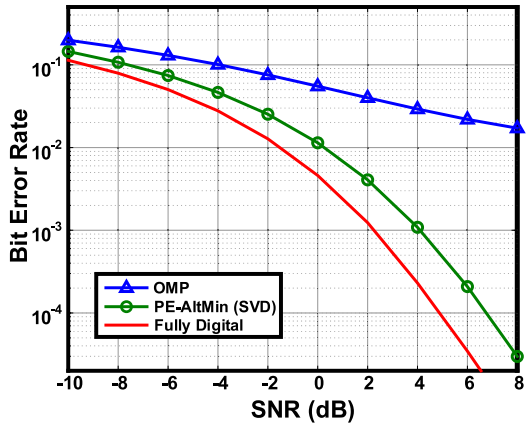

Fig. 4. BER performance of the PE-AltMin and OMP algorithms for 64 × 64 mmWave MIMO systems with $(N_{RF}, N_s) = (4, 4)$ and a phase resolution of 4 bits under 64 QAM.

IV. System Architecture

Fig. 6 shows the system architecture of the proposed hybrid precoding processor. The processor is designed to support 64 antennas and 4-to-8 RF chains and 4-to-8 data streams. It consists of a PD engine, a correlation engine, and a phase extractor. A memory bank is used to store the optimal matrix and the intermediate value of the matrix. A random pattern of $\mathbf{F}_{RF}^{(0)}$ is preloaded as the initial $\mathbf{F}_{RF}$.

A. PD Engine

Fig. 7 shows the proposed PD engine that consists of a PD calculator and a PD buffer. The PD calculator includes a multiply-accumulate (MAC) array, a processing element (PE) array, and a scaling and subtraction unit. To enhance the throughput, the PD engine is designed with a pipelined structure. The PD buffer stores the matrix $\mathbf{X}$ in the previous iteration and in the current iteration. Thanks to the Hermitian property of the Gram matrix $\mathbf{G}$, only the upper triangular part of $\mathbf{G}$ needs to be computed. Two PE1s and two PE2s are deployed for computing $\mathbf{G}$ in a scalable way.

TABLE I
Comparison of SVD and PD Implementations

	TCAS-I'15 [28]	TCAS-I'19 [29]	Proposed PD engine
Bitwidth	15	19	10
Computation Cycles (matrix size: 8×8)	1138	313	133
Gate Count	378k	555k	169k
Normalized Gate Count*	252k	292.1k	169k

*Gate Count × (10/Bitwidth)

Fig. 8 shows computation and data allocation for one iteration in the iterative PD algorithm for a MIMO system with $(N_{RF}, N_s) = (4, 4)$. Two PE1s and two PE2s are configured to compute either two 2 × 2 diagonal sub-matrices or one 2 × 2 off-diagonal sub-matrix. For a 2 × 2 sub-matrix in the diagonal blocks, each PE1 computes two real-valued diagonal elements, while each PE2 computes complex-valued off-diagonal elements. For off-diagonal blocks, all PEs are assigned to compute one of the complex-valued elements of a 2 × 2 sub-matrix. The sub-matrices of $\mathbf{Q}$ are computed from the sub-matrices of the Gram matrix by employing the scaling and subtraction unit. The corresponding multiplications for updating $\mathbf{X}$ are conducted by the MAC array. With the proposed architecture, the hardware complexity for computing the Gram matrix is reduced by 47%.

The proposed PD engine achieve better circuit performance than the design that implements the SVD and the succeeding matrix multiplication with the singular vectors. Although SVD can be realized by using CORDICs with simple shift-and-add operations, direct-mapped implementation also exhibits a long latency due to the nature of highly-iterative computation. To support a high throughput, parallel or pipelined CORDIC architectures are usually applied at the cost of higher hardware complexity. In [28], a systolic array with CORDICs is adopted for performing SVD in a highly parallel manner. In [29], a pipeline CORDIC architecture that connects multiple CORDICs in serial for one iteration is adopted. Additional multiplexers are also needed to support various matrix dimensions, which also introduces extra overhead. Table I shows the comparison of the proposed PD engine and the SVD processors of [28], [29] for 8 × 8 matrices based on synthesis estimates. The PD engine achieves a 2.4-to-8.6× lower latency with 1.5-to-1.7× less normalized gate count, even when the multipliers for the succeeding matrix multiplication that are required for SVD-based implementation are not taken into consideration.

B. Correlation Engine

The correlation engine computes the matrix product of $\mathbf{F}_{RF}$ and $\mathbf{F}_{opt}$ with a scaling unit for PD. In our application, due to the quantized phase of the analog phase shifters, the values of the elements in $\mathbf{F}_{RF}$ are some specified numbers. Thus, multipliers for the matrix multiplication can be implemented by low-complexity constant multipliers. To further simplify the hardware complexity, the distributive property of multiplication is utilized. When the phase differences of $\mathbf{F}_{RF}$ elements are the multiples of 90 degrees, their corresponding

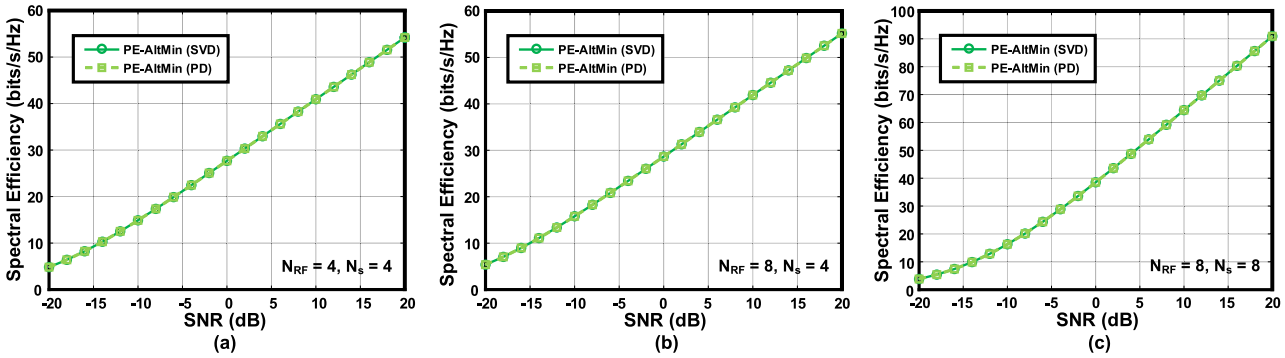

Fig. 5. Spectral efficiency for 64×64 mmWave MIMO systems with $(N_{RF}, N_s) = (4, 4)$, $(8, 4)$, and $(8, 8)$.

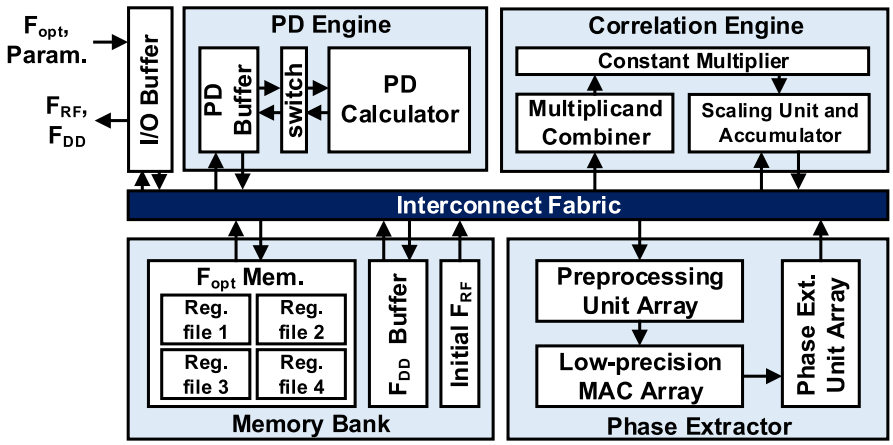

Fig. 6. System architecture of the proposed hybrid precoding processor.

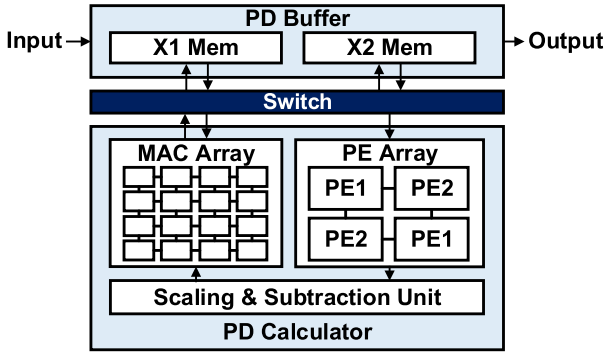

Fig. 7. Architecture of the PD engine.

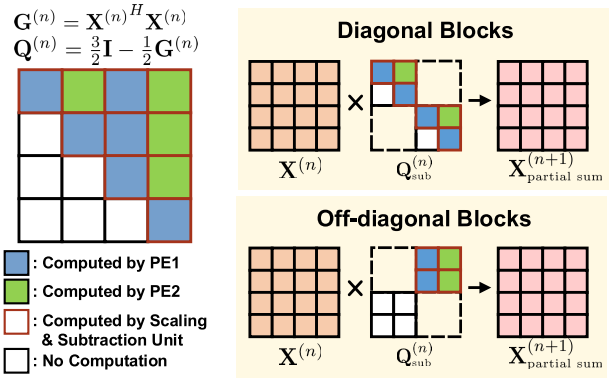

Fig. 8. Computation and data allocation for one iteration in the iterative PD algorithm.

multiplicands can be combined. Fig. 9 shows such an example. The phase difference between Phase 2, Phase 6, Phase 10, and Phase 14 is 90 degrees each, and therefore their corresponding multiplicands can be combined to reduce the number of constant multipliers. By leveraging this property, 55% area is reduced compared to the direct-mapped implementation.

C. Phase Extractor

The phase extractor computes matrix multiplication of $\mathbf{F}_{opt}$ and $\mathbf{F}_{DD}$. It also performs phase extraction to decide the quantized phase for the elements in $\mathbf{F}_{RF}$. Several design techniques are proposed to reduce the hardware complexity.

1) Approximate Phase Extraction: The phase extraction unit performs element-wise quantized phase extraction to update the phase terms of $\mathbf{F}_{RF}$. The phase terms are originally determined by the angles of the complex-valued elements and then quantized by applying exact decision boundaries. The procedure can be simplified by introducing approximate decision boundaries because only specific quantized phases are allowed. Fig. 10 illustrates the approximate scheme. There are 16 Phases in total based on the 4-bit resolution and each Phase covers 22.5° ($360°/2^4$). As an example, Phase 2 covers the

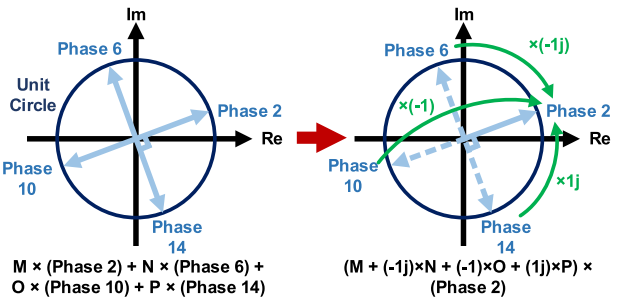

Fig. 9. Illustration of multiplicand combination.

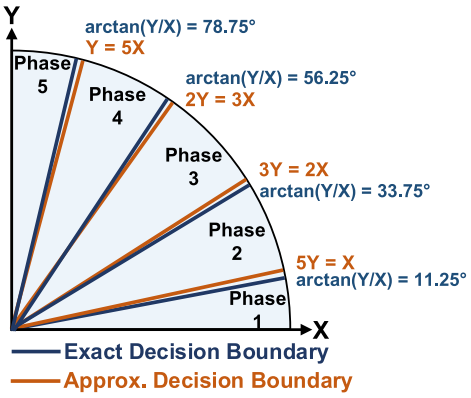

Fig. 10. Approximate scheme for phase extraction.

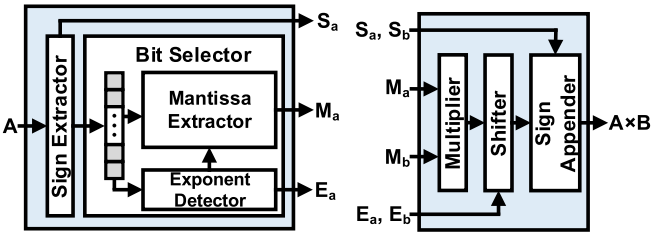

Fig. 11. Proposed low-precision multiplier, in which S, M, and E denote sign, mantissa, and exponent, respectively.

angles between 11.25° and 33.75°. The decision boundary of 11.25° can be approximated by the one of $5Y = X$. Similarly, the decision boundary of 33.75° can be approximated by the one of $3Y = 2X$. The decision boundaries can be implemented by simple shift-and-add operations without computing any arctangent functions. By applying this technique, the area of the phase extraction units is reduced by 43% compared to the design that calculates the exact phases.

2) Low-Precision Matrix Multiplication: Since the matrix multiplication before quantized phase extraction does not need to be computed exactly, matrix multiplication of $\mathbf{F}_{opt}$ and $\mathbf{F}_{DD}{}^{H}$ can be computed in a lower precision to reduce hardware complexity. Direct truncation, however, is infeasible because of the larger dynamic range of the inputs. In this work, floating-point (FLP) arithmetic is adopted to accommodate the dynamic range in a more efficient way. A 10-bit fixed-point (FP) number is converted into a customized FLP representation

TABLE II
CHIP SUMMARY

Technology (nm)	40
Core area (mm^2)	1.54
Supply voltage (V)	0.9
Clock frequency (MHz)	278
No. of Antennas (N_t)	64
Configuration (N_{RF}, N_s)	(4-to-8, 4-to-8)
Throughput (kMat/s)	10,288, for (N_{RF}, N_s) = (4, 4) 6,460, for (N_{RF}, N_s) = (8, 4) 2,089, for (N_{RF}, N_s) = (8, 8)
Power Consumption (mW)	170.9

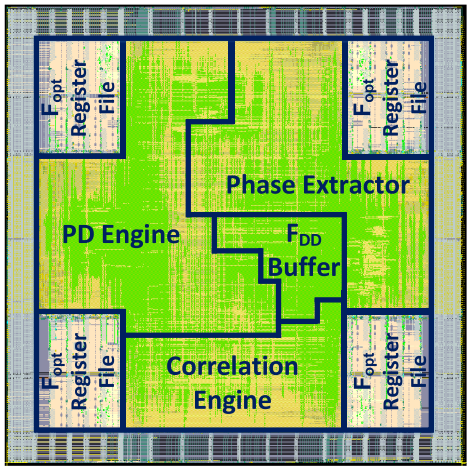

Fig. 12. Layout of the proposed hybrid precoding processor.

that includes 1-bit sign, 5-bit mantissa, and 1-bit exponent. Fig. 11 shows the architecture of the proposed low-precision multiplier. It is noted that the exponent here determines a shift by 3 bits. The multiplication is then conducted in the FLP domain using only 5 bits. After that, the output is converted back to the FP domain with 10 bits. Since the low-precision multiplications are computed with less bits, the hardware complexity of the proposed low-precision multiplier (including the converters between the FP and FLP domains) is reduced by 41% compared to the direct-mapped implementation.

V. EXPERIMENTAL VERIFICATION

The proposed hybrid precoding processor is designed in a 40-nm CMOS technology. Fig. 12 shows the layout of proposed hybrid precoding processor. Table II summarizes the chip performance. The proposed hybrid precoding processor supports any numbers of RF chains (N_{RF}) and data streams (N_s) from 4 to 8, but N_{RF} has to be greater than or equal to N_s. The core area of the chip is 1.54 mm^2 and the power consumption is 170.9 mW at a clock frequency of 278 MHz from a 0.9V supply. It delivers a throughput of 10,288, 6,460, 2,089 kMat/s under the configurations of (N_{RF}, N_s) = (4, 4), (8, 4) and (8, 8), respectively. Fig. 13 shows the fixed-point performance of the proposed hybrid precoding processor. The proposed hybrid precoding processor achieves better spectral efficiency than floating-point OMP implementation by 2 dB under the configuration of (N_{RF}, N_s) = (4, 4). It achieves

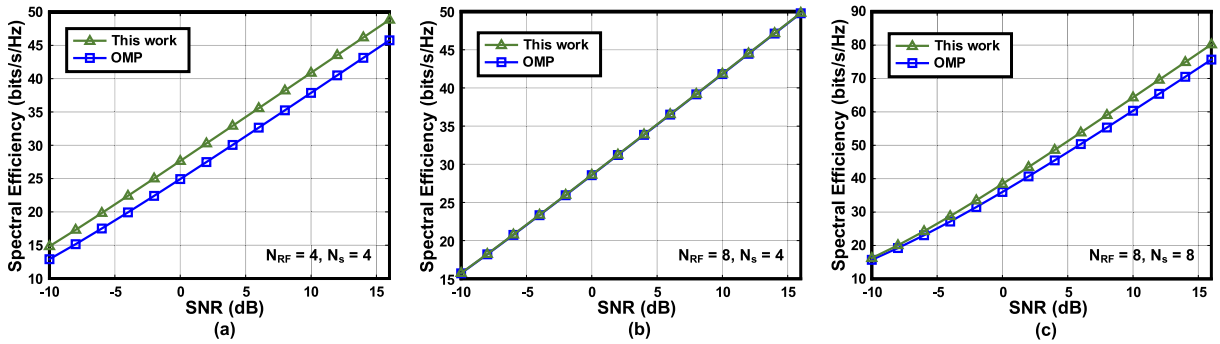

Fig. 13. Spectral efficiency of the proposed hybrid precoding processor for 64 × 64 mmWave MIMO systems with (N_{RF}, N_s) = (4, 4), (8, 4), and (8, 8).

TABLE III
COMPARISON WITH THE STATE-OF-THE-ART HYBRID PRECODING PROCESSORS

	TSP'15 [15]	TCAS-II'19 [17]	Access'19 [18]	This work
Algorithm	PIS-MIB-SOMP	OBMP	OMP	PE-AltMin
No. of antennas N_t	8	8	8	64
No. of RF chains N_{RF}	8	4	4	4-to-8
No. of data streams N_s	1-to-4	1-to-4	4	4-to-8
No. of candidate basis vectors L	9	24	9	Not applicable
Technology (nm)	90	90	40	40
Core area (mm^2)	3.94	1.13	0.58	1.54
Supply voltage (V)	1.0	1.0	0.9	0.9
Clock frequency (MHz)	167	167	333	278
Power consumption (mW)	243.2	30.76	125.1	170.9
Norm. area eff. (kMat/s/mm^2)†,‡	307.2	758.5	364.2	4194.8
Norm. energy (μJ/kMat)†,‡	1017.3	181.7	592.2	26.5

†Technology normalized to 40-nm, system configuration set to $N_t = 64, N_{RF} = 8, N_s = 4$.
‡Complexity of OMP-based designs ([15], [17], [18]) scaled by $(L \times N_t \times N_s + N_t \times N_{RF} \times N_s)$ [18], where $L \propto N_t$ [17].

an up to 1.7 dB improvement in the high-SNR regime for (N_{RF}, N_s) = (8, 8), respectively. The gain of the PE-AltMin algorithm decreases for the case of (N_{RF}, N_s) = (8, 4), as derived in [21].

Table III shows the comparison of the performance with the state-of-the-art OMP-based hybrid precoding processors [15], [17], [18]. Compared to previous works that only support 8 antennas, this work supports 64 antennas. The proposed design also supports more (4-to-8) data streams and flexible (4-to-8) RF chains. This makes this work more flexible for mmWave systems. To make a fair comparison, the area efficiency and normalized energy are normalized to 40-nm and the system configuration is set to $N_t = 64, N_{RF} = 8, N_s = 4$. The hardware complexity (in terms of the number of matrices that need to be processed) of the OMP-based designs is scaled according to the relationships presented by [17] and [18]. This work achieves 5.5-to-13.7× higher normalized area efficiency with 6.9-to-38.4× lower normalized energy than prior art.

VI. CONCLUSION

This work presents a high area-and-energy efficient hybrid precoding processor for 64 × 64 mmWave MIMO systems. It supports 4-to-8 data streams with feasible 4-to-8 RF chains. It is the first processor that implements PE-AltMin precoding algorithm that has better performance than OMP-based counterparts. Phase quantization is also taken into account in this work to reduce the implementation complexity of mmWave MIMO systems. An iterative PD algorithm with proposed PD engine is adopted to enhance the throughput with less gate count compared to similar configuration SVD-based implementations without multipliers for matrix multiplication. By leveraging the characteristic of phase quantization, multiplicands are combined in the correlation engine to reduce the hardware complexity. For the phase extractor, approximate phase extraction and low-precision multiplication are applied to reduce the hardware cost. The proposed hybrid precoding processor dissipates 170.9 mW at a clock frequency of 278 MHz. It is able to support more antennas with a higher flexibility in the number of data streams and RF chains, when compared to the state-of-the-art designs. This work achieves a 5.5-to-13.7× higher normalized area efficiency and 6.9-to-38.4× lower normalized energy, thereby making this work a promising solution for mmWave massive MIMO systems.

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