2021 Fall Computer Architecture

Homework 5

Solution

Grading policy:

1. 2-point deduction for minor mistake.
2. 3- or above-point deduction for major mistake.
3. Full-point deduction for not showing how you derive the answer.

1.

a. Block size = $2^{\#\text{ of offset bits}}$

$2^4 = 16$ (bytes)

b. # of blocks = $2^{\#\text{ of index bits}}$

$2^6 = 64$

c. Total bits = # of set × (valid bit + dirty bit + tag bits + data bits)

$64 \times (1 + 1 + 22 + 16 \times 8) = 9728$ (bits)

d.

Address	Binary Address	Tag	Index	Offset	Hit/Miss
00	0000 0000 0000 0000	0x00	0x00	0x0	Miss
04	0000 0000 0000 0100	0x00	0x00	0x4	Hit
802	0000 1000 0000 0010	0x02	0x00	0x2	Miss
A66	0000 1010 0110 0110	0x02	0x26	0x6	Miss
4CFB	0100 1100 1111 1011	0x13	0x0f	0xb	Miss
A65	0000 1010 0110 0101	0x02	0x26	0x5	Hit
188	0000 0001 1000 1000	0x00	0x18	0x8	Miss
3705	0011 0111 0000 0101	0x0d	0x30	0x5	Miss

For each row in the table:

1-point deduction for wrong Tag, Index, or Offset

2-point deduction for wrong Hit/Miss

Granted points = max(0, 20 - deduction)

2.

> The access time to either the cache or the main memory is the response time which CPU knows that data is ready. So, you must round up the number of cycles it takes to integer. For sub-problems in this problem, 3-point deduction will be imposed for not rounding up, but only imposed once at most.

a. Cycle Time = 0.6 ns
Access time to the main memory = $\left\lceil \frac{70}{0.6} \right\rceil$ = 117 (cycles)
AMAT = L1 Hit time + L1 Miss Rate × L1 Miss Penalty
1 + 0.05 × 117 = 6.85 (cycles)

b. Let the # of total instructions be n, and the # of data access instruction is n'.

$$\text{Total CPI} = \frac{\text{Total \# of Cycles}}{\text{Total \# of Instructions}} = \frac{n \times \text{Base CPI} + n \times (\text{L1 Miss Rate}_{\text{Instruction}} \times \text{L1 Miss Penalty}_{\text{Instruction}}) + n' \times (\text{L1 Miss Rate}_{\text{Data}} \times \text{L1 Miss Penalty}_{\text{Data}})}{n}$$

1.0 + 0.05 × 117 + 0.3 × 0.05 × 117 = 8.605

c. AMAT = L1 Hit Time + L1 Miss Rate × (L2 Hit Time + L2 Miss Rate × L2 Miss Penalty)
L2 Hit Time = $\left\lceil \frac{5}{0.6} \right\rceil$ = 9 (cycles)
1 + 0.05 × (9 + 0.9 × 117) = 6.715 (cycles)

d. Borrow the logic from problem b..
1.0 + 0.05 × (9 + 0.9 × 117) + 0.3 × 0.05 × (9 + 0.9 × 117) = 8.4295

3.

a. # of offset bits = $\log_2 16K$ = 14
# of tag bits = 40 – 14 = 26
# of page table entries = 2^{26}

b. Size of page tables
= # of processes × size of a page table
= 3 × 2^{26} × 4 bytes = 768 MB

c. # of page table entries = 2^{26}
# of entries of a second-level table = 2^{26} / 256 = 2^{18}
Size of a second-level table = 2^{18} × 4 bytes = 1 MB

d. Minimal memory required for the second-level tables
= Minimal # of activated first-level entries × size of the second-level table
= 3 × (256 ÷ 2) × 1 MB = 384 MB