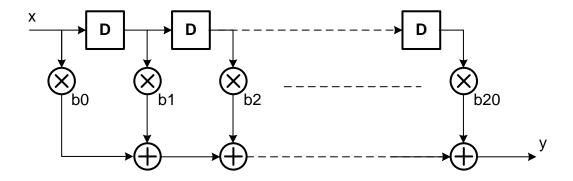
VLSI for DSP 2020 Fall

Project - FIR Filter Design



- 1. Design a 21-tap FIR filter. The coefficients of this filter are listed in Table I.
- 2. Please finish this filter before 2020/11/25, and give a 6-min presentation on the class of 2020/11/25.
- 3. A technique report about this filter is also needed. Please upload the report to E-learning system before 2020/12/02.

Table I Coefficients table

b0	-0.0156	b7	0.0182	b14	-0.0625
b1	0.0182	b8	0.1536	b15	-0.0677
b2	0.0417	b9	0.2813	b16	-0.0208
b3	0.0260	b10	0.3333	b17	0.0260
b4	-0.0208	b11	0.2813	b18	0.0417
b5	-0.0677	b12	0.1536	b19	0.0182
b6	-0.0625	b13	0.0182	b20	-0.0156