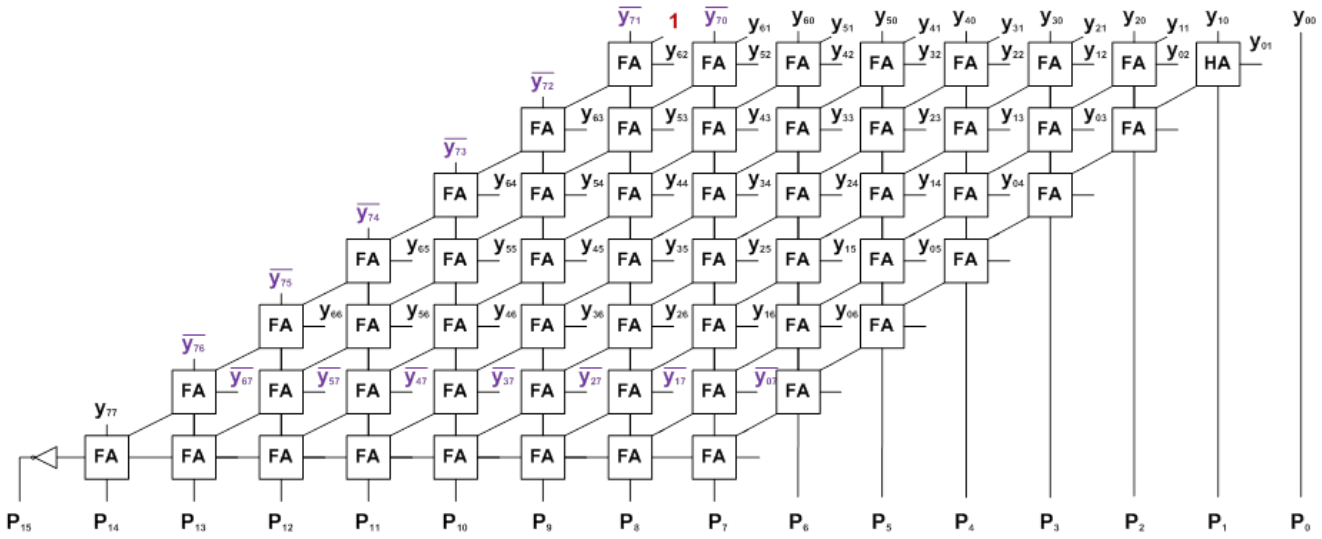
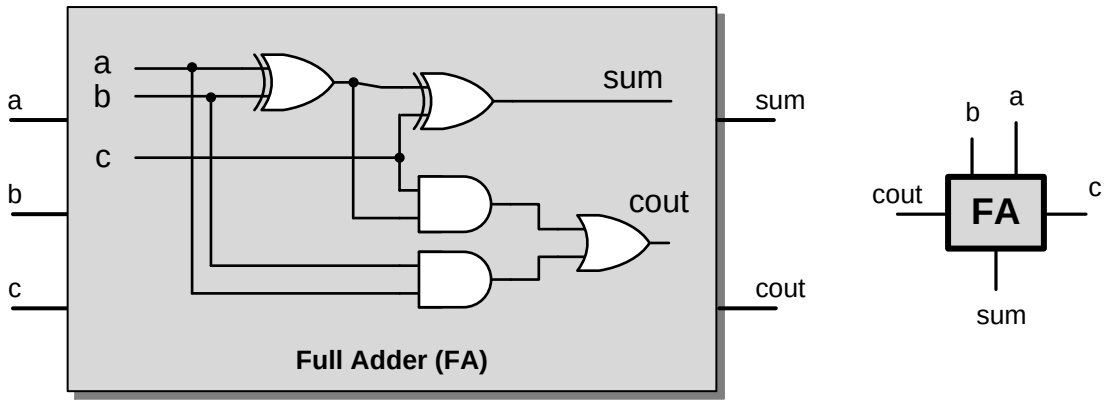
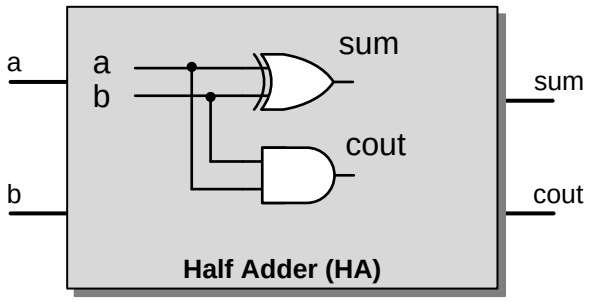
Lab 3 – Multiplier Design

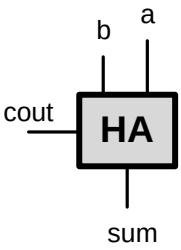


設計一個 8-bit Baugh–Wooley Array Multiplier

1. 其中 FA, HA, P8x8 由下面的架構進行 verilog 設計。







2. 可以利用 TM8x8.v 進行模擬：

TM8x8.v P8x8.v FA.v HA.v