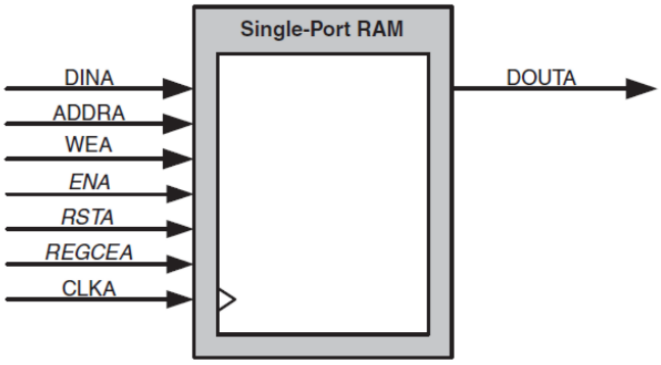
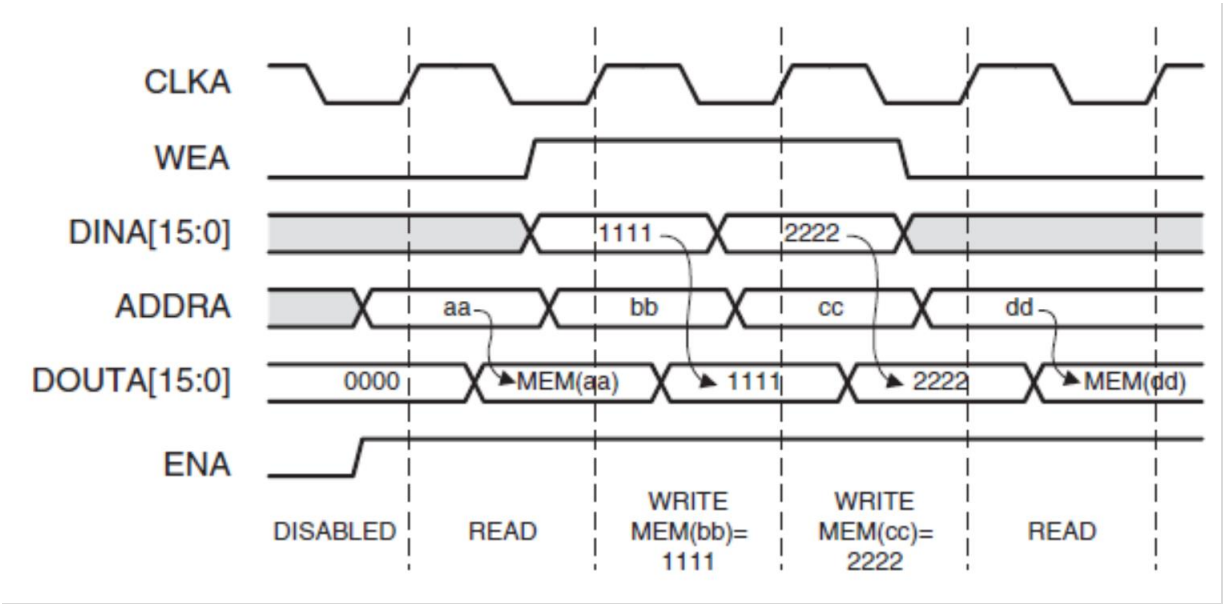
Lab 5 – 65536-word x 16-bit Memory Design

1. 一 65536-word x 16-bit 的 memory。



Name	Direction	Description
clka	Input	**Port A Clock**: Port A operations are synchronous to this clock. For synchronous operation, this must be driven by the same signal as CLKB.
addra	Input	**Port A Address**: Addresses the memory space for port A Read and Write operations. Available in all configurations.
dina	Input	**Port A Data Input**: Data input to be written into the memory through port A. Available in all RAM configurations.
douta	Output	**Port A Data Output**: Data output from Read operations through port A. Available in all configurations except Simple Dual-port RAM.
ena	Input	**Port A Clock Enable**: Enables Read, Write, and reset operations through port A. Optional in all configurations.
wea	Input	**Port A Write Enable**: Enables Write operations through port A. Available in all RAM configurations.
rsta	Input	**Port A Set/Reset**: Resets the Port A memory output latch or output register. Optional in all configurations.
regcea	Input	**Port A Register Enable**: Enables the last output register of port A. Optional in all configurations with port A output registers.

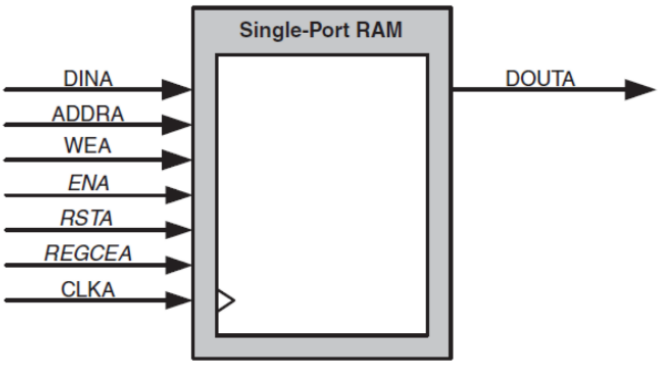
2. 其中 lab5.v 中 mem 的訊號設計如下所示:



Read/Write data control signal

Lab 5B – 256-word x 16-bit Memory Design

1. 一 256-word x 16-bit 的 memory。

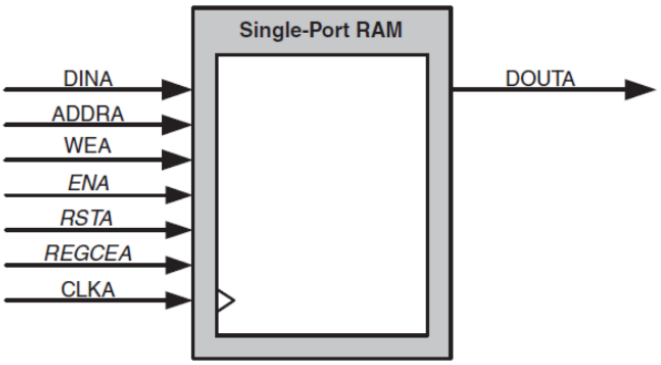


2. rst 完後先將 Mem 中的 data 依序寫入，寫入的內容與 address 相同。
3. 寫入完成後，將 mem 中的資料依序讀出，並將其累加，如下表
4.

addra	Value in mem	douta
0	0	0
1	1	1
2	2	3
3	3	6
4	4	10
5	5	15
6	6	21
255	255	32640

Lab 5C – 256-word x 8-bit Memory Design

1. 一 256-word x 8-bit 的 memory。



2. 利用 mem.coe 檔案初始化記憶體內的值。
3. 依序讀出記憶體內的數值。

addra	douta
0	3A
1	60
2	17
3	A4
4	2F
5	0C
6	BA
255	4A