

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
0	RW	0x0	gpio0c0_pull_dis when 1'b1, disable GPIO0C0 pull up/down when output enable

**PMU2 IOC GPIO0D PDIS**

Address: Operational Base + offset (0x0054)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	gpio0d6_pull_dis when 1'b1, disable GPIO0D6 pull up/down when output enable
5	RW	0x0	gpio0d5_pull_dis when 1'b1, disable GPIO0D5 pull up/down when output enable
4	RW	0x0	gpio0d4_pull_dis when 1'b1, disable GPIO0D4 pull up/down when output enable
3	RW	0x0	gpio0d3_pull_dis when 1'b1, disable GPIO0D3 pull up/down when output enable
2	RW	0x0	gpio0d2_pull_dis when 1'b1, disable GPIO0D2 pull up/down when output enable
1	RW	0x0	gpio0d1_pull_dis when 1'b1, disable GPIO0D1 pull up/down when output enable
0	RW	0x0	gpio0d0_pull_dis when 1'b1, disable GPIO0D0 pull up/down when output enable

**6.27 BUS\_IOC Register Description****6.27.1 Registers Summary**

<b>Name</b>	<b>Offset</b>	<b>Size</b>	<b>Reset Value</b>	<b>Description</b>
<u>BUS_IOC GPIO0B IOMUX SEL_H</u>	0x000C	W	0x00000000	GPIO0B IOMUX Select High bits
<u>BUS_IOC GPIO0C IOMUX SEL_L</u>	0x0010	W	0x00000000	GPIO0C IOMUX Select Low bits
<u>BUS_IOC GPIO0C IOMUX SEL_H</u>	0x0014	W	0x00000000	GPIO0C IOMUX Select High bits
<u>BUS_IOC GPIO0D IOMUX SEL_L</u>	0x0018	W	0x00000000	GPIO0D IOMUX Select Low bits
<u>BUS_IOC GPIO0D IOMUX SEL_H</u>	0x001C	W	0x00000000	GPIO0D IOMUX Select High bits
<u>BUS_IOC GPIO1A IOMUX SEL_L</u>	0x0020	W	0x00000000	GPIO1A IOMUX Select Low bits
<u>BUS_IOC GPIO1A IOMUX SEL_H</u>	0x0024	W	0x00000000	GPIO1A IOMUX Select High bits
<u>BUS_IOC GPIO1B IOMUX SEL_L</u>	0x0028	W	0x00000000	GPIO1B IOMUX Select Low bits
<u>BUS_IOC GPIO1B IOMUX SEL_H</u>	0x002C	W	0x00000000	GPIO1B IOMUX Select High bits
<u>BUS_IOC GPIO1C IOMUX SEL_L</u>	0x0030	W	0x00000000	GPIO1C IOMUX Select Low bits

Name	Offset	Size	Reset Value	Description
BUS IOC GPIO1C IOMUX SEL_H	0x0034	W	0x00000000	GPIO1C IOMUX Select High bits
BUS IOC GPIO1D IOMUX SEL_L	0x0038	W	0x00000000	GPIO1D IOMUX Select Low bits
BUS IOC GPIO1D IOMUX SEL_H	0x003C	W	0x00000000	GPIO1D IOMUX Select High bits
BUS IOC GPIO2A IOMUX SEL_L	0x0040	W	0x00000000	GPIO2A IOMUX Select Low bits
BUS IOC GPIO2A IOMUX SEL_H	0x0044	W	0x00000000	GPIO2A IOMUX Select High bits
BUS IOC GPIO2B IOMUX SEL_L	0x0048	W	0x00000000	GPIO2B IOMUX Select Low bits
BUS IOC GPIO2B IOMUX SEL_H	0x004C	W	0x00000000	GPIO2B IOMUX Select High bits
BUS IOC GPIO2C IOMUX SEL_L	0x0050	W	0x00000000	GPIO2C IOMUX Select Low bits
BUS IOC GPIO2C IOMUX SEL_H	0x0054	W	0x00000000	GPIO2C IOMUX Select High bits
BUS IOC GPIO2D IOMUX SEL_L	0x0058	W	0x00000000	GPIO2D IOMUX Select Low bits
BUS IOC GPIO2D IOMUX SEL_H	0x005C	W	0x00000000	GPIO2D IOMUX Select High bits
BUS IOC GPIO3A IOMUX SEL_L	0x0060	W	0x00000000	GPIO3A IOMUX Select Low bits
BUS IOC GPIO3A IOMUX SEL_H	0x0064	W	0x00000000	GPIO3A IOMUX Select High bits
BUS IOC GPIO3B IOMUX SEL_L	0x0068	W	0x00000000	GPIO3B IOMUX Select Low bits
BUS IOC GPIO3B IOMUX SEL_H	0x006C	W	0x00000000	GPIO3B IOMUX Select High bits
BUS IOC GPIO3C IOMUX SEL_L	0x0070	W	0x00000000	GPIO3C IOMUX Select Low bits
BUS IOC GPIO3C IOMUX SEL_H	0x0074	W	0x00000000	GPIO3C IOMUX Select High bits
BUS IOC GPIO3D IOMUX SEL_L	0x0078	W	0x00000000	GPIO3D IOMUX Select Low bits
BUS IOC GPIO3D IOMUX SEL_H	0x007C	W	0x00000000	GPIO3D IOMUX Select High bits
BUS IOC GPIO4A IOMUX SEL_L	0x0080	W	0x00000000	GPIO4A IOMUX Select Low bits
BUS IOC GPIO4A IOMUX SEL_H	0x0084	W	0x00000000	GPIO4A IOMUX Select High bits
BUS IOC GPIO4B IOMUX SEL_L	0x0088	W	0x00000000	GPIO4B IOMUX Select Low bits
BUS IOC GPIO4B IOMUX SEL_H	0x008C	W	0x00000000	GPIO4B IOMUX Select High bits
BUS IOC GPIO4C IOMUX SEL_L	0x0090	W	0x00000000	GPIO4C IOMUX Select Low bits
BUS IOC GPIO4C IOMUX SEL_H	0x0094	W	0x00000000	GPIO4C IOMUX Select High bits
BUS IOC GPIO4D IOMUX SEL_L	0x0098	W	0x00005500	GPIO4D IOMUX Select Low bits

Name	Offset	Size	Reset Value	Description
BUS IOC GPIO4D IOMUX SEL H	0x009C	W	0x00000000	GPIO4D IOMUX Select High bits

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access

## 6.27.2 Detail Registers Description

### **BUS IOC GPIO0B IOMUX SEL H**

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0b7_sel 4'h8: SPI0_CS1_M0 4'h9: I2C2_SCL_M0 4'hb: CAN0_TX_M0 4'hc: PCIE30X1_1_PERSTN_M0
11:8	RW	0x0	gpio0b6_sel 4'h9: I2C1_SDA_M0 4'ha: UART2_RX_M0 4'hc: PCIE30X1_1_WAKEN_M0
7:4	RW	0x0	gpio0b5_sel 4'h9: I2C1_SCL_M0 4'ha: UART2_TX_M0 4'hc: PCIE30X1_1_CLKREQN_M0
3:0	RO	0x0	reserved

### **BUS IOC GPIO0C IOMUX SEL L**

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x0	gpio0c0_sel 4'h8: SPI0_MOSI_M0 4'h9: I2C2_SDA_M0 4'hb: CAN0_RX_M0 4'hc: PCIE30X1_0_CLKREQN_M0

### **BUS IOC GPIO0C IOMUX SEL H**

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:12	RW	0x0	gpio0c7_sel 4'h8: SPI0_MISO_M0 4'h9: I2C6_SDA_M0 4'ha: UART1_RTSN_M2 4'hb: PWM6_M0 4'hc: PCIE30X4_WAKEN_M0
11:8	RW	0x0	gpio0c6_sel 4'h8: SPI0_CLK_M0 4'hb: PWM5_M1 4'hc: PCIE30X4_CLKREQN_M0 4'hd: SATA_CP POD
7:4	RW	0x0	gpio0c5_sel 4'h9: I2C4_SCL_M2 4'ha: DP1_HPDIN_M1 4'hb: PWM4_M0 4'hc: PCIE30X1_0_PERSTN_M0
3:0	RW	0x0	gpio0c4_sel 4'h9: I2C4_SDA_M2 4'ha: DP0_HPDIN_M1 4'hc: PCIE30X1_0_WAKEN_M0

**BUS IOC GPIOOD\_IOMUX\_SEL\_L**

Address: Operational Base + offset (0x0018)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0d3_sel 4'h8: SPI3_CLK_M2
11:8	RW	0x0	gpio0d2_sel 4'h8: SPI3_MOSI_M2 4'ha: UART1_RX_M2 4'hb: HDMI_RX_SCL_M0 4'hc: PCIE30X2_WAKEN_M0 4'hd: HDMI_TX1_CEC_M1
7:4	RW	0x0	gpio0d1_sel 4'h8: SPI0_CS0_M0 4'ha: UART1_TX_M2 4'hb: HDMI_RX_SDA_M0 4'hc: PCIE30X2_CLKREQN_M0 4'hd: HDMI_TX0_CEC_M1
3:0	RW	0x0	gpio0d0_sel 4'h8: SPI3_MISO_M2 4'h9: I2C6_SCL_M0 4'ha: UART1_CTSN_M2 4'hb: PWM7_IR_M0 4'hc: PCIE30X4_PERSTN_M0

**BUS IOC GPIOOD\_IOMUX\_SEL\_H**

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio0d5_sel 4'h8: SPI3_CS1_M2 4'h9: I2C1_SDA_M2 4'ha: CAN2_TX_M1 4'hb: HDMI_TX0_SCL_M1 4'hd: SATA_MP_SWITCH
3:0	RW	0x0	gpio0d4_sel 4'h8: SPI3_CS0_M2 4'h9: I2C1_SCL_M2 4'ha: CAN2_RX_M1 4'hb: HDMI_TX0_SDA_M1 4'hc: PCIE30X2_PERSTN_M0 4'hd: SATA_CPDET

**BUS IOC GPIO1A IOMUX SEL L**

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1a3_sel 4'h0: GPIO 4'h5: HDMI_TX1_SDA_M2 4'h8: SPI4_CS0_M2 4'h9: I2C4_SCL_M3 4'ha: UART6_CTSN_M1 4'hb: PWM1_M2
11:8	RW	0x0	gpio1a2_sel 4'h0: GPIO 4'h1: VOP_POST_EMPTY 4'h8: SPI4_CLK_M2 4'h9: I2C4_SDA_M3 4'ha: UART6_RTSN_M1 4'hb: PWM0_M2
7:4	RW	0x0	gpio1a1_sel 4'h0: GPIO 4'h4: PCIE30X1_1_WAKEN_M2 4'h5: DP1_HPDIN_M2 4'h6: SATA1_ACT_LED_M1 4'h8: SPI4_MOSI_M2 4'h9: I2C2_SCL_M4 4'ha: UART6_TX_M1

Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio1a0_sel 4'h0: GPIO 4'h4: PCIE30X1_1_CLKREQN_M2 4'h5: DP0_HPDIN_M2 4'h7: HDMI_DEBUG6 4'h8: SPI4_MISO_M2 4'h9: I2C2_SDA_M4 4'ha: UART6_RX_M1

**BUS IOC GPIO1A IOMUX SEL H**

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1a7_sel 4'h0: GPIO 4'h2: PDM1_SDIO_M1 4'h4: PCIE30X1_1_PERSTN_M2 4'h7: HDMI_DEBUG0 4'h8: SPI2_CS0_M0 4'hb: PWM3_IR_M3
11:8	RW	0x0	gpio1a6_sel 4'h0: GPIO 4'h5: HDMI_TX1_HPD_M0 4'h8: SPI2_CLK_M0
7:4	RW	0x0	gpio1a5_sel 4'h0: GPIO 4'h5: HDMI_TX0_HPD_M0 4'h8: SPI2_MOSI_M0
3:0	RW	0x0	gpio1a4_sel 4'h0: GPIO 4'h5: HDMI_TX1_SCL_M2 4'h8: SPI2_MISO_M0

**BUS IOC GPIO1B IOMUX SEL L**

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1b3_sel 4'h0: GPIO 4'h2: PDM1_CLK1_M1 4'h4: PCIE30X1_0_WAKEN_M2 4'h6: SATA0_ACT_LED_M1 4'h7: HDMI_DEBUG4 4'h8: SPI0_CLK_M2 4'ha: UART4_TX_M2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:8	RW	0x0	gpio1b2_sel 4'h0: GPIO 4'h2: PDM1_SDI3_M1 4'h4: PCIE30X4_PERSTN_M3 4'h7: HDMI_DEBUG3 4'h8: SPI0_MOSI_M2 4'ha: UART4_RX_M2
7:4	RW	0x0	gpio1b1_sel 4'h0: GPIO 4'h2: PDM1_SDI2_M1 4'h4: PCIE30X4_WAKEN_M3 4'h7: HDMI_DEBUG2 4'h8: SPI0_MISO_M2
3:0	RW	0x0	gpio1b0_sel 4'h0: GPIO 4'h2: PDM1_SDI1_M1 4'h4: PCIE30X4_CLKREQN_M3 4'h7: HDMI_DEBUG1 4'h8: SPI2_CS1_M0

**BUS IOC GPIO1B IOMUX SEL H**

Address: Operational Base + offset (0x002C)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1b7_sel 4'h0: GPIO 4'h2: MIPI_CAMERA2_CLK_M0 4'h3: SPDIF1_TX_M0 4'h4: PCIE30X2_PERSTN_M3 4'h5: HDMI_RX_CEC_M2 4'h6: SATA2_ACT_LED_M1 4'h9: I2C5_SDA_M3 4'ha: UART1_RX_M1 4'hb: PWM13_M2
11:8	RW	0x0	gpio1b6_sel 4'h0: GPIO 4'h2: MIPI_CAMERA1_CLK_M0 4'h3: SPDIF0_TX_M0 4'h4: PCIE30X2_WAKEN_M3 4'h5: HDMI_RX_HPDOUT_M2 4'h9: I2C5_SCL_M3 4'ha: UART1_TX_M1
7:4	RW	0x0	gpio1b5_sel 4'h0: GPIO 4'h4: PCIE30X1_0_CLKREQN_M2 4'h8: SPI0_CS1_M2 4'ha: UART7_TX_M2

Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio1b4_sel 4'h0: GPIO 4'h2: PDM1_CLK0_M1 4'h4: PCIE30X1_0_PERSTN_M2 4'h7: HDMI_DEBUG5 4'h8: SPI0_CS0_M2 4'ha: UART7_RX_M2

**BUS IOC GPIO1C IOMUX SEL L**

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1c3_sel 4'h0: GPIO 4'h1: I2S0_SCLK 4'h8: SPI4_CS0_M0 4'h9: I2C6_SCL_M1 4'ha: UART3_CTSN 4'hb: PWM7_IR_M2
11:8	RW	0x0	gpio1c2_sel 4'h0: GPIO 4'h1: I2S0_MCLK 4'h8: SPI4_CLK_M0 4'h9: I2C6_SDA_M1 4'ha: UART3_RTSN 4'hb: PWM3_IR_M2
7:4	RW	0x0	gpio1c1_sel 4'h0: GPIO 4'h8: SPI4_MOSI_M0 4'h9: I2C3_SCL_M0 4'ha: UART3_TX_M0
3:0	RW	0x0	gpio1c0_sel 4'h0: GPIO 4'h8: SPI4_MISO_M0 4'h9: I2C3_SDA_M0 4'ha: UART3_RX_M0

**BUS IOC GPIO1C IOMUX SEL H**

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1c7_sel 4'h0: GPIO 4'h1: I2S0_SDO0 4'h9: I2C4_SCL_M4 4'ha: UART4_CTSN

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:8	RW	0x0	gpio1c6_sel 4'h0: GPIO 4'h3: PDM0_CLK0_M0 4'h9: I2C4_SDA_M4 4'hb: PWM15_IR_M2
7:4	RW	0x0	gpio1c5_sel 4'h0: GPIO 4'h1: I2S0_LRCK 4'h9: I2C2_SCL_M3 4'ha: UART4_RTSN
3:0	RW	0x0	gpio1c4_sel 4'h0: GPIO 4'h3: PDM0_CLK1_M0 4'h4: PCIE30PHY_DTB0 4'h8: SPI4_CS1_M0 4'h9: I2C2_SDA_M3 4'hb: PWM11_IR_M2

**BUS IOC GPIO1D\_IOMUX\_SEL\_L**

Address: Operational Base + offset (0x0038)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1d3_sel 4'h0: GPIO 4'h2: I2S0_SDI1 4'h3: PDM0_SDI3_M0 4'h8: SPI1_CS0_M2 4'h9: I2C1_SDA_M4 4'ha: UART4_RX_M0 4'hb: PWM1_M1
11:8	RW	0x0	gpio1d2_sel 4'h0: GPIO 4'h1: I2S0_SDO3 4'h2: I2S0_SDI2 4'h3: PDM0_SDI2_M0 4'h8: SPI1_CLK_M2 4'h9: I2C1_SCL_M4 4'ha: UART4_TX_M0 4'hb: PWM0_M1
7:4	RW	0x0	gpio1d1_sel 4'h0: GPIO 4'h1: I2S0_SDO2 4'h2: I2S0_SDI3 4'h3: PDM0_SDI1_M0 4'h4: PCIE30PHY_DTB1 4'h8: SPI1_MOSI_M2 4'h9: I2C7_SDA_M0 4'ha: UART6_RX_M2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3:0	RW	0x0	gpio1d0_sel 4'h0: GPIO 4'h1: I2S0_SDO1 4'h8: SPI1_MISO_M2 4'h9: I2C7_SCL_M0 4'ha: UART6_TX_M2

**BUS IOC GPIO1D IOMUX SEL H**

Address: Operational Base + offset (0x003C)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1d7_sel 4'h0: GPIO 4'h2: MIPI_CAMERA4_CLK_M0 4'h4: PCIE30X2_CLKREQN_M3 4'h5: HDMI_RX_SDA_M2 4'h9: I2C8_SDA_M2 4'ha: UART1_CTSN_M1 4'hb: PWM15_IR_M3
11:8	RW	0x0	gpio1d6_sel 4'h0: GPIO 4'h2: MIPI_CAMERA3_CLK_M0 4'h5: HDMI_RX_SCL_M2 4'h9: I2C8_SCL_M2 4'ha: UART1_RTSN_M1 4'hb: PWM14_M2
7:4	RW	0x0	gpio1d5_sel 4'h0: GPIO 4'h3: PDM0_SDIO0_M0 4'h8: SPI1_CS1_M2
3:0	RW	0x0	gpio1d4_sel 4'h0: GPIO 4'h2: I2S0_SDIO

**BUS IOC GPIO2A IOMUX SEL L**

Address: Operational Base + offset (0x0040)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2a3_sel 4'h0: GPIO 4'h1: EMMC_RSTN 4'h9: I2C2_SCL_M2 4'ha: UART5_RTSN_M1
11:8	RW	0x0	gpio2a2_sel 4'h0: GPIO 4'h1: EMMC_DATA_STROBE 4'h9: I2C2_SDA_M2 4'ha: UART5_CTSN_M1

Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio2a1_sel 4'h0: GPIO 4'h1: EMMC_CLKOUT
3:0	RW	0x0	gpio2a0_sel 4'h0: GPIO 4'h1: EMMC_CMD 4'h2: FSPI_CLK_M0

**BUS IOC GPIO2A IOMUX SEL H**

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2a7_sel 4'h0: GPIO 4'h1: GMAC0_RXD3 4'h2: SDIO_D1_M0 4'h3: FSPI_D1_M1 4'ha: UART6_TX_M0
11:8	RW	0x0	gpio2a6_sel 4'h0: GPIO 4'h1: GMAC0_RXD2 4'h2: SDIO_D0_M0 4'h3: FSPI_D0_M1 4'ha: UART6_RX_M0
7:0	RO	0x00	reserved

**BUS IOC GPIO2B IOMUX SEL L**

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2b3_sel 4'h0: GPIO 4'h1: GMAC0_TXCLK 4'h2: SDIO_CLK_M0 4'h3: FSPI_CLK_M1 4'h9: I2C3_SDA_M3
11:8	RW	0x0	gpio2b2_sel 4'h0: GPIO 4'h1: GMAC0_TXD3 4'h2: SDIO_CMD_M0 4'h9: I2C3_SCL_M3
7:4	RW	0x0	gpio2b1_sel 4'h0: GPIO 4'h1: GMAC0_TXD2 4'h2: SDIO_D3_M0 4'h3: FSPI_D3_M1 4'h9: I2C8_SDA_M1 4'ha: UART6_CTSN_M0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3:0	RW	0x0	gpio2b0_sel 4'h0: GPIO 4'h1: GMAC0_RXCLK 4'h2: SDIO_D2_M0 4'h3: FSPI_D2_M1 4'h9: I2C8_SCL_M1 4'ha: UART6_RTSN_M0

**BUS IOC GPIO2B IOMUX SEL H**

Address: Operational Base + offset (0x004C)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2b7_sel 4'h0: GPIO 4'h1: GMAC0_TXD1 4'h2: I2S2_SCLK_M0 4'h9: I2C5_SDA_M4 4'ha: UART1_TX_M0
11:8	RW	0x0	gpio2b6_sel 4'h0: GPIO 4'h1: GMAC0_TXD0 4'h2: I2S2_MCLK_M0 4'h9: I2C5_SCL_M4 4'ha: UART1_RX_M0
7:4	RW	0x0	gpio2b5_sel 4'h0: GPIO 4'h1: GMAC0_PPSTRING 4'h3: FSPI_CS1N_M1 4'h4: HDMI_TX1_SCL_M0 4'h9: I2C4_SCL_M1 4'ha: UART7_TX_M0
3:0	RW	0x0	gpio2b4_sel 4'h0: GPIO 4'h1: GMAC0_PTP_REFCLK 4'h3: FSPI_CS0N_M1 4'h4: HDMI_TX1_SDA_M0 4'h9: I2C4_SDA_M1 4'ha: UART7_RX_M0

**BUS IOC GPIO2C IOMUX SEL L**

Address: Operational Base + offset (0x0050)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2c3_sel 4'h0: GPIO 4'h1: ETH0_REFCLKO_25M 4'h2: I2S2_SDI_M0 4'h8: SPI1_CS0_M0 4'h9: I2C6_SCL_M2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:8	RW	0x0	gpio2c2_sel 4'h0: GPIO 4'h1: GMAC0_RXD1 4'h8: SPI1_MOSI_M0 4'h9: I2C6_SDA_M2 4'ha: UART9_TX_M0
7:4	RW	0x0	gpio2c1_sel 4'h0: GPIO 4'h1: GMAC0_RXD0 4'h8: SPI1_MISO_M0 4'h9: I2C2_SCL_M1 4'ha: UART1_CTSN_M0
3:0	RW	0x0	gpio2c0_sel 4'h0: GPIO 4'h1: GMAC0_TXEN 4'h2: I2S2_LRCK_M0 4'h8: SPI1_CLK_M0 4'h9: I2C2_SDA_M1 4'ha: UART1_RTSN_M0

**BUS IOC GPIO2C IOMUX SEL H**

Address: Operational Base + offset (0x0054)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio2c5_sel 4'h0: GPIO 4'h1: CLK32K_OUT1
3:0	RW	0x0	gpio2c4_sel 4'h0: GPIO 4'h1: GMAC0_PPSCLK 4'h3: TEST_CLKOUT_M1 4'h4: HDMI_TX1_CEC_M0 4'h8: SPI1_CS1_M0 4'ha: UART9_RX_M0

**BUS IOC GPIO2D IOMUX SEL L**

Address: Operational Base + offset (0x0058)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2d3_sel 4'h0: GPIO 4'h1: EMMC_D3 4'h2: FSPI_D3_M0
11:8	RW	0x0	gpio2d2_sel 4'h0: GPIO 4'h1: EMMC_D2 4'h2: FSPI_D2_M0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:4	RW	0x0	gpio2d1_sel 4'h0: GPIO 4'h1: EMMC_D1 4'h2: FSPI_D1_M0
3:0	RW	0x0	gpio2d0_sel 4'h0: GPIO 4'h1: EMMC_D0 4'h2: FSPI_D0_M0

**BUS IOC GPIO2D IOMUX SEL H**

Address: Operational Base + offset (0x005C)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio2d7_sel 4'h0: GPIO 4'h1: EMMC_D7 4'h2: FSPI_CS1N_M0
11:8	RW	0x0	gpio2d6_sel 4'h0: GPIO 4'h1: EMMC_D6 4'h2: FSPI_CS0N_M0
7:4	RW	0x0	gpio2d5_sel 4'h0: GPIO 4'h1: EMMC_D5 4'h9: I2C1_SDA_M3 4'ha: UART5_TX_M2
3:0	RW	0x0	gpio2d4_sel 4'h0: GPIO 4'h1: EMMC_D4 4'h9: I2C1_SCL_M3 4'ha: UART5_RX_M2

**BUS IOC GPIO3A IOMUX SEL L**

Address: Operational Base + offset (0x0060)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3a3_sel 4'h0: GPIO 4'h1: GMAC1_RXD3 4'h2: SDIO_D3_M1 4'h3: I2S3_SDO 4'h4: AUDDSM_RN 4'h5: FSPI_D3_M2 4'h8: SPI4_CS0_M1 4'ha: UART8_RX_M1

Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio3a2_sel 4'h0: GPIO 4'h1: GMAC1_RXD2 4'h2: SDIO_D2_M1 4'h3: I2S3_LRCK 4'h4: AUDDSM_LP 4'h5: FSPI_D2_M2 4'h8: SPI4_CLK_M1 4'ha: UART8_TX_M1
7:4	RW	0x0	gpio3a1_sel 4'h0: GPIO 4'h1: GMAC1_TXD3 4'h2: SDIO_D1_M1 4'h3: I2S3_SCLK 4'h4: AUDDSM_LN 4'h5: FSPI_D1_M2 4'h8: SPI4_MOSI_M1 4'h9: I2C6_SCL_M4 4'hb: PWM11_IR_M0
3:0	RW	0x0	gpio3a0_sel 4'h0: GPIO 4'h1: GMAC1_TXD2 4'h2: SDIO_D0_M1 4'h3: I2S3_MCLK 4'h5: FSPI_D0_M2 4'h8: SPI4_MISO_M1 4'h9: I2C6_SDA_M4 4'hb: PWM10_M0

**BUS IOC GPIO3A\_IOMUX\_SEL\_H**

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3a7_sel 4'h0: GPIO 4'h1: GMAC1_RXD0 4'h4: MIPI_CAMERA2_CLK_M1 4'hb: PWM8_M0
11:8	RW	0x0	gpio3a6_sel 4'h0: GPIO 4'h1: ETH1_REFCLKO_25M 4'h4: MIPI_CAMERA1_CLK_M1 4'h9: I2C4_SCL_M0
7:4	RW	0x0	gpio3a5_sel 4'h0: GPIO 4'h1: GMAC1_RXCLK 4'h2: SDIO_CLK_M1 4'h4: MIPI_CAMERA0_CLK_M1 4'h5: FSPI_CLK_M2 4'h9: I2C4_SDA_M0 4'ha: UART8_CTSN_M1

Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio3a4_sel 4'h0: GPIO 4'h1: GMAC1_TXCLK 4'h2: SDIO_CMD_M1 4'h3: I2S3_SDI 4'h4: AUDDSM_RP 4'h8: SPI4_CS1_M1 4'ha: UART8_RTSN_M1

**BUS IOC GPIO3B IOMUX SEL L**

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3b3_sel 4'h0: GPIO 4'h1: GMAC1_TXDO 4'h3: I2S2_SDO_M1 4'ha: UART2_RTSN
11:8	RW	0x0	gpio3b2_sel 4'h0: GPIO 4'h1: GMAC1_TXER 4'h3: I2S2_SDI_M1 4'ha: UART2_RX_M2 4'hb: PWM3_IR_M1
7:4	RW	0x0	gpio3b1_sel 4'h0: GPIO 4'h1: GMAC1_RXDV_CRS 4'h4: MIPI_CAMERA4_CLK_M1 4'ha: UART2_TX_M2 4'hb: PWM2_M1
3:0	RW	0x0	gpio3b0_sel 4'h0: GPIO 4'h1: GMAC1_RXD1 4'h4: MIPI_CAMERA3_CLK_M1 4'hb: PWM9_M0

**BUS IOC GPIO3B IOMUX SEL H**

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3b7_sel 4'h0: GPIO 4'h1: GMAC1_PTP_REF_CLK 4'h5: HDMI_TX1_HPD_M1 4'h8: SPI1_MOSI_M1 4'ha: I2C3_SCL_M1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:8	RW	0x0	gpio3b6_sel 4'h0: GPIO 4'h1: GMAC1_MCLKINOUT 4'h3: I2S2_LRCK_M1 4'h9: CAN1_TX_M0 4'ha: UART3_RX_M1 4'hb: PWM13_M0
7:4	RW	0x0	gpio3b5_sel 4'h0: GPIO 4'h1: GMAC1_TXEN 4'h3: I2S2_SCLK_M1 4'h9: CAN1_RX_M0 4'ha: UART3_TX_M1 4'hb: PWM12_M0
3:0	RW	0x0	gpio3b4_sel 4'h0: GPIO 4'h1: GMAC1_TXD1 4'h3: I2S2_MCLK_M1 4'ha: UART2_CTSN

**BUS IOC GPIO3C IOMUX SEL L**

Address: Operational Base + offset (0x0070)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3c3_sel 4'h0: GPIO 4'h1: GMAC1_MDIO 4'h2: MIPI_TE1 4'h8: SPI1_CS1_M1 4'h9: I2C8_SDA_M4 4'ha: UART7_CTSN_M1 4'hb: PWM15_IR_M0
11:8	RW	0x0	gpio3c2_sel 4'h0: GPIO 4'h1: GMAC1_MDC 4'h2: MIPI_TE0 4'h8: SPI1_CS0_M1 4'h9: I2C8_SCL_M4 4'ha: UART7_RTSN_M1 4'hb: PWM14_M0
7:4	RW	0x0	gpio3c1_sel 4'h0: GPIO 4'h1: GMAC1_PPSCLK 4'h4: PCIE30X2_BUTTON_RSTN 4'h8: SPI1_CLK_M1 4'ha: UART7_RX_M1
3:0	RW	0x0	gpio3c0_sel 4'h0: GPIO 4'h1: GMAC1_PPSTRIG 4'h8: SPI1_MISO_M1 4'h9: I2C3_SDA_M1 4'ha: UART7_TX_M1

**BUS IOC GPIO3C IOMUX SEL H**

Address: Operational Base + offset (0x0074)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3c7_sel 4'h0: GPIO 4'h1: CIF_D11 4'h4: PCIE20X1_2_CLKREQN_M0 4'h5: HDMI_TX0_SCL_M2 4'h8: SPI3_MOSI_M3 4'h9: I2C5_SCL_M0
11:8	RW	0x0	gpio3c6_sel 4'h0: GPIO 4'h1: CIF_D10 4'h4: PCIE30X4_PERSTN_M2 4'h5: HDMI_TX1_SCL_M1 4'h8: SPI3_MISO_M3
7:4	RW	0x0	gpio3c5_sel 4'h0: GPIO 4'h1: CIF_D9 4'h2: FSPI_CS1N_M2 4'h4: PCIE30X4_WAKEN_M2 4'h5: HDMI_TX1_SDA_M1 4'h8: SPI3_CS1_M3 4'h9: CAN2_TX_M0 4'ha: UART5_RX_M1
3:0	RW	0x0	gpio3c4_sel 4'h0: GPIO 4'h1: CIF_D8 4'h2: FSPI_CS0N_M2 4'h4: PCIE30X4_CLKREQN_M2 4'h5: HDMI_TX1_CEC_M2 4'h8: SPI3_CS0_M3 4'h9: CAN2_RX_M0 4'ha: UART5_TX_M1

**BUS IOC GPIO3D IOMUX SEL L**

Address: Operational Base + offset (0x0078)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3d3_sel 4'h0: GPIO 4'h1: CIF_D15 4'h4: PCIE30X2_WAKEN_M2 4'h5: HDMI_RX_SDA_M1 4'h8: SPI0_CLK_M3 4'h9: I2C7_SDA_M2 4'ha: UART9_CTSN_M2 4'hb: PWM10_M2

Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio3d2_sel 4'h0: GPIO 4'h1: CIF_D14 4'h4: PCIE30X2_CLKREQN_M2 4'h5: HDMI_RX_SCL_M1 4'h8: SPI0_MOSI_M3 4'h9: I2C7_SCL_M2 4'ha: UART9_RTSN_M2
7:4	RW	0x0	gpio3d1_sel 4'h0: GPIO 4'h1: CIF_D13 4'h4: PCIE20X1_2_PERSTN_M0 4'h5: HDMI_RX_CEC_M1 4'h8: SPI0_MISO_M3 4'ha: UART4_TX_M1 4'hb: PWM9_M2
3:0	RW	0x0	gpio3d0_sel 4'h0: GPIO 4'h1: CIF_D12 4'h4: PCIE20X1_2_WAKEN_M0 4'h5: HDMI_TX0_SDA_M2 4'h8: SPI3_CLK_M3 4'h9: I2C5_SDA_M0 4'ha: UART4_RX_M1 4'hb: PWM8_M2

**BUS IOC GPIO3D IOMUX SEL H**

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio3d5_sel 4'h0: GPIO 4'h4: PCIE30X4_BUTTON_RSTN 4'h5: DP1_HPDIN_M0 4'h6: MCU_JTAG_TMS_M1 4'h8: SPI0_CS1_M3 4'ha: UART9_TX_M2 4'hb: PWM11_IR_M3
3:0	RW	0x0	gpio3d4_sel 4'h0: GPIO 4'h3: HDMI_TX0_HPD_M1 4'h4: PCIE30X2_PERSTN_M2 4'h5: HDMI_RX_HPDOUT_M1 4'h6: MCU_JTAG_TCK_M1 4'h8: SPI0_CS0_M3 4'ha: UART9_RX_M2

**BUS IOC GPIO4A IOMUX SEL L**

Address: Operational Base + offset (0x0080)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4a3_sel 4'h0: GPIO 4'h1: CIF_D3 4'h2: BT1120_D3 4'h4: PCIE30X1_0_CLKREQN_M1 4'h7: DDRPHYCH0_DTB3 4'ha: UART0_TX_M2
11:8	RW	0x0	gpio4a2_sel 4'h0: GPIO 4'h1: CIF_D2 4'h2: BT1120_D2 4'h3: I2S1_LRCK_M0 4'h4: PCIE30X1_1_PERSTN_M1 4'h7: DDRPHYCH0_DTB2 4'h8: SPI0_CLK_M1
7:4	RW	0x0	gpio4a1_sel 4'h0: GPIO 4'h1: CIF_D1 4'h2: BT1120_D1 4'h3: I2S1_SCLK_M0 4'h4: PCIE30X1_1_WAKEN_M1 4'h7: DDRPHYCH0_DTB1 4'h8: SPI0_MOSI_M1 4'ha: UART9_CTSN_M1
3:0	RW	0x0	gpio4a0_sel 4'h0: GPIO 4'h1: CIF_D0 4'h2: BT1120_D0 4'h3: I2S1_MCLK_M0 4'h4: PCIE30X1_1_CLKREQN_M1 4'h7: DDRPHYCH0_DTB0 4'h8: SPI0_MISO_M1 4'ha: UART9_RTSN_M1

**BUS IOC GPIO4A IOMUX SEL H**

Address: Operational Base + offset (0x0084)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4a7_sel 4'h0: GPIO 4'h1: CIF_D7 4'h2: BT1120_D7 4'h3: I2S1_SDI2_M0 4'h4: PCIE30X2_WAKEN_M1 4'h7: DDRPHYCH1_DTB3 4'h8: SPI2_CS0_M1 4'h9: I2C5_SDA_M2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:8	RW	0x0	gpio4a6_sel 4'h0: GPIO 4'h1: CIF_D6 4'h2: BT1120_D6 4'h3: I2S1_SDI1_M0 4'h4: PCIE30X2_CLKREQN_M1 4'h7: DDRPHYCH1_DTB2 4'h8: SPI2_CLK_M1 4'h9: I2C5_SCL_M2 4'ha: UART3_RX_M2
7:4	RW	0x0	gpio4a5_sel 4'h0: GPIO 4'h1: CIF_D5 4'h2: BT1120_D5 4'h3: I2S1_SDI0_M0 4'h4: PCIE30X1_0_PERSTN_M1 4'h7: DDRPHYCH1_DTB1 4'h8: SPI2_MOSI_M1 4'h9: I2C3_SDA_M2 4'ha: UART3_TX_M2
3:0	RW	0x0	gpio4a4_sel 4'h0: GPIO 4'h1: CIF_D4 4'h2: BT1120_D4 4'h4: PCIE30X1_0_WAKEN_M1 4'h7: DDRPHYCH1_DTB0 4'h8: SPI2_MISO_M1 4'h9: I2C3_SCL_M2 4'ha: UART0_RX_M2

**BUS IOC GPIO4B IOMUX SEL\_L**

Address: Operational Base + offset (0x0088)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4b3_sel 4'h0: GPIO 4'h1: CIF_VSYNC 4'h2: BT1120_D9 4'h3: I2S1_SDO2_M0 4'h4: PCIE20X1_2_BUTTON_RSTN 4'h7: DDRPHYCH2_DTB3 4'h9: I2C7_SDA_M3 4'ha: UART8_CTSN_M0 4'hb: PWM15_IR_M1 4'hc: CAN1_TX_M1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:8	RW	0x0	gpio4b2_sel 4'h0: GPIO 4'h1: CIF_HREF 4'h2: BT1120_D8 4'h3: I2S1_SDO1_M0 4'h4: PCIE30X1_1_BUTTON_RSTN 4'h7: DDRPHYCH2_DTB2 4'h8: SPI0_CS0_M1 4'h9: I2C7_SCL_M3 4'ha: UART8_RTSN_M0 4'hb: PWM14_M1 4'hc: CAN1_RX_M1
7:4	RW	0x0	gpio4b1_sel 4'h0: GPIO 4'h1: MIPI_CAMERA0_CLK_M0 4'h2: SPDIF1_TX_M1 4'h3: I2S1_SDO0_M0 4'h4: PCIE30X1_0_BUTTON_RSTN 4'h6: SATA2_ACT_LED_M0 4'h7: DDRPHYCH2_DTB1 4'h8: SPI0_CS1_M1 4'h9: I2C6_SCL_M3 4'ha: UART8_RX_M0
3:0	RW	0x0	gpio4b0_sel 4'h0: GPIO 4'h1: CIF_CLKIN 4'h2: BT1120_CLKOUT 4'h3: I2S1_SDI3_M0 4'h4: PCIE30X2_PERSTN_M1 4'h7: DDRPHYCH2_DTB0 4'h8: SPI2_CS1_M1 4'h9: I2C6_SDA_M3 4'ha: UART8_TX_M0

**BUS IOC GPIO4B IOMUX SEL H**

Address: Operational Base + offset (0x008C)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4b7_sel 4'h0: GPIO 4'h2: BT1120_D13 4'h4: PCIE20X1_2_CLKREQN_M1 4'h5: HDMI_TX0_SCL_M0 4'h7: DDRPHYCH3_DTB3 4'h8: SPI3_CLK_M1 4'h9: I2C5_SDA_M1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:8	RW	0x0	gpio4b6_sel 4'h0: GPIO 4'h2: BT1120_D12 4'h4: PCIE30X4_PERSTN_M1 4'h5: HDMI_RX_HPDOUT_M0 4'h6: SATA0_ACT_LED_M0 4'h7: DDRPHYCH3_DTB2 4'h8: SPI3_MOSI_M1 4'h9: I2C5_SCL_M1 4'hb: PWM13_M1
7:4	RW	0x0	gpio4b5_sel 4'h0: GPIO 4'h2: BT1120_D11 4'h4: PCIE30X4_WAKEN_M1 4'h5: HDMI_RX_CEC_M0 4'h6: SATA1_ACT_LED_M0 4'h7: DDRPHYCH3_DTB1 4'h8: SPI3_MISO_M1 4'ha: UART9_RX_M1 4'hb: PWM12_M1
3:0	RW	0x0	gpio4b4_sel 4'h0: GPIO 4'h1: CIF_CLKOUT 4'h2: BT1120_D10 4'h3: I2S1_SDO3_M0 4'h4: PCIE30X4_CLKREQN_M1 4'h5: DP0_HPDIN_M0 4'h6: SPDIF0_TX_M1 4'h7: DDRPHYCH3_DTB0 4'ha: UART9_TX_M1 4'hb: PWM11_IR_M1

**BUS IOC GPIO4C IOMUX SEL\_L**

Address: Operational Base + offset (0x0090)

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4c3_sel 4'h0: GPIO 4'h1: GMAC0_MCLKINOUT 4'h2: I2S2_SDO_M0 4'h8: SPI3_CS1_M0 4'ha: I2C7_SCL_M1 4'hb: PWM4_M1
11:8	RW	0x0	gpio4c2_sel 4'h0: GPIO 4'h1: GMAC0_RXDV CRS 4'h8: SPI3_CS0_M0 4'ha: UART7_RTSN_M0 4'hb: PWM2_M2

Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio4c1_sel 4'h0: GPIO 4'h2: BT1120_D15 4'h3: SPDIF1_TX_M2 4'h4: PCIE20X1_2_PERSTN_M1 4'h5: HDMI_TX0_CEC_M0 4'h8: SPI3_CS1_M1 4'h9: I2C8_SDA_M3 4'hb: PWM6_M1
3:0	RW	0x0	gpio4c0_sel 4'h0: GPIO 4'h2: BT1120_D14 4'h4: PCIE20X1_2_WAKEN_M1 4'h5: HDMI_TX0_SDA_M0 4'h8: SPI3_CS0_M1 4'h9: I2C8_SCL_M3

**BUS IOC GPIO4C IOMUX SEL H**

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x0	gpio4c6_sel 4'h0: GPIO 4'h1: GMAC0_TXER 4'h8: SPI3_CLK_M0 4'h9: I2C0_SDA_M1 4'ha: UART7_CTSN_M0 4'hb: PWM7_IR_M3
7:4	RW	0x0	gpio4c5_sel 4'h0: GPIO 4'h1: GMAC0_MDIO 4'h8: SPI3_MOSI_M0 4'h9: I2C0_SCL_M1 4'ha: UART9_CTSN_M0 4'hb: PWM6_M2
3:0	RW	0x0	gpio4c4_sel 4'h0: GPIO 4'h1: GMAC0_MDC 4'h8: SPI3_MISO_M0 4'h9: I2C7_SDA_M1 4'ha: UART9_RTSN_M0 4'hb: PWM5_M2

**BUS IOC GPIO4D IOMUX SEL L**

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:12	RW	0x5	gpio4d3_sel 4'h0: GPIO 4'h1: SDMMC_D3 4'h2: PDM1_SDI0_M0 4'h5: JTAG_TMS_M0 4'h9: I2C8_SDA_M0 4'ha: UART5_RTSN_M0 4'hb: PWM10_M1
11:8	RW	0x5	gpio4d2_sel 4'h0: GPIO 4'h1: SDMMC_D2 4'h2: PDM1_SDI1_M0 4'h5: JTAG_TCK_M0 4'h9: I2C8_SCL_M0 4'ha: UART5_CTSN_M0
7:4	RW	0x0	gpio4d1_sel 4'h0: GPIO 4'h1: SDMMC_D1 4'h2: PDM1_SDI2_M0 4'h5: JTAG_TMS_M1 4'h9: I2C3_SDA_M4 4'ha: UART2_RX_M1 4'hb: PWM9_M1
3:0	RW	0x0	gpio4d0_sel 4'h0: GPIO 4'h1: SDMMC_D0 4'h2: PDM1_SDI3_M0 4'h5: JTAG_TCK_M1 4'h9: I2C3_SCL_M4 4'ha: UART2_TX_M1 4'hb: PWM8_M1

**BUS IOC GPIO4D IOMUX SEL H**

Address: Operational Base + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio4d5_sel 4'h0: GPIO 4'h1: SDMMC_CLK 4'h2: PDM1_CLK0_M0 4'h4: TEST_CLKOUT_M0 4'h5: MCU_JTAG_TMS_M0 4'h9: CAN0_RX_M1 4'ha: UART5_TX_M0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3:0	RW	0x0	gpio4d4_sel 4'h0: GPIO 4'h1: SDMMC_CMD 4'h2: PDM1_CLK1_M0 4'h5: MCU_JTAG_TCK_M0 4'h9: CAN0_TX_M1 4'ha: UART5_RX_M0 4'hb: PWM7_IR_M1

## 6.28 VCCIO1\_4\_IOC Register Description

### 6.28.1 Registers Summary

<b>Name</b>	<b>Offset</b>	<b>Size</b>	<b>Reset Value</b>	<b>Description</b>
VCCIO1_4_IOC_GPIO1A_DS_L	0x0020	W	0x00006666	GPIO1A Driver Strength Control Low bits
VCCIO1_4_IOC_GPIO1A_DS_H	0x0024	W	0x00006666	GPIO1A Driver Strength Control High bits
VCCIO1_4_IOC_GPIO1B_DS_L	0x0028	W	0x00006666	GPIO1B Driver Strength Control Low bits
VCCIO1_4_IOC_GPIO1B_DS_H	0x002C	W	0x00006666	GPIO1B Driver Strength Control High bits
VCCIO1_4_IOC_GPIO1C_DS_L	0x0030	W	0x00001111	GPIO1C Driver Strength Control Low bits
VCCIO1_4_IOC_GPIO1C_DS_H	0x0034	W	0x00001111	GPIO1C Driver Strength Control High bits
VCCIO1_4_IOC_GPIO1D_DS_L	0x0038	W	0x00001111	GPIO1D Driver Strength Control Low bits
VCCIO1_4_IOC_GPIO1D_DS_H	0x003C	W	0x00006611	GPIO1D Driver Strength Control High bits
VCCIO1_4_IOC_GPIO1A_P	0x0110	W	0x0000D555	GPIO1A Pull-up/down Control
VCCIO1_4_IOC_GPIO1B_P	0x0114	W	0x0000FF57	GPIO1B Pull-up/down Control
VCCIO1_4_IOC_GPIO1C_P	0x0118	W	0x00005550	GPIO1C Pull-up/down Control
VCCIO1_4_IOC_GPIO1D_P	0x011C	W	0x0000F555	GPIO1D Pull-up/down Control
VCCIO1_4_IOC_GPIO1A_I_E	0x0180	W	0x000000FF	GPIO1A Input Enable Control
VCCIO1_4_IOC_GPIO1B_I_E	0x0184	W	0x000000FF	GPIO1B Input Enable Control
VCCIO1_4_IOC_GPIO1C_I_E	0x0188	W	0x000000FF	GPIO1C Input Enable Control
VCCIO1_4_IOC_GPIO1D_I_E	0x018C	W	0x000000FF	GPIO1D Input Enable Control
VCCIO1_4_IOC_GPIO1A_SMT	0x0210	W	0x00000000	GPIO1A Schmitt Trigger Control
VCCIO1_4_IOC_GPIO1B_SMT	0x0214	W	0x00000000	GPIO1B Schmitt Trigger Control
VCCIO1_4_IOC_GPIO1C_SMT	0x0218	W	0x00000000	GPIO1C Schmitt Trigger Control