ECE 284 – Final Project Deliverables

It is very important to attach all the files mentioned below in a zip file in the **exact same structure**. Please follow the directory structure within the zip file as below:
Not following the structure may result in up to **15%** penalty.

You should name the zip file as follows: "**ECE284_Team_<Teamname>.zip**"

Your zip file should contain the following main folders
ECE284_Team_<Teamname>.zip

- ➔ Part1
- ➔ Part2
- ➔ Part3
- ➔ Part4
- ➔ Part5
- ➔ Part6
- ➔ Part7

Please find below the detailed file deliverables for each part and structure them as shown

- ➔ **Part1**
  - ➔ VGG16_Quantization_Aware_Training.ipynb
  - ➔ VGG16_Quantization_Aware_Training.pdf
  - ➔ **misc**
    - ➔ Add any miscellaneous files (Eg. Modified .py files, etc)

Notes:

- PDF file should indicate accuracy > 90%.
- Indicate the modified 8 input/output channels' layer using print(model)
- Error < 0.001 for psum_recovered must be visible in the PDF

- ➔ **Part2**
  - ➔ **verilog**
    - ➔ core.v
    - ➔ corelet.v
    - ➔ mac_array.v
    - ➔ etc.. all design files must be added here
  - ➔ **sim**
    - ➔ filelist

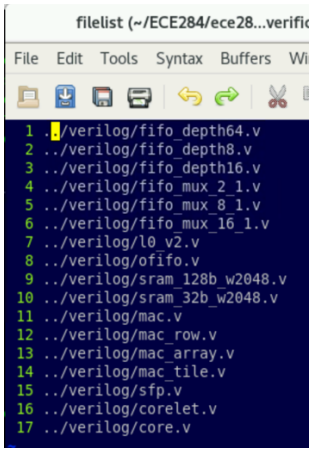
Note:

- "filelist" file should be named just "filelist" (**no** .txt, .pdf, .doc etc)
- Filelist should contain paths for all design files (See snapshot below for how to specify the paths. Do not provide full absolute paths that have your username etc. Just follow the structure like in the snapshot below, so that we can compile from your submitted folders directly
- TAs will do:

- cd Part2/sim/
- iveri filelist

Expectation: Your design should be compiled without any errors. No testbench is needed for this Part

- Example filelist snapshot:



➔ **Part3**

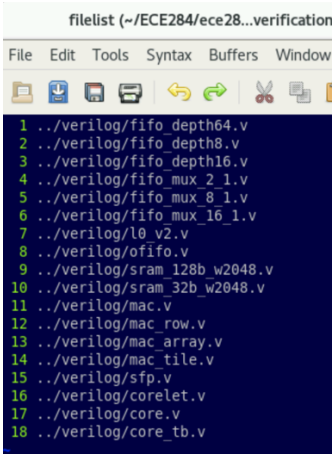
- ➔ **verilog**
  - ➔ core.v
  - ➔ corelet.v
  - ➔ mac_array.v
  - ➔ etc.. all design files must be added here
- ➔ **sim**
  - ➔ filelist
  - ➔ activation.txt
  - ➔ weight_kij0.txt
  - ➔ weight_kij1.txt
  - ➔ .
  - ➔ .
  - ➔ weight_kij8.txt
  - ➔ psum.txt
  - ➔ (Can place any text files that your testbench reads, here in this **sim** folder)

Note:

- "filelist" file should be named just "filelist" (**no** .txt, .pdf, .doc etc)
- Filelist should contain paths for all design files + core_tb.v(See the snapshot below for how to specify the paths). Do not provide full absolute paths that have your username etc. Just follow the structure like in the snapshot below so that we can compile from your submitted folders directly
- TAs will do: (May replace your .txt files with TA's activation/weight text files)
  - cd Part3/sim/
  - iveri filelist
  - irun

Expectation: Your design should be compiled without any errors. Data Matched Message must be printed for "psum" as well as for the final "output feature" obtained post accumulation in SFP

- Example filelist snapshot:



➔ **Part4**
  ➔ FPGA_Report.pdf

Note:

- Your FPGA Report PDF should have a Table that contains below parameters:

Cyclone IV FPGA Mapping of Vanilla Version	
Fmax	132.29 MHz
Switching Activity	20%
PVT	ss-1.2V-100C
Thermal Dynamic Power	15.69 mW
Total Logic Elements	8,476
Total Registers	4,234
Total Operations	8x8x2 = 128
GOPs/s	17
TOPs/W	1.079

(The numbers above are for a heavily optimized design. Your numbers may be much higher or lower depending on the design. Don't take the numbers above as expected values. This snapshot is to give you an idea of what parameters you should capture in your Table and how to calculate them)

➔ **Part5**
  ➔ **verilog**
    ➔ core.v
    ➔ corelet.v
    ➔ mac_array.v
    ➔ etc.. all design files must be added here
  ➔ **sim**
    ➔ filelist
    ➔ activation.txt
    ➔ weight_kij0.txt
    ➔ weight_kij1.txt
    ➔ .
    ➔ .
    ➔ weight_kij8.txt

- ➔ psum.txt
- ➔ (Can place any text files that your testbench reads, here in this **sim** folder)

Note: You should follow the same structure as Part 3. All design files (even non-modified ones like SRAM) must be added again in this folder for TA verification purposes. Your testbench for Part 5 will be different so add your new core_tb.v file accordingly in this folder

- ➔ **Part6**
  - ➔ **Alpha1**
  - ➔ **Alpha2**
  - ➔ **.**
  - ➔ **.**

Note: This is a very open-ended part. Your file deliverables depend on whether your Alpha is a Software or a Hardware Idea. If software, follow the Part1 structure under each Alpha folder. If Hardware, follow Part 2/3/5 type structure under the respective Alpha folder. You may add a simple "Readme" file to explain the file deliverables for your Alpha.

- ➔ **Part7**
  - ➔ **ECE284_Team_<Teamname>_Poster.pdf**
  - ➔ **ECE284_Team_<Teamname>_Report.pdf**

Note: Use this Directory to upload your Poster and Report. See Project Description on the assignment tab for Poster and Report Guidelines

Final Comments:

1. You should make an **initial submission by Dec 3rd 11:59 pm** (If your poster session is on Dec 3rd) and **by Dec 5th 11:59 pm** (If your poster session is on Dec 5th)

- Please note this submission will be used as *proof of progress* until the poster day (e.g., functionality pass, alpha implementation, and others) while the final submission will be used for the final grading.
- You need not submit Poster and Report in this submission

2. You should make the **final submission by Dec 14th at 11:59 pm**

- This submission will be used for final grading.
- Any additions after the Poster Session will be given only 70% of the score
  For eg., if you did not upload Part 5 in the initial submission, because you did not start WS+OS style by the poster day, and you only upload it in Final Submission, you will be given only 70% of the score for that part. (So, don't forget to make good progress on all parts by Poster Day!)
- If you choose to add more Alphas after Poster Day, those Alphas will also be Capped at max 70%