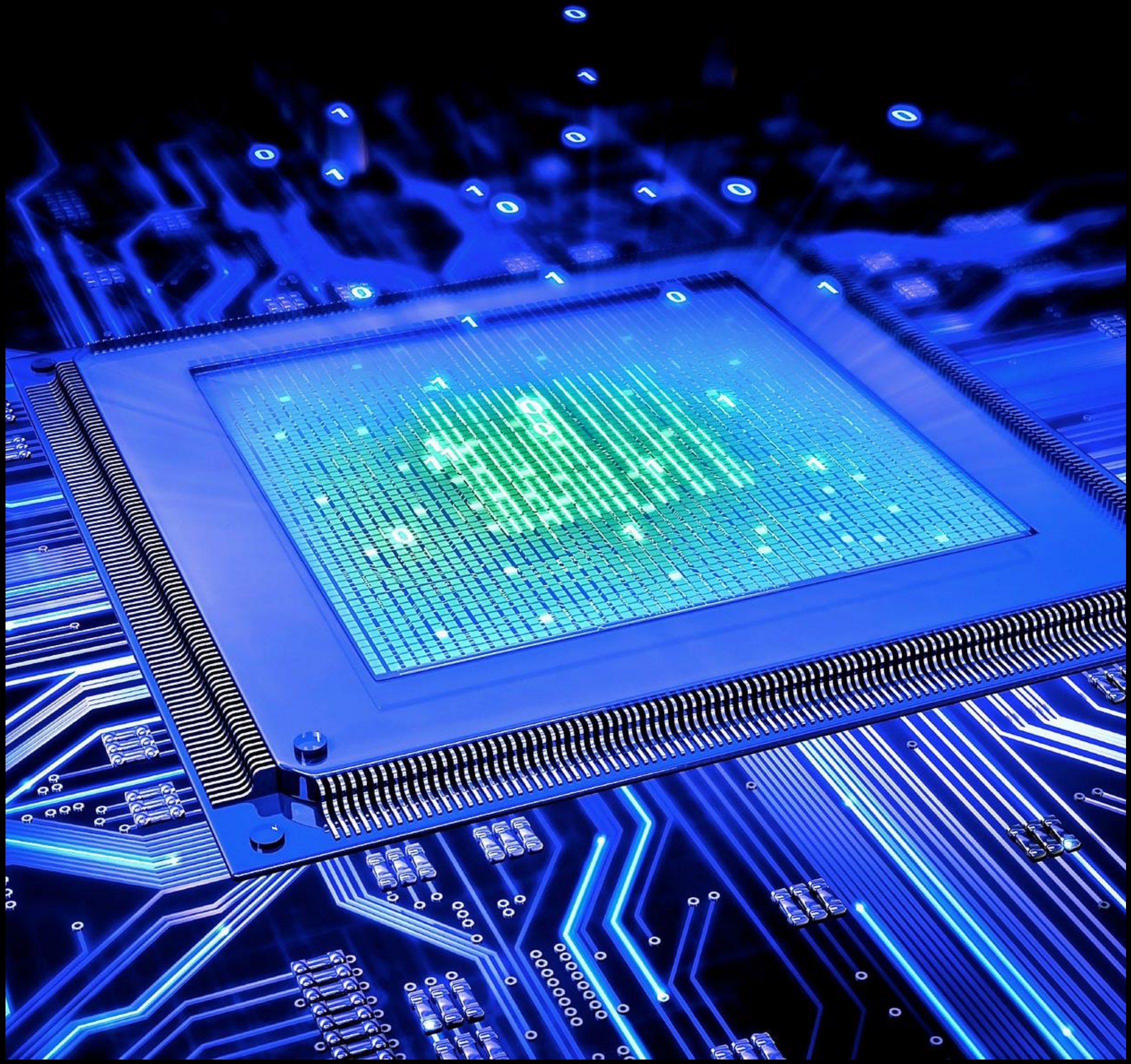
CSE3666-INTRODUCTION TO COMPUTER ARCHITECTURE

LAB 5

One Bit ALU



EXTRA SUPPORT

- Jacob.gerow@uconn.edu
- Find me in class discord
- Office Hours: 11:15am-12:15pm Wednesday
- BEACH (ITE 360) Drop-in Hours **Subject to change**:

Tuesday 6:00pm-8:00pm

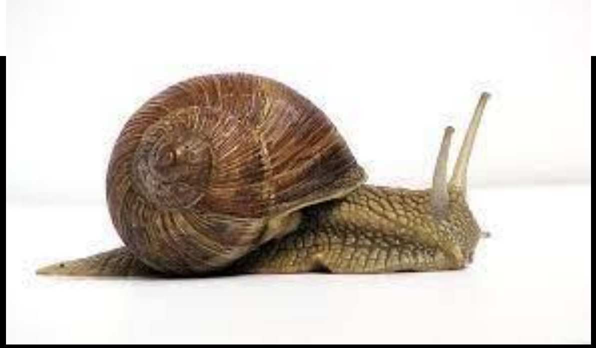
Thursday 4:00pm-8:00pm

Friday 6:00pm-8:00pm

WHAT IS A HARDWARE DESIGN LANGUAGE (HDL)

- Not a programming language (but similar)
- Specification for how hardware should behave

Software Implementation



Hardware Implementation

HARDWARE DESIGN LANGUAGES (HDL)

- Describe a design in a way engineers can understand
- Can be utilized to test descriptions of designs
- Are used to synthesize designs for Programmable Logic Devices (PLDs) and Field Programmable Gate Arrays (FPGAs)

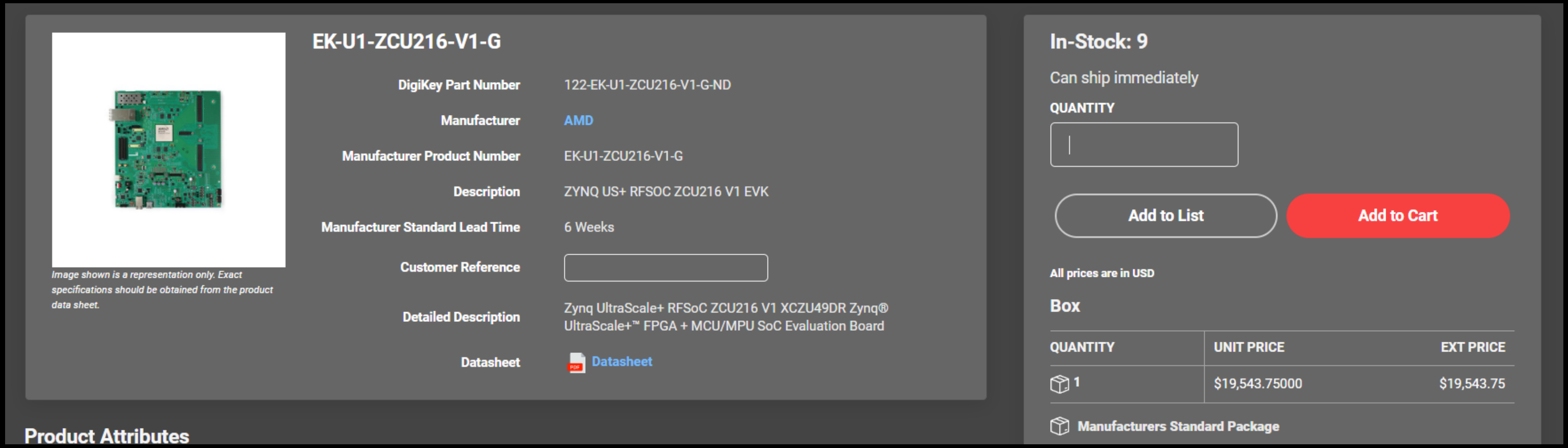


Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

EK-U1-ZCU216-V1-G

DigiKey Part Number	122-EK-U1-ZCU216-V1-G-ND
Manufacturer	AMD
Manufacturer Product Number	EK-U1-ZCU216-V1-G
Description	ZYNQ US+ RFSOC ZCU216 V1 EVK
Manufacturer Standard Lead Time	6 Weeks
Customer Reference	
Detailed Description	Zynq UltraScale+ RFSoC ZCU216 V1 XCZU49DR Zynq® UltraScale+™ FPGA + MCU/MPU SoC Evaluation Board
Datasheet	Datasheet

Product Attributes

In-Stock: 9

Can ship immediately

QUANTITY

All prices are in USD

Box

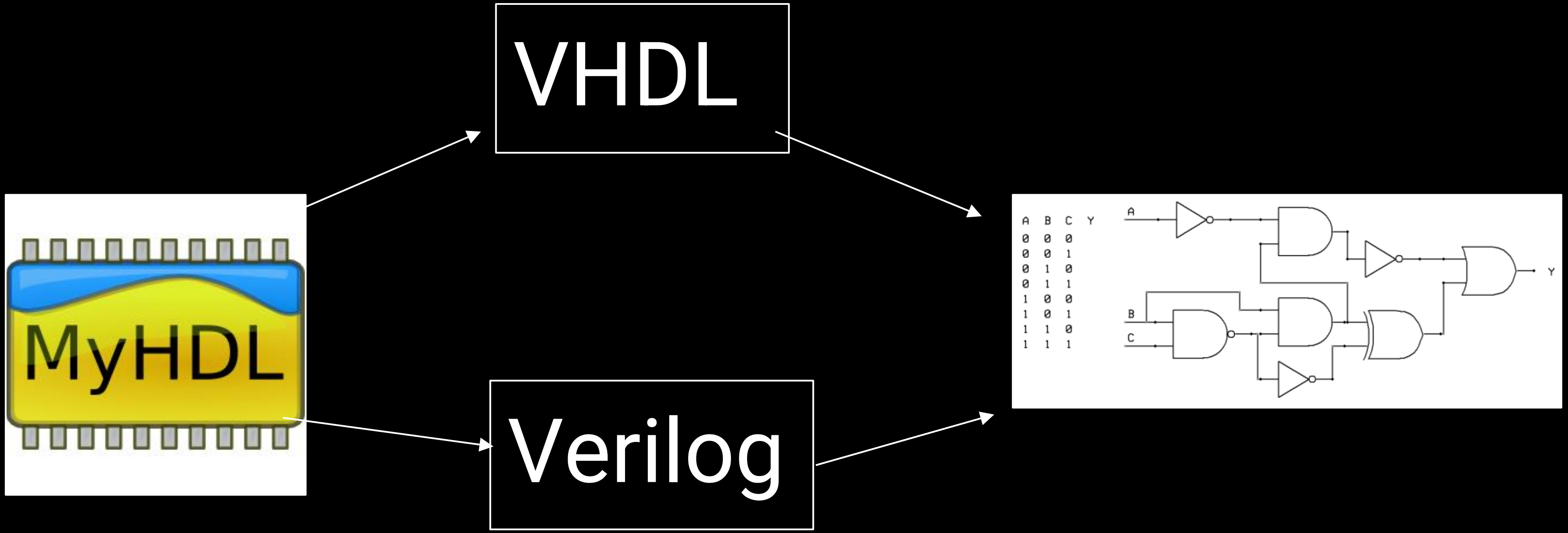
QUANTITY	UNIT PRICE	EXT PRICE
1	$19,543.75000	$19,543.75

Manufacturers Standard Package

HOW ARE HARDWARE DESIGN LANGUAGES USED

1. Engineer creates a design for a project
2. Engineer creates a “testbench” for a project (testbench itself is another design)
3. Once the two solutions match project is synthesized into real design components (latches, and gates, or gates, multiplexers, etc.)
4. Synthesized Project is tested and eventually deployed onto a device

WHAT IS MYHDL



VHDL

Verilog

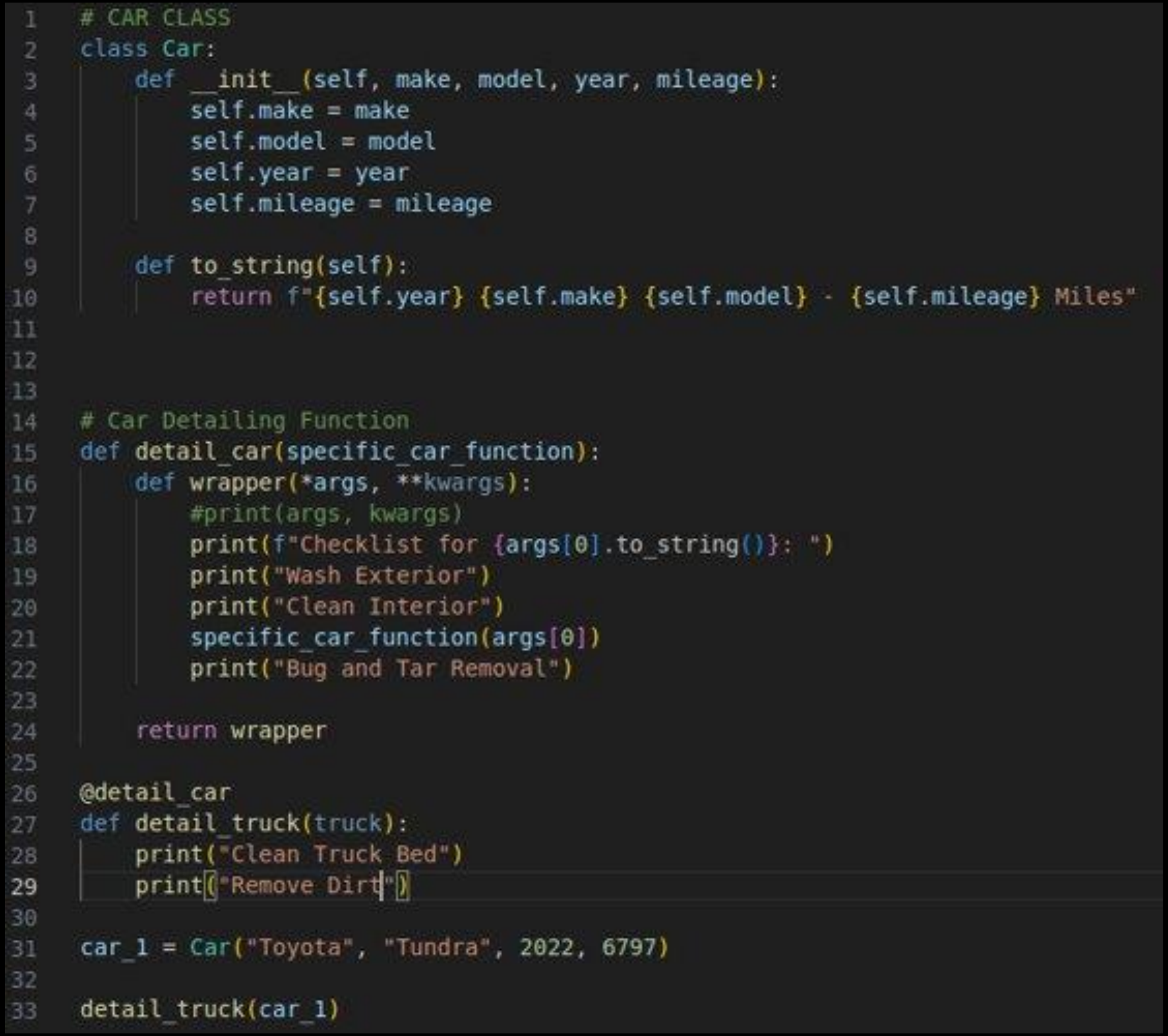
A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Basically it’s just good if you only want to program in python

IMPORTANCE OF .NEXT

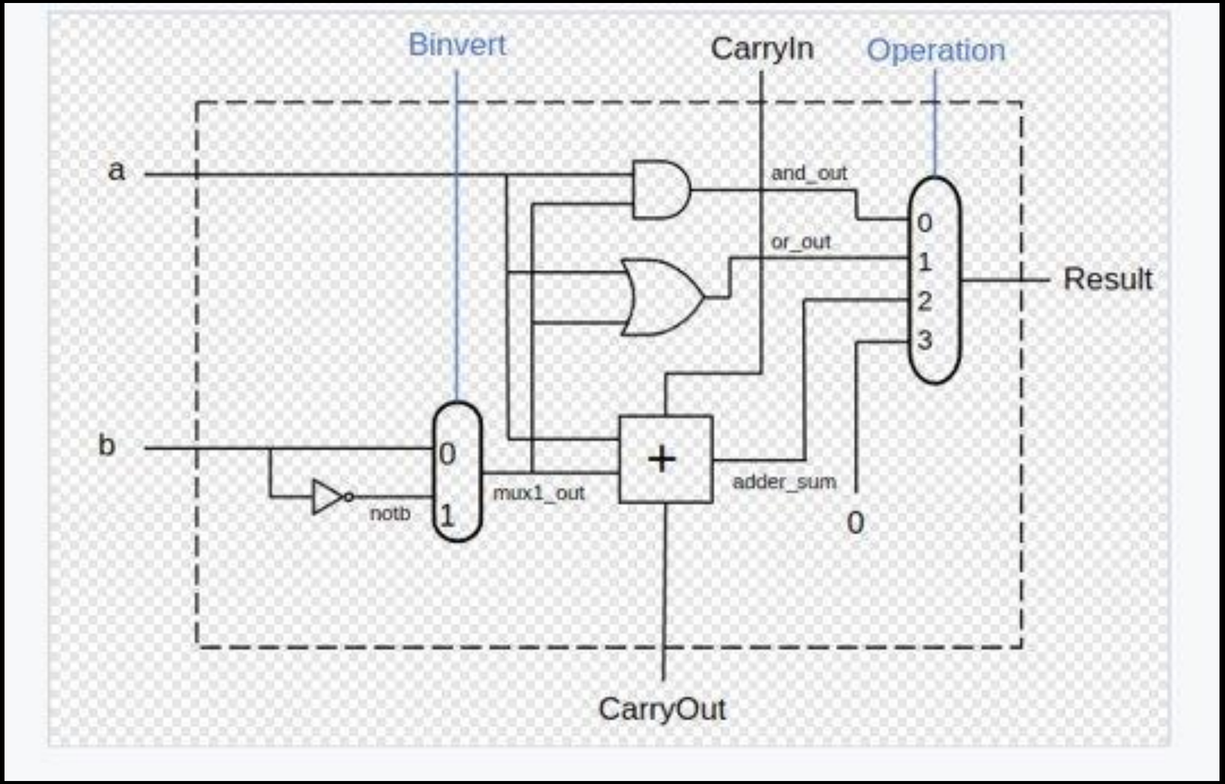
- signal = 1 tries to overwrite the instantaneous current value of signal (Does not work)
- signal.next = 1 sets the next value of the signal to 1 (after propagation delays) (correct implementation)

DECORATORS



```python
# CAR CLASS
class Car:
    def __init__(self, make, model, year, mileage):
        self.make = make
        self.model = model
        self.year = year
        self.mileage = mileage

    def to_string(self):
        return f"{self.year} {self.make} {self.model} - {self.mileage} Miles"



# Car Detailing Function
def detail_car(specific_car_function):
    def wrapper(*args, **kwargs):
        #print(args, kwargs)
        print(f"Checklist for {args[0].to_string()}: ")
        print("Wash Exterior")
        print("Clean Interior")
        specific_car_function(args[0])
        print("Bug and Tar Removal")

    return wrapper

@detail_car
def detail_truck(truck):
    print("Clean Truck Bed")
    print("Remove Dirt")

car_1 = Car("Toyota", "Tundra", 2022, 6797)

detail_truck(car_1)
```

FOLLOW THIS SCHEMATIC AND LINK EACH SIGNAL TOGETHER



AUTOGRADER SPECIFICATIONS

Use "and", "or", "not" instead of "&", "|", "~"

^ for xor is still fine

IMPORTANT RESOURCES

Discord (must join, **change name to first and last**, and set role):
https://discord.gg/xE4fTGRS

Github Repo: https://github.uconn.edu/zhs04001/cse3666-2025spring

Lab Presentation Repo: https://github.com/Jacob-Gerow/CSE_3666