Shenzhen Youritech Technology Co., Limited

specification

size of

product:

product code: ET039XGM

client
Approved by Customer
Date of approval:

fiction	examine and verify	ratify	
		R &D	O A

catalogue

specification

Revised records

edition	revision note	Revised date	remarks
Y01	The initial version	2022 -0913	

.summary

ET039XGM Is a 0.39-inch full-color silicon-based display module with a 1024 * 768 dot array. The display module is characterized by high brightness, high contrast, narrow frame, wide view, wide temperature domain and low power consumption, used for head-mounted display and AR glasses.

2. Product characteristics

- Display color: full color
- Highest resolution of 1024 * 768
- Digital video interface

  -Support for 24-bit RGB digital video
  -Support for 24-bit YCbCr digital video
  -Supports a 16-bit 4:2:2 format for YCbCr digital video
  -Support for a line-by-line scan

- Digital signal enhancement

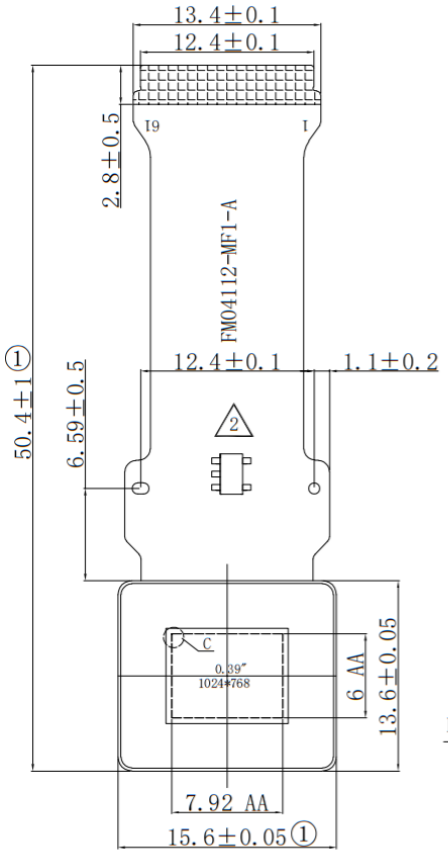
  -contrast control

- 8-bit input, 256-level gray scale display, and 10-bit D / A transformation
- Horizontal / vertical mirror images
- 2-line serial encoding interface
- Working at-40℃ ~65℃ (to ensure the normal operation of the chip, the heat dissipation module is required, and the recommended operating temperature is 60℃)

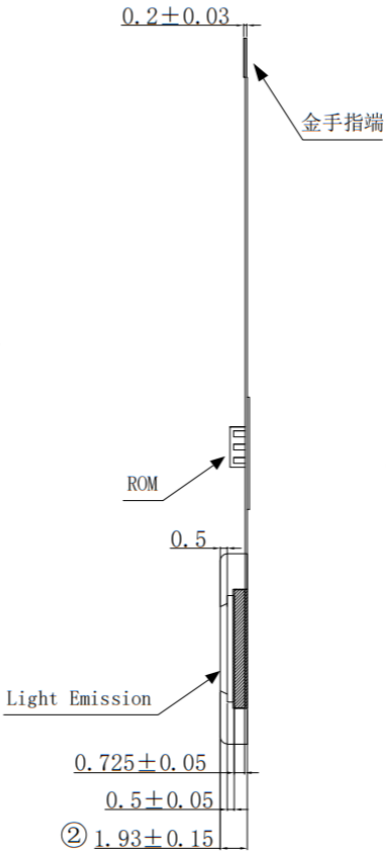
3. Structural parameters

order number	project	specifications	unit
1	Resolution ratio	1024×768	-
2	Pixel size	7.5×7.5	μm^2
3	Pixel spacing	7.5	μm^2
4	Display the area	7.92×6.00	mm^2
5	Screen body size	11.72×8.41	mm^2
6	Module size (FPCA)	50.4×15.6	mm^2
7	Diagonal dimension of area A / A	0.39	inch
8	Module weight	0.73±0.1	gram

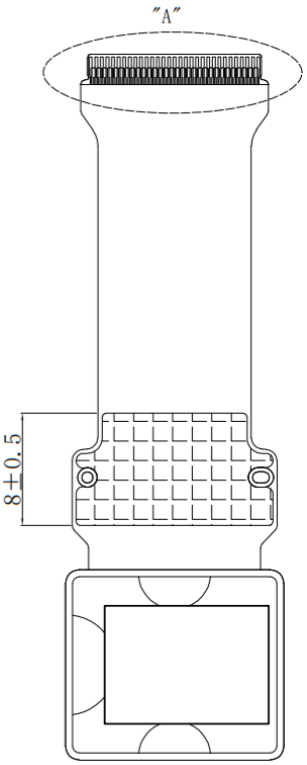
4. Structure diagram



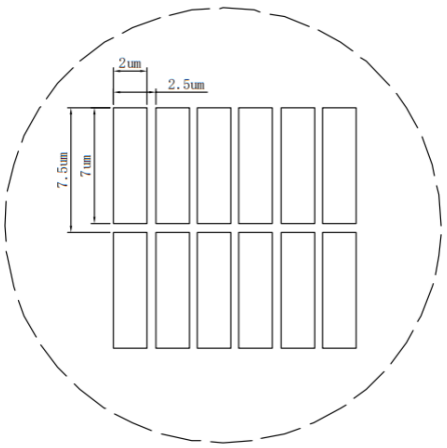
front view



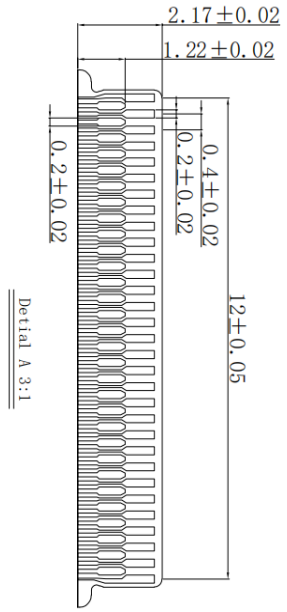
lateral view



dorsal view



Scale plot of local pixels



Scale view of the golden finger area

5 module interface

Pin order	Pin definitio n	type	description
1	V SS	V SS	landing
2	V COM	source	OLED, the device co-cathode
3	AVDD	source	The 5V power supply is connected with the parallel connection capacitor 22uF, 0.1uF to the ground
4	V SS	V SS	landing
5	V SS	V SS	landing
6	V SS	V SS	landing
7	V SS	V SS	landing
8	VDD1V8	source	Digital power supply 1.8V is connected to the 0.1 uF capacitor to the ground
9	P CLK	import	Pixel clock
10	H S	import	horizontal synchronizing signal
11	VS	import	field sync signal
12	OLED RST	import	reset signal
13	R 7	import	Red [7] digital video input
14	R 6	import	Red [6] digital video input
15	R 5	import	Red [5] digital video input
16	R 4	import	Red [4] digital video input
17	R 3	import	Red [3] digital video input
18	R 2	import	Red [2] digital video input
19	R 1	import	Red [1] digital video input
20	R 0	import	Red [0] digital video input
21	G 7	import	Green [7] for digital video input
22	G 6	import	Green [6] for digital video input
23	G 5	import	Green [5] for digital video input
24	G 4	import	Green [4] for digital video input
25	G 3	import	Green [3] for digital video input
26	G 2	import	Green [2] for digital video input
27	G 1	import	Green [1] for digital video input
28	G 0	import	Green [0] for digital video input

29	VDD1V8	source	Digital power supply 1.8V isconnected to the 0.1 uF capacitor to the ground
30	V SS	V SS	landing
31	B 7	import	Blue [7] for digital video input
32	B 6	import	Blue [6] for digital video input
33	B 5	import	Blue [5] for digital video input
34	B 4	import	Blue [4] for digital video input
35	B 3	import	Blue [3] for digital video input
36	B 2	import	Blue [2] for digital video input
37	B 1	import	Blue [1] for digital video input
38	B 0	import	Blue [0] for digital video input
39	ADDR 0	import	Internal I²C Slave address control
40	N C	N C	hang in the air
41	REF IN	import	Reference voltage control port, connecting the 0.1 uF capacitor to the ground
42	N C	N C	hang in the air
43	I²C SCL	import	I ²C Serial communication clock line
44	N C	N C	hang in the air
45	I²C SDA	Input / output	The I ²C serial communication data line
46	D E	import	Data valid signal
47	V SS	V SS	landing
48	V SS	V SS	landing
49	VDD1V8	source	Digital power supply 1.8V is connected to the 0.1 uF capacitor to the ground
50	FSA R	output	R channel brightness adjustment, connected to 12 K resistance to the ground
51	FSA G	output	G channel brightness adjustment, connected to 12 K resistance to the ground
52	FSA B	output	B channel brightness, adjust, connected with 12 K resistance to the ground
53	BW R	import	R channel DAC performance control port, connected 0.1 uF, capacitance to 1.8V
54	BW G	import	G channel DAC performance control port, connected 0.1 uF, capacitance to 1.8V
55	BW B	import	A B-channel DAC performance control port, connected with a 0.1 uF capacitor to 1.8V
56	V SS	V SS	landing
57	V SS	V SS	landing
58	V SS	V SS	landing
59	AVDD	source	The 5V power supply is connected with the parallel connection capacitor 22uF, 0.1uF to the ground
60	V COM	source	OLED, the device co-cathode
61	V SS	V SS	landing

6. Limit the operating range

project	characteristic	least value	crest value	unit	remarks
1.8V power supply	VDD 1V8	-0.3	2	V	IC maximum range value
5V power supply	A VDD	-0.3	6	V	IC maximum range value
Negative power supply	V COM	-5.5	0	V	IC maximum range value
working temperature	Top	-40	+65	℃	-
storage temperature	Tpnl	-55	+80	℃	-

Note: The maximum range value is the limit value that cannot be exceeded in the instant. Using or exceeding these ratings may affect the product Life and reliability, but the product can also be damaged. It is recommended to work under the typical operating conditions of the product.

7. Rated operation range

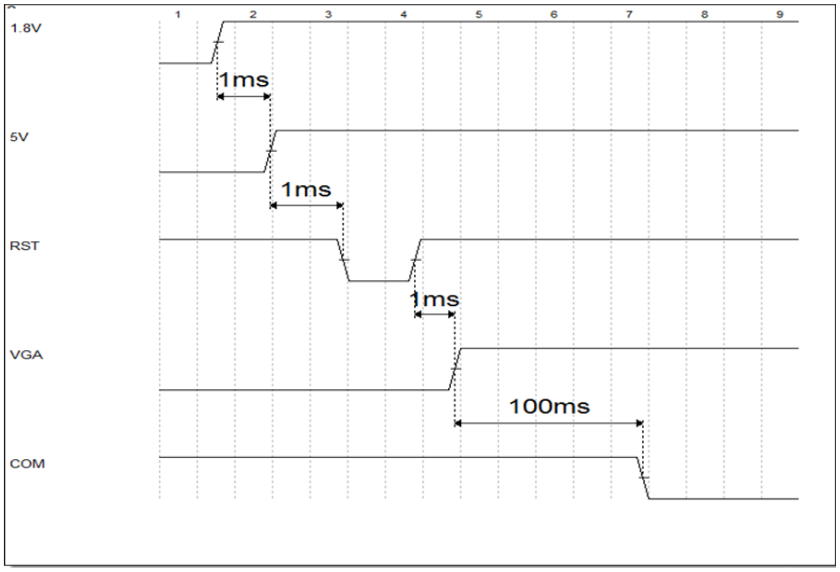
project	characteri stic	test condition	least value	representa tive value	crest valu	unit
working voltage	VDD1V8	_	1.62	1.8	1.98	V
	A VDD	_	4.5	5	5.5	V
	V COM	_	-	0	-	V
high level input voltage	VIH	_	0.7VDD	-	VDD	V
low level input voltage	VIL	_	0	-	0.3VDD	V
high level input voltage	Vt+	Schm itt Enter	0.7VDD	-	VDD	
low level input voltage	Vt+	Sc hmitt Enter	0	-	0.3VDD	
Vt + - Vt+	V hys	Sc hmitt Enter	-	0.50	-	
Logic high-level output voltage	VOH	_	VDD -0.4	-	-	V
Logic low-level output voltage	VOL	_	-	-	0.4	V

8. Photoelectric characteristics

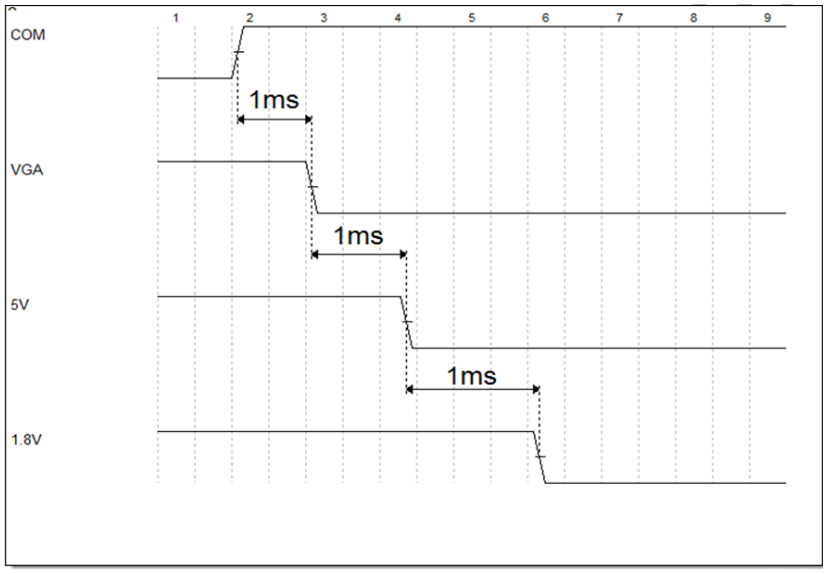
project	symbol	test condition	least value	represe ntative value	crest value	unit
Normal mode, type brightness	Lbr	Full pixel lighting (white light)	-	300	-	c d/ m 2
Normal-mode power consumption	Pt	Full pixel lighting (white light)	-	85	-	m W
Color coordinate (white)	(x)	x ,y (CIE 1931)	0.28	0.31	0.34	-
	(y)		0.30	0.33	0.36	-
Color coordinate (red)	(x)		0.57	0.60	0.63	-
	(y)		0.30	0.33	0.36	-
Color coordinate (green)	(x)		0.20	0.23	0.26	-
	(y)		0.60	0.63	0.66	-
Color coordinate (blue)	(x)		0.11	0.14	0.17	-
	(y)		0.04	0.07	0.10	-
contrast ratio	C R	-	≥10000:1	-	-	-
Viewing Angle	-	-	-	TB D	-	Degree

9. Functional description and application circuit

9.r power supply time sequence



The electric timing



Under the electric timing

9.2 Color space conversion

When the input signal is YCbCr, this function can be converted to the RGB signal. When the input format is 4:4:4 format, the color space conversion function is directly used; when the input format is 4:2:2 format, it should first go through the internal 4:2:2 cases

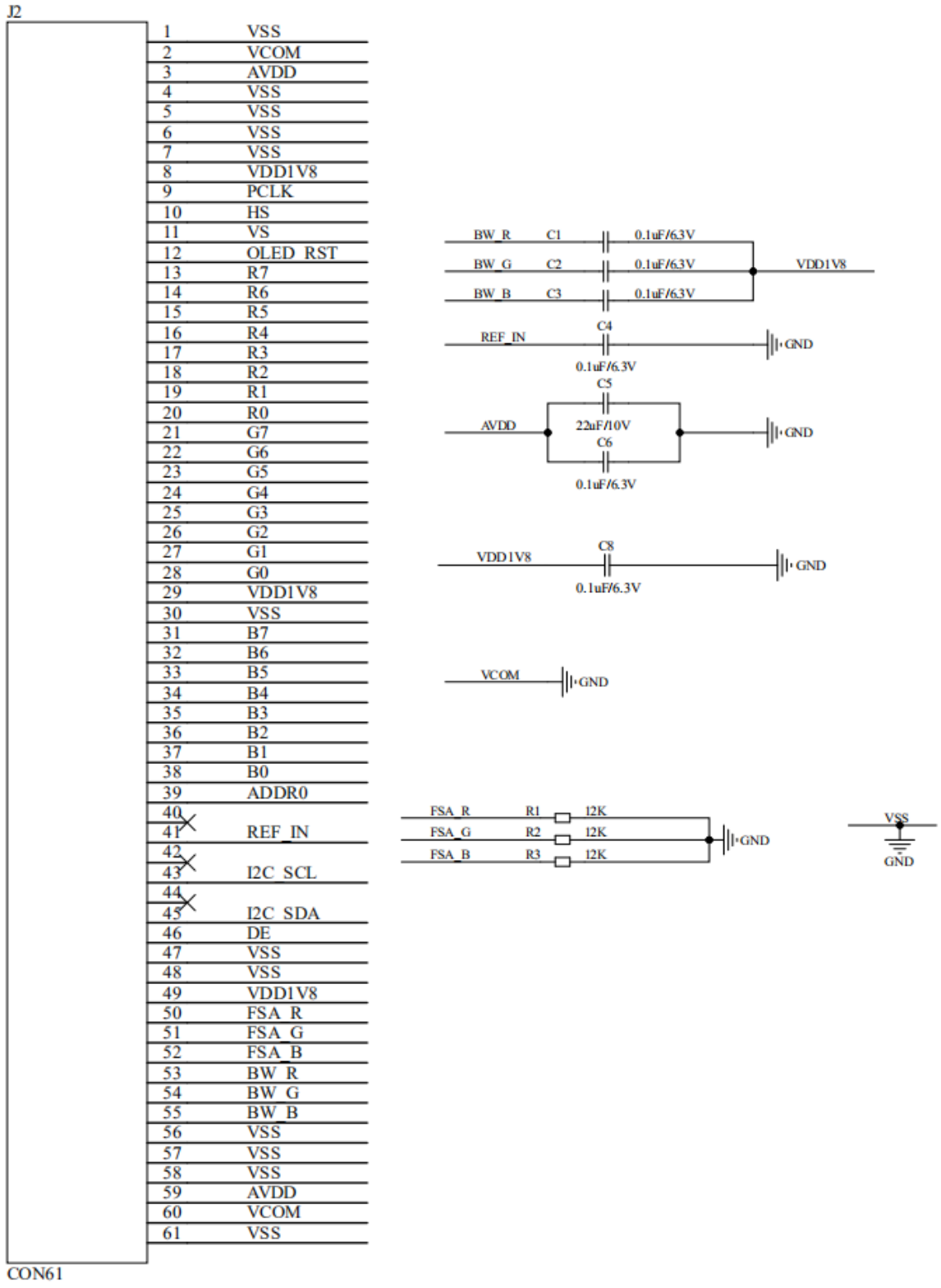
Conversion 4:4:4 format function module, then color space conversion.

Signal connection in 16 bit 4:2:2 format YCbCr, 24 bit 4:4:4 format YCbCr and 24 bit RGB format as shown in the table below.

order number	pin	Video format			remarks
		YCbCr (4:2:2)	YCbCr (4:4:4)	RGB (4:4:4)	
1	19~12	Y[7:0]	Y[7:0]	R [7:0]	
2	27~20	Cb Cr [7:0]	C b [7:0]	G[7:0]	
3	39~32	Unused, grounded	C r [7:0]	B [7:0]	

This function uses registers of 0 x 04 ~ 0 x 05.

9.3, the applied circuit



Match Connector Model: 61FVXS-RSM1-GAN_LF_SN

0. Register configuration description

The general overview of the register settings is shown in the following table:

address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	The reset value
0x00	Identify code registers								8'h 00
0x01	Temperature value access register								8'h 00
0x02	obligate				*	Sel _data _out			8'h 00
0x03	obligate	*	*	*	*	*	*	*	8'h 00
0x04	Sel _cr _in		Sel _cb _in		Sel _y _in		*	*	8'h 00
0x05	obligate	*	*	*	Sel _cbcr _in		Sel _y _in		8'hff
0x06			Gamma correction lose		*	*	Contrast input		8'h 00
0x07~ 0x1b	Lut values for gamma correction in R data								-
0x1c ~ 0x30	The lut value in the gamma correction for the G data								
0x31~ 0x45	B The lut values in the gamma correction for the data								
0x46~ 0x56	The region-values in the gamma correction								-
0x57	Contrast adjustment register								8'h 40
0x58	*								8'h 00
0x59	obligate								8'h 00
0x5a~ 0x5b	Displays location movement time = {0x 5b, 0x 5a} * 16.6ms								8'h 00
0x5c	Displays the number of rows moved by the position								8'h 00
0x5d	Displays the number of columns where the position moves								8'h 00
0x5e ~ 0x5f	0x 5e + 0x 5f = line back porch-1								8'h00/8'h9f
0x60	Back porch value-25								8'h 87
0x61	C _ DIN pulse width = clk * (0x 61 + 1)								8'h 00
0x62	Backfield Gallery-16								8'h 0d

0x63	T B	8'h 00
0x64	obligate	8'h 00
0x65	TB _ ENABLE _ OUT signal pulse width = clk * 4* 0x 65	8'h 80
0x66	PRESET _FOLLOW _TB signal pulse width = clk * 4* 0x 66	8'h 80
0x67	obligate	8'h 00
0x68	Select the test picture	8'h 00
0x69	Automatic switching test graph time interval=16.6 * 0x 69 ms	8'hb 4
0x6a	Full screen black and white squares (test figure 16) number of pixels per square	8'h 32

0x6b	Stripe width (number of pixels)							8'h0a
0x6c ~ 0x6d	Full-screen controllable grayscale graphics gray scale = {0x 6c, 0x 6d [1:0]}							8'h00~8'h00
0x6e ~ 0x81	4 * 4 of the test figure 25, area grayscale							8'h 00
0x82	obligate					*	*	8'h 00
0x83	Update the temperature value at 16.6 * This register value is ms							8'h 06
0x84	Count 1						*	8'h 14
0x85	Count 2							8'h 05
0x86	*	*	*	*	Sel _com _in		Sel _vref _in	8'h 00
0x87	temp _fedback _VREF							8'hd 0
0x88	temp _fedback _COM							8'he 3
0x89~ 0xa9	The lut value of the VREF-related temperature correction algorithm							
0xaa ~ 0xca	The lut value of the COM-related temperature correction algorithm							
0xcb	oblig ate	*	*	Sel _out		Sel _vs _in _pwm	*	8'h 00
0xcc	The first pulse of PWM							8'hff
0xcd	Generation time of the second pulse of the PWM							8'hff
0xce	The third pulse generation time of the PWM							8'h 00
0xcf	Fourth pulse generation time of the PWM							8'h 00
0xd 0	The fifth pulse generation time of the PWM							8'h 00
0xd 1	Sixth pulse generation time of the PWM							8'h 00
0xd 2	PWM first pulse generation time supplement							8'h 20
0xd 3	PWM second pulse generation time supplement							8'h 21
0xd4~ 0xd 5	Number of pixel cycles illuminated in one row of time {0 xd 4,0 xd 5}							8'h 00/8'h 64
0xd6	The PWM scan chain clock pulse width is the pixel clock * 0 xd 6 value							8'h 64
0xd7	obligate						*	8'h 00
0xd8	obligate		*	*	*	*	*	8'h 00
0xd9	Temperature value of the overtemperature protection							8'he 1
0xda	Restore the temperature value							8'hc 8
0xdb	Generation disable, signal field rear gallery count							8'h 19

0xdc	obligate						*	*	8'h 00
0xdd	*	*	*	*	*	*	*	*	8'h 00
0xde	CTR _R _IN [8:1]								8'h 00
0xdf	CTR _G _IN [8:1]								8'h 00
0xe0	CTR _B _IN [8:1]								8'h 00
0xe1	Pixel clock delay module A: DelayA Control[8:1]								8'h 00
0xe2	Pixel clock delay module B: DelayB Control[8:1]								8'h 00

0xe3	R-channel DAC brightness adjustment: BR _ R[8:1]								8'h ..
0xe4	G-channel DAC brightness adjustment: BR _ G[8:1]								8'h 7f
0xe5	B-channel DAC brightness adjustment: BR _ B[8:1]								8'h 7f
0xe6	obligate						EN _R _IN [4:1]		8'h 23
0xe7	EN _G _IN [4:1]						EN _B _IN [4:1]		8'h 23
0xe8	VREF Control [8:1]								8'h 23
0xe9	Analog signal module REG 15: Ctrl 1 ect.								8'h 1e
0xea	Analog signal module REG 16: Ctrl 2 ect.								8'h 18
0xeb	Number of blank rows above when displaying the low-resolution image								8'h 00
0xec	Number of left blank columns when displaying low-resolution images								8'h 00
0xed	Column direction compensation settings when displaying low-resolution images								8'h 00
0xee	{0 xee, 0 xf 0 [6:4]} is the number of lines showing the low resolution								8'h 00
0xef	{0 xef, 0 xf 0 [2:0]} is the number of columns showing the low resolution								8'h 00
0xf0	*	{0 xee, 0 xf 0[6:4]}: Total number of low resolution			obliga te	{0 xee, 0 xf 0[2:0]}: Total number of columns at low resolution			8'h 00
0xf1	obligate								8'h 80
0xf2	*			sel _3d _mode		left _right_frame		3d _mode _start	8'h 00
0xf3	obligate								8'h 01
0xf4	obligate								8'h 80
0xf5	sc6008_v 2: reg _sel _state								8'h 00
0xf6	TSTA [8:1]								8'h 00
0xf7	TSTB [8:1]								8'h 01
0xf8	DC _A [8:1]								8'hfe
0xf9	DC _B [8:1]								8'he 4
0xfa	DC _C [8:1]								8'he 0
0xfb	DC _D [8:1]								8'h 4c

Note: Reference I²C register details for settings with *.

The I ²C register detailed usage instructions are shown below.

1) I ²C address description

I²C, address bit			
Bi t	Bit Field	description	remarks
Bit [7:1]	I²C address	{000010,sla _ addr}, sla _addr is configurable	
Bit 0	R /W	I 2C read / write bits 0: Write 1: Read	

2) Identification code reserved address

Register address of 0x00		
Bi t	description	The reset value
Bit [7:0]	ID register when reading EEPROM. Read this EEPROM subsequent value when the 0x 00 address register value of EEPROM is 0 x A 3 ,otherwise not.	8'h00

3) Temperature value access register

Register address of 0x01		
Bi t	description	The reset value
Bit [7:0]	Temperature values are automatically updated to this register.	8'h00

4) The RGB data output selection register

Register address of 0x02			
Bi t	B IT FIELD	description	The reset value
Bit [7:4]	obligate	obligate	8'h00
Bit 3	Sel_timing	0: The timin g signal generated by the timing module 1: External input timing signal	
Bit [2:0]	Sel_data_out	000: gamma, ma correction data 001: {data_in,2'b00} 010: Contrast adjustment data 011: {data_in,2'b00} 100: {2'b00 , data_in} 101: Color swap data 110: {YCbCr , 2'b00} 111: {2'b00,YCbCr}	

4) Enter the selection register

Register address of 0x 03				
B it	Bit Field		description	The reset value
Bit 7	obligate	obligate		8'h 00
Bit 6	EN _SELF	0: VS / HS / DE polarity 1: Do not use the adaptive determined polarity 0: The data of the blanking area is the data given by the decoding chip		
Bit 5	D ATA	1: The data given by the blanking area is 0		
Bit 4	R _CK	0: For the input of R _CK 1: reverse for input R_CK		
Bit 3	T B	0: For the input TB 1: reverse the input TB		
Bit 2	DE	0: for input DE 1: reverse for input DE		
Bit 1	H S	0: Input HS 1: reverse for input HS		
Bit 0	V S	0: for input VS 1: reverse for input VS		

5) YCbCr to RGB correlation

Register address of 0x04			
Bi t	BIT FIELD	description	The reset value
Bit [7:6]	Sel _cr _in	YCbCr Turn to RGB for input selection 00:422 to 444 output CR _ OUT 01: b_in 10: r _in 11: g _in	8'h00
Bit [5:4]	Sel _cb _in	YCbCr Turn to RGB for input selection 00:422 to 444 output CB _ OUT 01: g_in 10: b _in 11: r _in	
Bit [3:2]	Sel _y _in	YCbCr Turn to RGB for input selection 00:422 to 444 output Y _ OUT 01: r_in 10: g_in 11: b_in	
Bit 1	Clk _gate _2	YCbCr Turn to the RGB gated clock 0: The clock is closed 1: The clock opens	
Bit 0	Clk _gate _1	422 to 444 format gating clock 0: The clock is closed 1: The clock opens	

Register address of 0x05			
Bit	BIT FIELD	description	The reset value
Bit 7	obligate	obligate	8'hff
Bit 6	Sel_out	After output cb and cr data swap 1: No swap 0: Exchange	
Bit 5	Sel_cbcr_flag	The first data at conversion is determined to be cb or cr 1: cb 0: cr	
Bit 4	Sel_de	1: de 0: de reverse	
Bit [3:2]	Sel_cbcr_in	422 format to 444 format input selection 00: r_in 10: b_in x 1: g_in	
Bit [1:0]	Sel_y_in	422 format to 444 format input selection 00: b_in 10: g_in x 1: r_in	

6) Contrast adjustment register

		Register address of 0x05	
Bit	BIT FIELD	description	The reset value
Bit [7:6]	obligate	obligate	8'h00
Bit [5:4]	Gamma correction for the input selection	Gamma correction module for input data selection 00: Contrast control module output 01: {RGB[7:0], 2'b00} 10: {2'b00, RGB[7:0]} 11: {YCBCR_OUT[7:0], 2'b00}	
Bit 3	gamma	Gamma correction clock 0: The clock opens 1: The clock is closed	
Bit 2	contrast	Contrast regulation clock 0: The clock opens 1: The clock is closed	
Bit [1:0]	Contrast input selection	Contrast regulation module input data selection x 0: {RGB[7:0], 2'b00} 01: {2'b00, RGB[7:0]} 11: {YCBCR_OUT[7:0], 2'b00}	

Register address of 0x 57		
B it	description	The reset value
Bit [7:0]	Contrast adjustment register	8'h 40

7) Color swap function register

Register address of 0x58			
Bi t	Bit Field	description	The reset value
Bit 7	Color swap clock	Color swap clock 0: The clock is closed 1: The clock opens	8'h 00
Bit 6	obligate	obligate	
Bit [5:4]	Color swap module B input select	Color swap module B input data selection 00: gamma correction module B output 01: {RGB_B[7:0],2'b00} 10: {2'b00,RGB_B[7:0]} 11: {YCBCR_OUT_B[7:0],2'b00}	
Bit [3:2]	Color swap module G input select	Color change module G input data selection 00: gamma correction module G output 01: {RGB_G[7:0], 2'b 00} 10: {2'b00, RGB_G[7:0]} 11: {YCBCR_OUT_G[7:0], 2'b00}	
Bit [1:0]	Color swap module R input select	Color swap module R input data selection 00: Gamma correction module R output 01: {RGB _ R [7:0], 2 'b00} 10: {2' b00, RGB _ R [7:0]} 11: {YCBCR_OUT_R[7:0], 2'b00}	

Register address of 0x59			
Bi t	Bit Field	description	The reset value
Bit [7:6]	obligate	obligate	8'h00
Bit [5:4]	Color swap module B channel output	B Data output selection 00: B_ OUT = B_IN 01: B_ OUT = R_IN 10: B_ OUT = G _IN 11: B _OUT = B _IN	
Bit [3:2]	Color swap module G-channel output	G Data output selection 00：G_OUT =G_IN 01：G_OUT =R_IN 10: G_OUT = B _IN 11: G_OUT = G _IN	
Bit [1:0]	Color swap module R-channel output	R Data output selection 00: R_OUT = R_IN 01: R_OUT = G_IN 10: R_OUT = B _IN 11: R_OUT = R _IN	

Take the R-channel data transformation register setting as an example:

1) Color swap module RGB channel input selection, When setting 0x58 [1:0] to 2'b00, R gamma calibration result as the color swap module R channel input; when setting 0x58 [1:0] to 2'b01, {RGB_R[7:0], The 2'b00} is used as the R channel input; When setting 0x58 [1:0] to 2'b10, {2'b00, RGB _ R [7:0]} acts as an input to the R channel; When setting 0x 58 [1:0] to 2'b10, {YCBCR_OUT_R[7:0], The 2'b00} is used as the R channel input;

2) Set 0x58 [7] to 1'b1 to open the gating clock. When performing the color change, always set 0x 58 [7] to be effective, otherwise the color change function cannot be realized;

3) Set 0x 59 [1:0] to 2'b00 to output R itself data, that is, the color of the display itself, set 0x 59 [1:0] is the output G channel data when 2 'b01, now the red and green color transformation, 0x59 [1:0] as the output B' b data 10, to realize the red and blue color transformation.

8) Temporal sequence correlation

Register address: 0x 5a / 0x 5b		
B it	description	The reset value
Bit [7:0]	Displays the position movement time ={0x 5b ,0x 5a }*16.6ms	8'h 00/8'h 00
Register address of 0x 5c		
B it	description	The reset value
Bit [7:0]	Displays the number of rows moved by the position	8'h 00
Register address of 0x 5d		
B it	description	The reset value
Bit [7:0]	Displays the number of columns where the position moves	8'h 00
Register address: 0x 5e / 0x 5f		
B it	description	The reset value
Bit [7:0]	0x 5e + 0x 5f = line back porch-1	8'h 00/8'h 9f
Register address of 0x 60		
B it	description	The reset value
Bit [7:0]	Back porch value-10	8'h 96
Register address of 0x 61		
B it	description	The reset value
Bit [7:0]	C _ DIN, and the pulsewidth =clk *(0x 61+1)	8'h 00
Register address of 0x 62		
B it	description	The reset value
Bit [7:0]	Field back porch-8	8'h 16

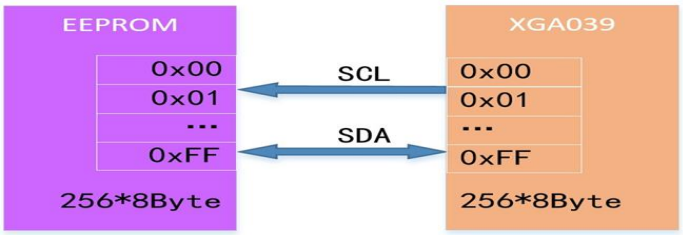
Register address of 0x 63			
B it	BIT FIELD	description	The reset value
Bit [7:6]	TB	00: TB _DLY [4] 01: TB _DLY [0] 10: TB _DLY [9] 11: TB _DLY [14]	8’h 00
Bit 5	C_DIN	0: HS _ FLAG generated inside 1: HS _ FLAG generated inside reverse	
Bit 4	R _CK	0: The HS generated internally 1: generated internally HS reverse	
Bit 3	R _DIN	0: VS generated internally reverse 1: The VS generated internally	
Bit 2	Sel _tb	0: Normal tb signal 1: flip frame tb with the previous frame	
Bit 1	Sel _col _move	0: No horizontal movement 1: Move horizontally	
Bit 0	Sel _row _move	0: No moving vertically 1: Move vertically	

11. Second-line serial interface

The chip internal integration applies to the functional module of the I²C standard protocol (8bit transmission protocol). Through the configuration of different registers, this module realizes the contrast adjustment, gamma correction and display position movement, which can directly communicate with the I²C upper computer chip.

This I²C will realize the reading data function as master after power up or reset, to find out whether there is a device supporting 2K EEPROM protocol on the I²C bus, the value inside the device is read to the internal 2K register according to the address, as shown in the following figure, where the value of EEPROM address 0x 00 should be 0 xA 3, as the identification code, otherwise the value of the address will not be updated later. After completing this function, do it

Communicate for slave with the external master, and can only exercise the function of slave.

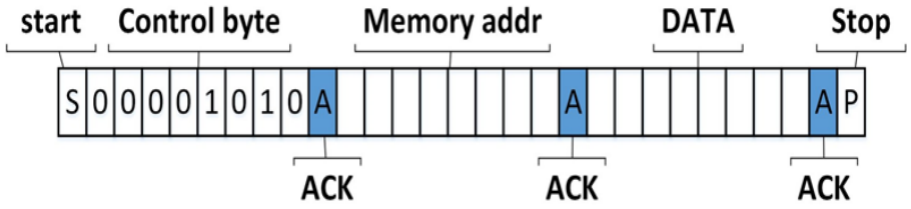


EEPROM Address to the I²C register address mapping

The address of this I²C is {6'b000010, sla _ addr}, plus a read and write bit becomes control byte.

FM 04112, I²C read and write instructions integrated inside the chip (take the address as 7'b0000101 as an example):

write data to one address at a time:



Write one register data SDA at a time

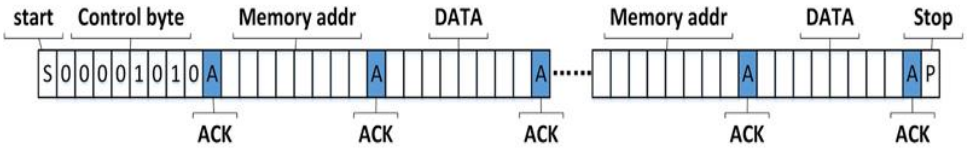
According to the timing of the figure above, the process of writing one register at a time is as follows:

1) master, send the start signal sta rt;
2) master then issues contro l byte and writes data to slave;
3) sla ve response;
4) master Send the register address to be written;
5) sla ve response;
6) master Data to write in the sending register

7) slave response;

8) The master generates an end signal.

Write data to multiple different registers:



Write more than one at a time, the register data SDAsignal

According to the timing of the figure above, the process of writing multiple registers at a time is as follows:

1) master sends a start signal start;

2) master then issues control byte and indicates the number to slaveoccupy;

3) slav e response;

4) master Send the register address to be written;

5) slave response;

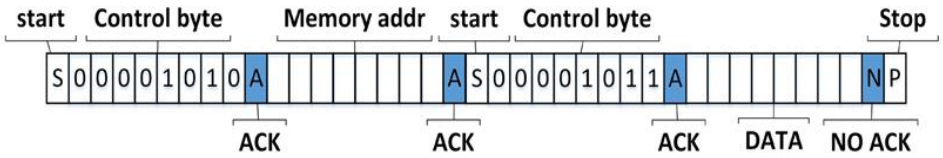
6) master, the data to be written by the sending register;

7) slave response;

8) Repeat 4) 5) 6) and 7) steps until all the required contactors are written;

9) The master generates an end signal.

Register data reading a specific address is shown in the following below:



Read Data SDA, schematic diagram

According to the timing of the above figure, the reading data process is as follows:

1) The mas ter sends out a start signal, start;

2) master then issues control byte and writes data to slave;

3) slave response;

4) master Send the register address to be read;

5) slave response;

6) master re-generates the start signal;

7) master then issues control by te and reads the data to slave;

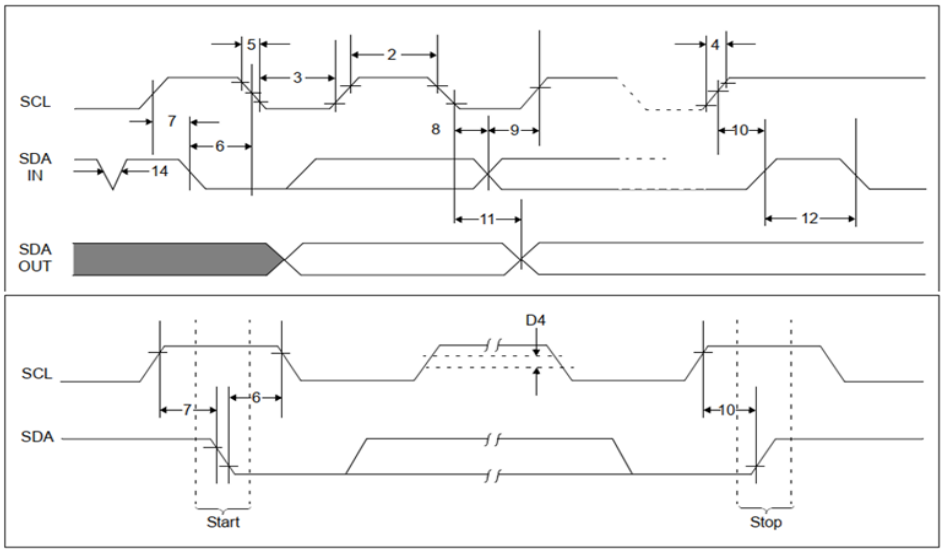
8) slave response;

9) s lave Send the register data to be read;

10) sla v e does not generate a response signal;

11) The master generates an end signal.

Referring to the I²C timing diagram below, the timing requirements of I²C communication are shown in the following table.



A Schematic diagram of the I ²C timingsequence

The timing requirements for the communication:

order number	parameter	characteristic	least value	representative value	crest value	unit
1	clock frequency	F clk	-	100	400	KH z
2	Clock high-leveltime	T high	4000	5000	-	ns
3	Clock low-leveltime	T low	4700	5000	-	ns
4	SDA and SCL rise time	Tr	-	-	300	ns
5	Time to decrease in SDA and SCL,respectively	T f	-	-	300	ns
6	Start Conditions Duration	Thd :sta	600	-	-	ns
7	Start the condition setting time	Tsu :sta	600	-	-	ns
8	Data Entry Duration	Thd :dat	0	-	-	ns
9	Set the time for the data entry	Tsu :dat	100	-	-	ns
10	Stop the condition for the setting of the time	Tsu :sto	600	-	-	ns
11	Clock output effective time	T aa	-	-	3500	ns

R 2. reliability

order number	test item	test condition	sample capacity	criterion for judgement	remarks
1	High temperature storage	Non-working condition of the product, test condition: 85℃, time 24H. After the test, the product is returned to room temperature to confirm the situation.	2pcs	Appearance OK, display function OK, color coordinates within the control range of our company	
2	High temperature work	Working condition of the product, test condition: 65℃, time 24H. After the test, the product is not removed, and the photoelectric parameters of the product are confirmed under this conditions. Check the product display function and appearance after removal and recovery to room temperature.	2pcs	Appearance OK, display function OK, color coordinates within the control range of our company	
3	Low temperature storage	Non-working condition of the product, test condition: -55℃, time 24H. After the test, the product is returned to room temperature to confirm the situation.	2pcs	Appearance OK, display function OK, color coordinates within the control range of our company	
4	Low temperature work	Working condition of the product, test condition: -40℃, time 24H. After the test, the product is not removed, and the photoelectric parameters of the product are confirmed under this conditions. Check the product display function and appearance after removal and recovery to room temperature.	2pcs	Appearance OK, display function OK, color coordinates within the control range of our company	
5	Hot and cold impact	Test conditions:: -55 / 85℃ high and low temperature each maintained for 30mi n for one cycles, high and low temperature conversion time <5min, a total of 10 cycles. After the test, the product is returned to room temperature to confirm the situation.	2pcs	Appearance OK, display function OK, color coordinates within the control range of our company	
6	High temperature and high humidity cycle	A Cycle (24H) was tested for 10 cycles. 1, the experimental box was initially placed at 30℃ / 90% RH.2, the humidity is unchanged, 2H time temperature uniform speed rise to 60℃.3,60℃ / 90% RH, maintain 6H.4, the humidity is unchanged, and the temperature of 8H time is uniform to 30℃.5,30℃ / 90% RH, maintain 8H. During the process, a performance check was conducted within the last 4 hours of the 30℃ / 90% RH stage of the fifth cycleand the product was returned to room temperature and reconfirms the condition.	2pcs	Appearance OK, display function OK, color coordinates within the control range of our company	