

Project 2 Report

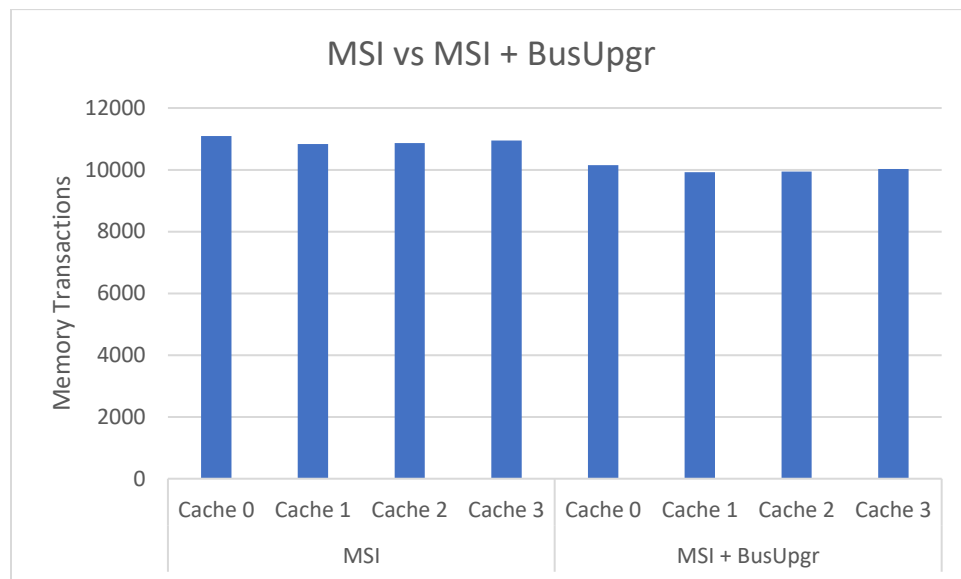
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From: Jacob Little
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Course: ECE 506 (001)
Topic: Project 2

Introduction:

This report compares the effectiveness of various cache coherency methods including MSI, MSI + BusUpgr, MESI, and MESI with a history filter with multiple configurations.

MSI vs MSI + BusUpgr:

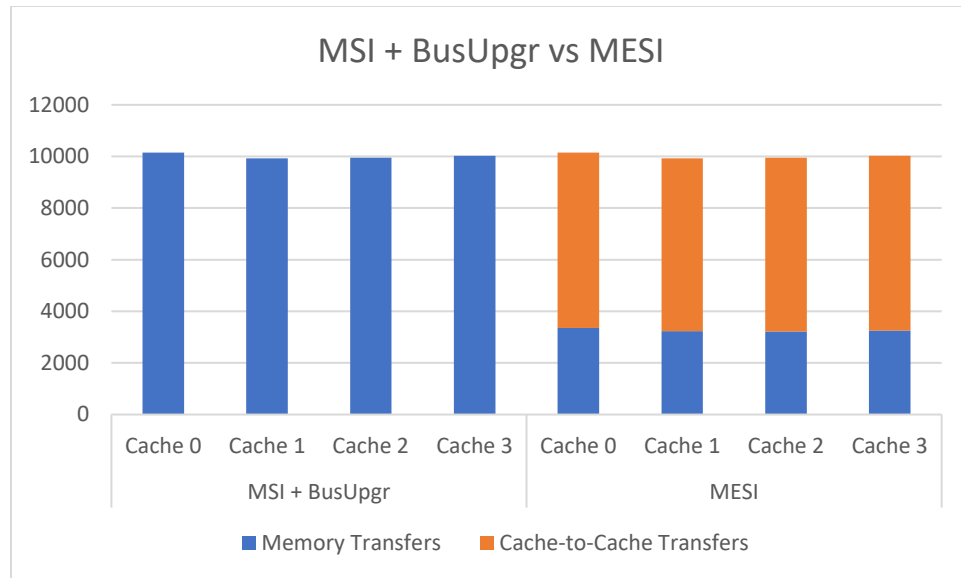
This chart compares MSI with and without the use of the BusUpgr bus transaction:



We see a reduced number of memory transaction with all caches with BusUpgr because we do not need to copy the requested block from memory when we go from the shared to modified states.

MSI + BusUpgr vs MESI:

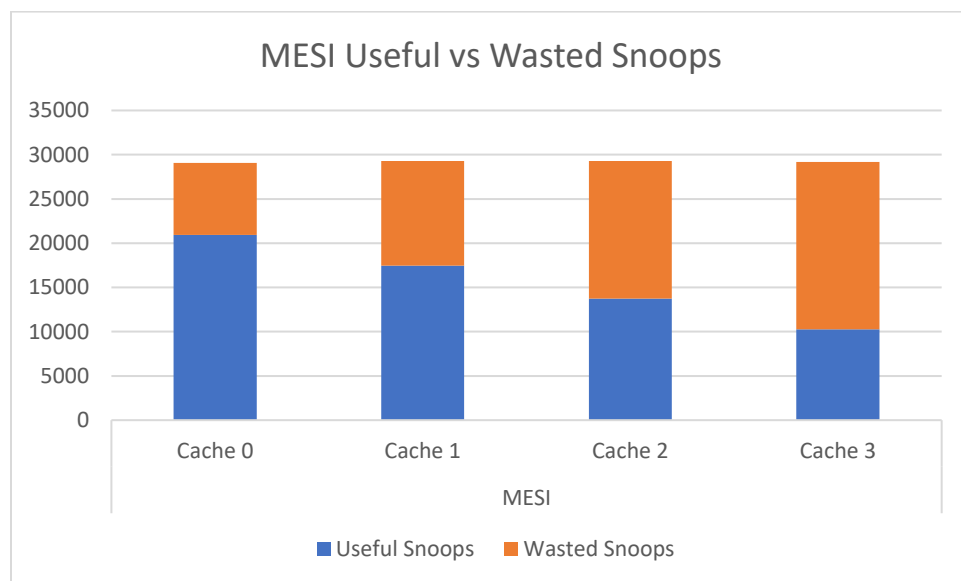
This chart compares MSI with BusUpgr and MESI:



Both protocols have the same total number of transfers, but a very large portion of the transfers in MESI are cache-to-cache which remove the need to reference main memory.

MESI Useful vs Wasted Snoops:

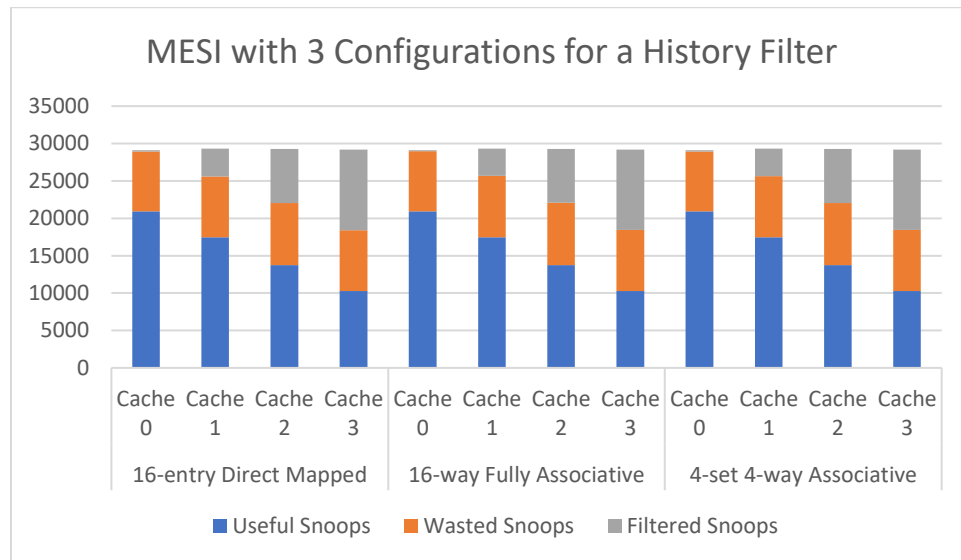
This chart demonstrates the number of useful and wasted snoops for each cache in MESI:



There are a lot of wasted snoops being performed that open an opportunity for optimization by attempting to filter those unnecessary snoops out.

MESI History Filter Configurations:

This chart compares three configurations for a history filter in the MESI protocol: 16-entry direct mapped, 16-way fully associative, and 4-set / 4-way associative.



For this trace, there does not appear to be much of a performance difference between the three configurations. Looking at the numbers more closely indicates that 16-entry direct mapped is optimal (filtering out the most wasted snoops), closely followed by 4-set / 4-way associative with 16-way fully associative being the least optimal. However, because the difference is so minute, it would probably be best to consider the complexity of implementing each configuration and choose the least complex for a real-world design assuming that this behavior continues for most other traces.