Exercise: Memory

Reference solutions

1. (1) Assume 32-bit main memory address, the total cache size in bits is 8 × (1 + 23 + 512) = 4288bits; Assume 16-bit main memory address, the total cache size in bits is 8 × (1 + 7 + 512) = 4160bits.

(2) 3200B/64B = 50, cache line index = 50 mod 8 =2.

1. (1) tag =8, index = 5, offset = 3

(2) a. line 3

b. line 6

c. line 3

d. line 21

1. Combined misses per instruction in I-Cache and D-Cache

1% + 30% \* 5% = 0.025 combined misses per instruction

Equal to 25 misses per 1000 instructions

Memory stall cycles

0.025 \* 100 = 2.5 stall cycles per instruction

Total memory stall cycles = 106 \* 2.5 = 2500000

1. Memory stalls per Instruction = 0.02\*100 + 0.2\*0.05\*100 = 3

CPIMemoryStalls = 1.5 + 3 = 4.5 cycles per instruction

CPIMemoryStalls / CPIPerfect = 4.5 /1.5 = 3

Processor is 3 times slower due to memory stall cycles

CPINoCache = 1.5 + (1 + 0.2) \* 100 = 121.5

CPINoCache / CPIPerfect = 121.5 / 1.5 = 81

Processor is 81 times slower if there is no cache

1. Assume the percent of the instructions having data memory access is X.

X \* 0.05 \* 100 + 1 = 1.5

X = 0.1

1. Read Mem [0x00005804]:

0000 5804 → 0000 0000 0000 0000 0101 1000 0000 0100

TAG: 0x000058

INDEX:0x1

RESULT: Hit

Read Mem [0x0000410C]:

0000 410C → 0000 0000 0000 0000 0100 0001 0000 1100

TAG: 0x000041

INDEX:0x3

RESULT: Miss

Read Mem [0x00005808]:

0000 4110 → 0000 0000 0000 0000 0100 0001 0001 1000

TAG: 0x000058

INDEX:0x2

Valid bit is 0

RESULT: Miss