**Exercise: Memory**

1. Suppose there is a byte addressable computer and a cache with 8 lines. Each cache line stores 64 byte data. Assume direct-mapped in the memory hierarchy. Calculate the following items.

(1) Assuming the memory address width is 32-bit/16-bit, compute the total cache size (in bits).

(2) The cache line index corresponding to the main memory address (3200)10

1. Consider a machine with a byte addressable main memory of 216 bytes and each cache line stores 8 bytes data. Assume that a direct-mapped cache consisting of 32 lines is used by this machine.

(1) How is a 16-bit memory address divided into tag, index, and offset?

(2) Into what line would bytes with each of the following addresses be stored?

a.0001 0001 0001 1011

b.1100 0011 0011 0100

c.1101 0000 0001 1101

d.1010 1010 1010 1010

1. Consider a program with the given characteristics:
   * Instruction count (IC) = 106 instructions
   * 30% of instructions need to access the data memory
   * Data cache miss rate is 5% and instruction cache miss rate is 1%
   * Miss penalty is 100 clock cycles for instruction and data caches

Compute the total number of cache misses (both instruction and data cache missed) per instruction and memory stall cycles

1. A processor has CPI of 1.5 if there is no cache miss

* Cache miss rate is 2% for instruction and 5% for data
  + 20% of instructions need to access the data memory
* Cache miss penalty is 100 clock cycles for I-cache and D-cache

Compute

1. The CPI if the memory stall (i.e., the cycles incurred by cache misses) is considered.
2. The CPI is both instruction cache and data caches are entirely removed (i.e., all memory accesses are misses).
3. How much slower are these two cases compared with the perfect situation with no cache misses?
4. Assume the CPI of a computer is 1 when all memory accesses are hits in the cache. Miss penalty is 100 cycles. The data cache miss rate is 5%. All instruction fetching were cache hits. What is the percentage of instructions having data memory accesses, so that the CPI of the computer is 1.5 in the presence of data cache misses?
5. Given a Direct-Mapped Caches (64 cache line). Answer the following questions based on the following graph. Each cache line stores 4 memory blocks.

* Is Read Mem [0x00005804] a hit?
* Is Read Mem [0x0000410C] a hit?
* Is Read Mem [0x00005808] a hit?

