Duration: 13 Sessions | Undergraduate Program | Winter 2023 | Department: Computer Science

Intro Assembly Lang & Op Sys

Instructor: Dr. Amin Safaei

Winter 2023

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Duration: 120 min | Undergraduate Program | Fall 2023 | Department: Computer Science

x86 Processor Architecture

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Winter 2023

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- **This set of lecture slides is made from the following textbooks:**
  - Barry B. Brey, The Intel Microprocessor: Architecture, Programming, and Interfacing, eight edition, Prentice Hall India, 2008.
  - M. A. Mazidi, R. D. McKinlay, J. G. Mazidi, 8051 Microcontroller, The: A Systems Approach
  - S. P. Dandamudi, Introduction to Assembly Language Programming For Pentium and RISC Processors
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2.1 Overview

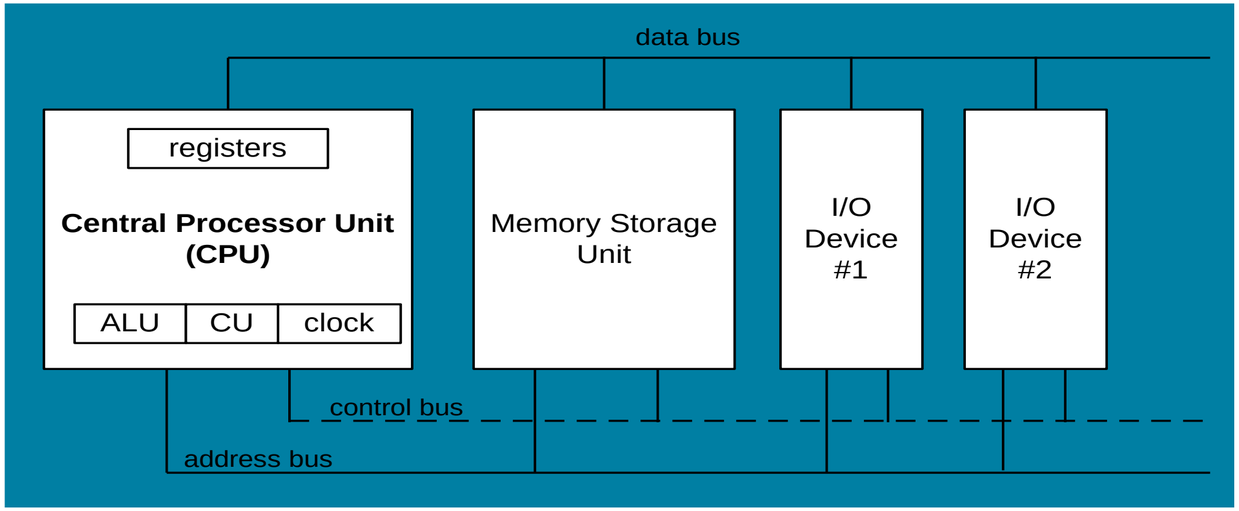
- **General Concepts**
- IA-32 Processor Architecture
- IA-32 Memory Management
- 64-bit Processors
- Components of an IA-32 Microcomputer
- Input-Output System

2.2 General Concepts

- Basic microcomputer design
- Instruction execution cycle
- Reading from memory
- How programs run

2.3 Basic Microcomputer Design

- Clock synchronizes CPU operations
- Control Unit (CU) coordinates sequence of execution steps
- ALU performs arithmetic and bitwise processing



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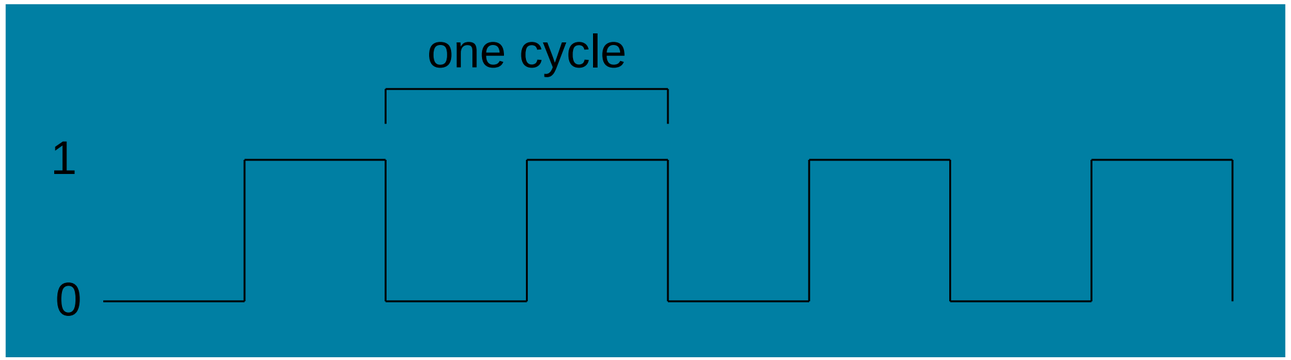
2.4 Clock

- Synchronizes all CPU and BUS operations
- Machine (clock) cycle measures time of a single operation
- Clock is used to trigger events



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2.1 Overview

- General Concepts
- **IA-32 Processor Architecture**
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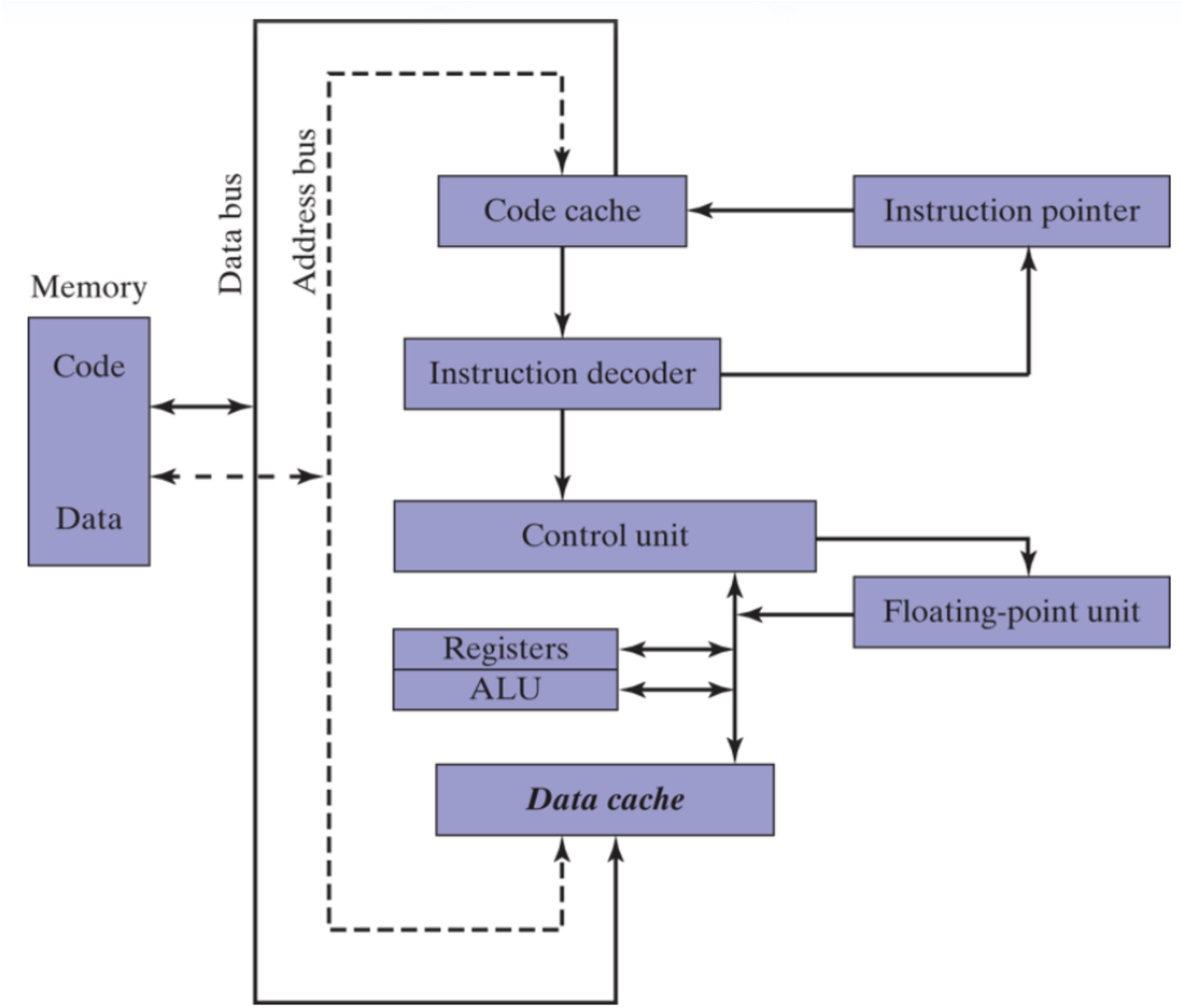
2.5 Instruction Execution Cycle

- Fetch
- Decode
- Fetch operands
- Execute
- Store output



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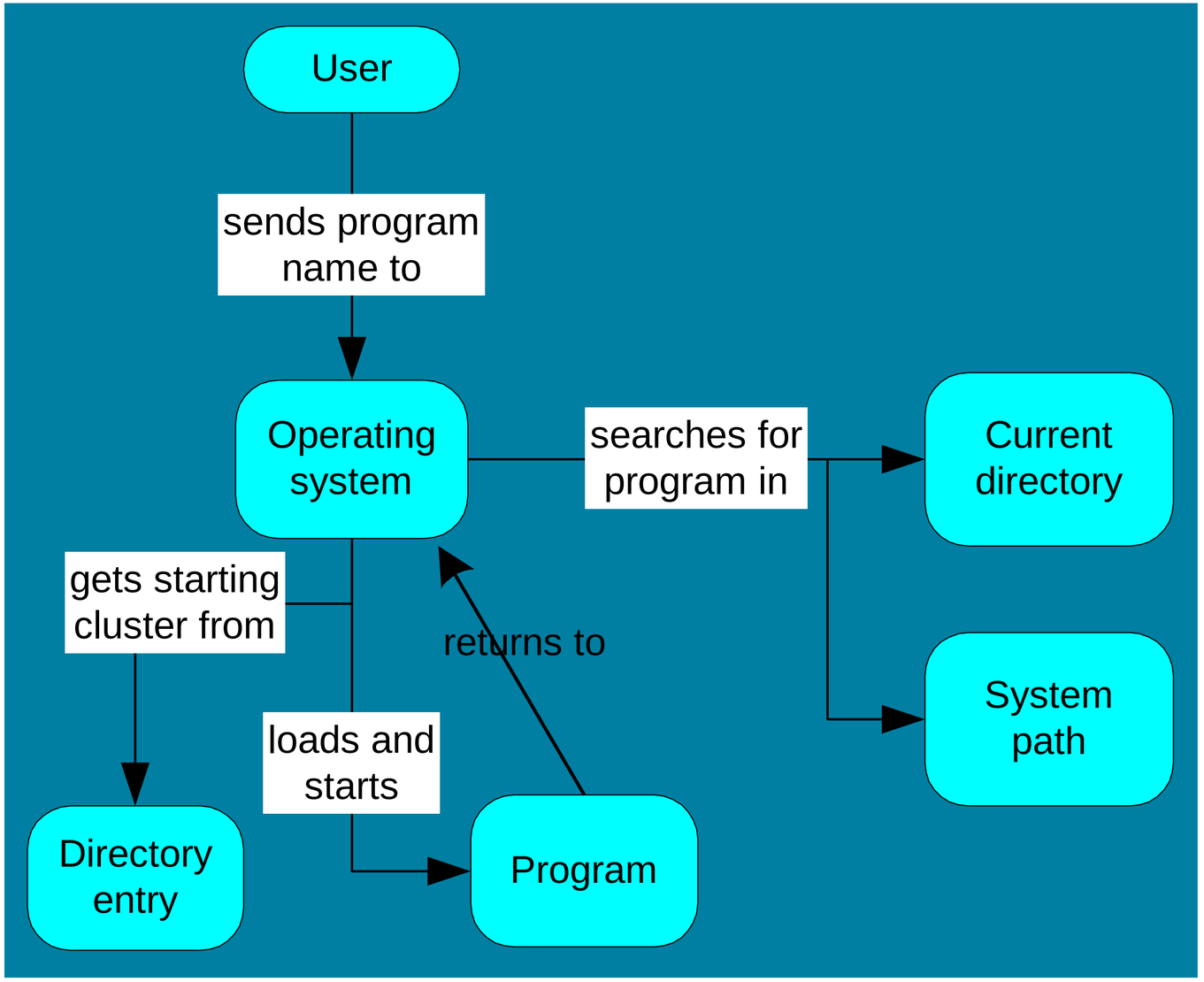
2.6 Reading from Memory

- Multiple machine cycles are required when reading from memory, because it responds much more slowly than the CPU. The steps are:
  1. Place the address of the value you want to read on the address bus.
  2. Assert (changing the value of) the processor's RD (read) pin.
  3. Wait one clock cycle for the memory chips to respond.
  4. Copy the data from the data bus into the destination operand

2.7 Cache Memory

- High-speed expensive static RAM both inside and outside the CPU.
  - Level-1 cache: inside the CPU
  - Level-2 cache: outside the CPU
- Cache hit: when data to be read is already in cache memory
- Cache miss: when data to be read is not in cache memory.

2.8 How a Program Runs



2.9 IA-32 Processor Architecture

- Modes of operation
- Basic execution environment
- Floating-point unit
- Intel Microprocessor history

2.10 Modes of Operation

- Protected mode
  - Native mode (Windows, Linux)
- Real-address mode
  - Native MS-DOS
- System management mode
  - Power management, system security, diagnostics
- Virtual-8086 mode
  - Hybrid of Protected
  - Each program has its own 8086 computer

2.11 Basic Execution Environment

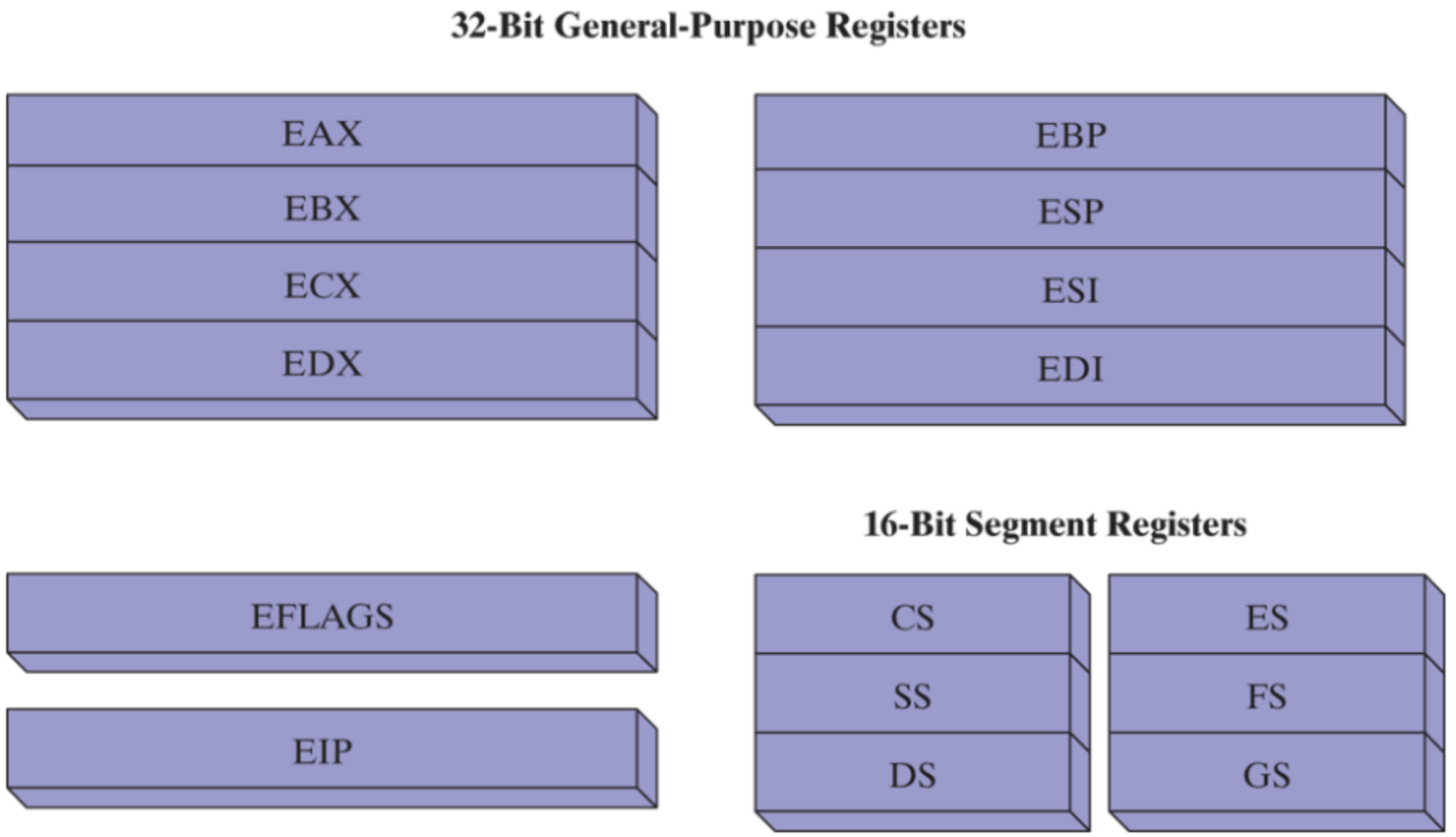
- Addressable memory
- General-purpose registers
- Index and base registers
- Specialized register uses
- Status flags
- Floating-point, MMX, XMM registers

2.12 Addressable Memory

- Protected mode
  - 4 GB
  - 32-bit address
- Real-address and Virtual-8086 modes
  - 1 MB space
  - 20-bit address

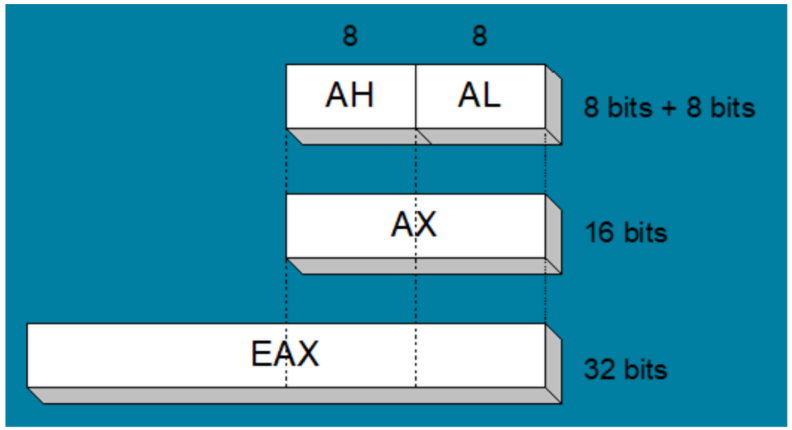
2.13 General-Purpose Registers

- Named storage locations inside the CPU, optimized for speed.



2.14 Accessing Parts of Registers

- Use 8-bit name,16-bit name, or 32-bit name
- Applies to EAX, EBX, ECX, and EDX



32-bit	16-bit	8-bit (high)	8-bit (low)
EAX	AX	AH	AL
EBX	BX	BH	BL
ECX	CX	CH	CL
EDX	DX	DH	DL

2.15 Index and Base Registers

- Some registers have only a 16-bit name for their lower half:

32-bit	16-bit
ESI	SI
EDI	DI
EBP	BP
ESP	SP

2.16 Some Specialized Register Uses

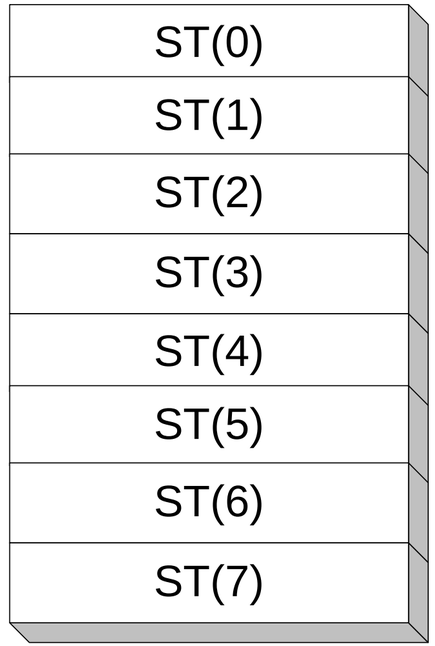
- **General-Purpose**
  - EAX – accumulator
  - ECX – loop counter
  - ESP – stack pointer
  - ESI, EDI – index registers
  - EBP – extended frame pointer (stack)
- **Segment**
  - CS – code segment
  - DS – data segment
  - SS – stack segment
  - ES, FS, GS – additional segments
  - EIP – instruction pointer
- **EFLAGS**
  - Status and control flags
  - Each flag is a single binary bit

2.17 Status Flags

- Carry
  - unsigned arithmetic out of range
- Overflow
  - signed arithmetic out of range
- Sign
  - result is negative
- Zero
  - result is zero
- Auxiliary Carry
  - carry from bit 3 to bit 4
- Parity
  - sum of 1 bits is an even number

2.18 Floating-Point, MMX, XMM Registers

- Eight 80-bit floating-point data registers
  - ST(0), ST(1), . . . , ST(7)
  - arranged in a stack
  - used for all floating-point arithmetic
- Eight 64-bit MMX registers
- Eight 128-bit XMM registers for single-instruction multiple-data (SIMD) operations



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- **IA-32 Memory Management**
- 64-bit Processors
- Components of an IA-32 Microcomputer
- Input-Output System

2.19 IA-32 Memory Management

- Real-address mode
- Calculating linear addresses
- Protected mode
- Multi-segment model
- Paging

2.20 Protected Mode

- 4 GB addressable RAM
  - (00000000 to FFFFFFFFh)
- Each program assigned a memory partition which is protected from other programs
- Designed for multitasking
- Supported by Linux & MS-Windows

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2.21 64-Bit Processors

- 64-Bit Operation Modes
  - Compatibility mode – can run existing 16-bit and 32-bit applications (Windows supports only 32-bit apps in this mode)
  - 64-bit mode – Windows 64 uses this
- Basic Execution Environment
  - addresses can be 64 bits (48 bits, in practice)
  - 16 64-bit general purpose registers
  - 64-bit instruction pointer named RIP

2.22 64-Bit General Purpose Registers

- 32-bit general purpose registers:
  - EAX, EBX, ECX, EDX, EDI, ESI, EBP, ESP, R8D, R9D, R10D, R11D, R12D, R13D, R14D, R15D
- 64-bit general purpose registers:
  - RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8, R9, R10, R11, R12, R13, R14, R15

Operand Size	Available Registers
8 bits	AL, BL, CL, DL, DIL, SIL, BPL, SPL, R8L, R9L, R10L, R11L, R12L, R13L, R14L, R15L
16 bits	AX, BX, CX, DX, DI, SI, BP, SP, R8W, R9W, R10W, R11W, R12W, R13W, R14W, R15W
32 bits	EAX, EBX, ECX, EDX, EDI, ESI, EBP, ESP, R8D, R9D, R10D, R11D, R12D, R13D, R14D, R15D
64 bits	RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8, R9, R10, R11, R12, R13, R14, R15

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- **Components of an IA-32 Microcomputer**
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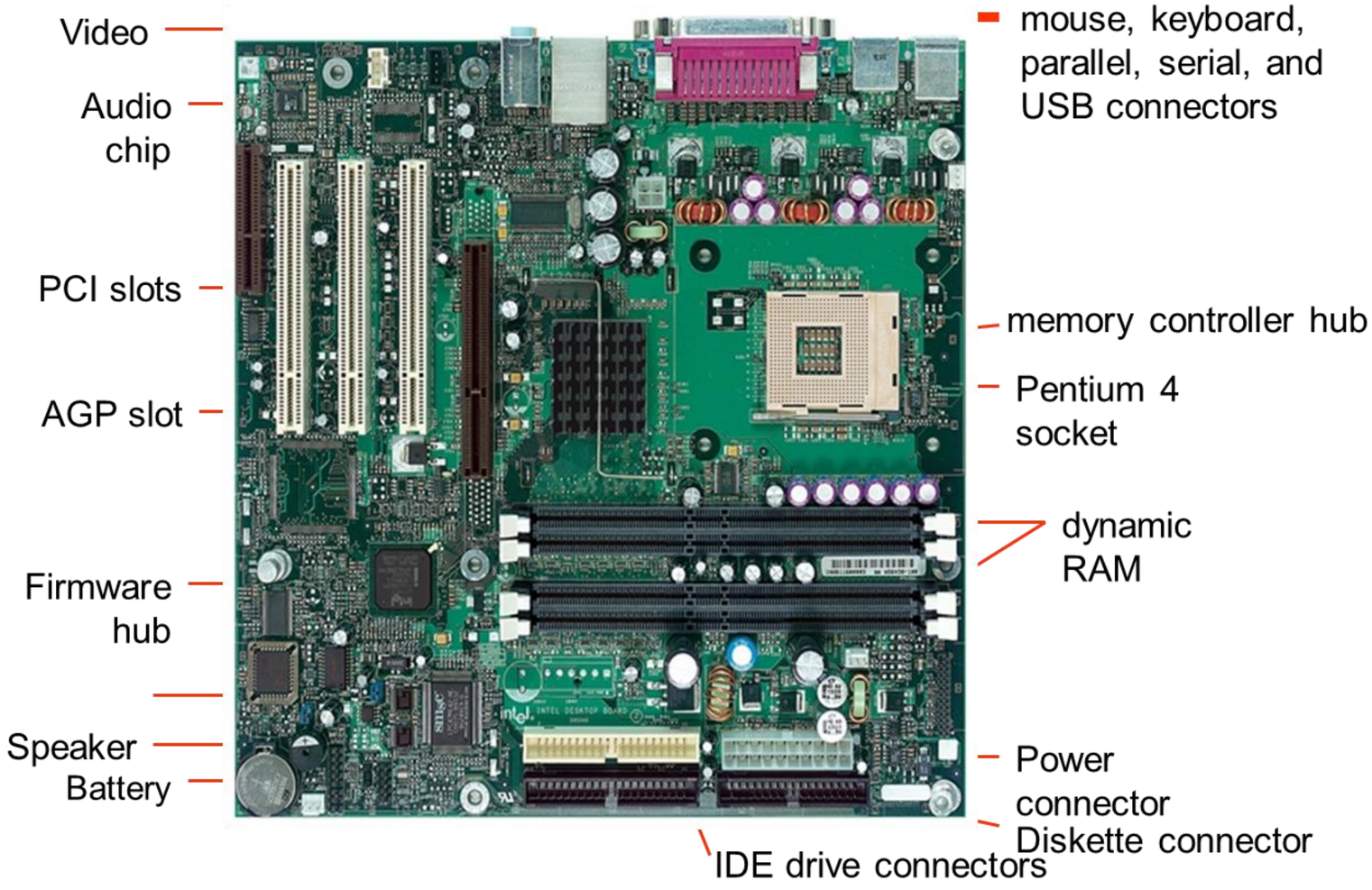
2.23 Components of an IA-32 Microcomputer

- Motherboard
- Video output
- Memory
- Input-output ports

2.24 Motherboard

- CPU socket
- External cache memory slots
- Main memory slots
- BIOS chips
- Sound synthesizer chip (optional)
- Video controller chip (optional)
- IDE, parallel, serial, USB, video, keyboard, joystick, network, and mouse connectors
- PCI bus connectors (expansion cards)

2.25 Intel D850MD Motherboard



Source: Intel® Desktop Board D850MD/D850MV Technical Product Specification

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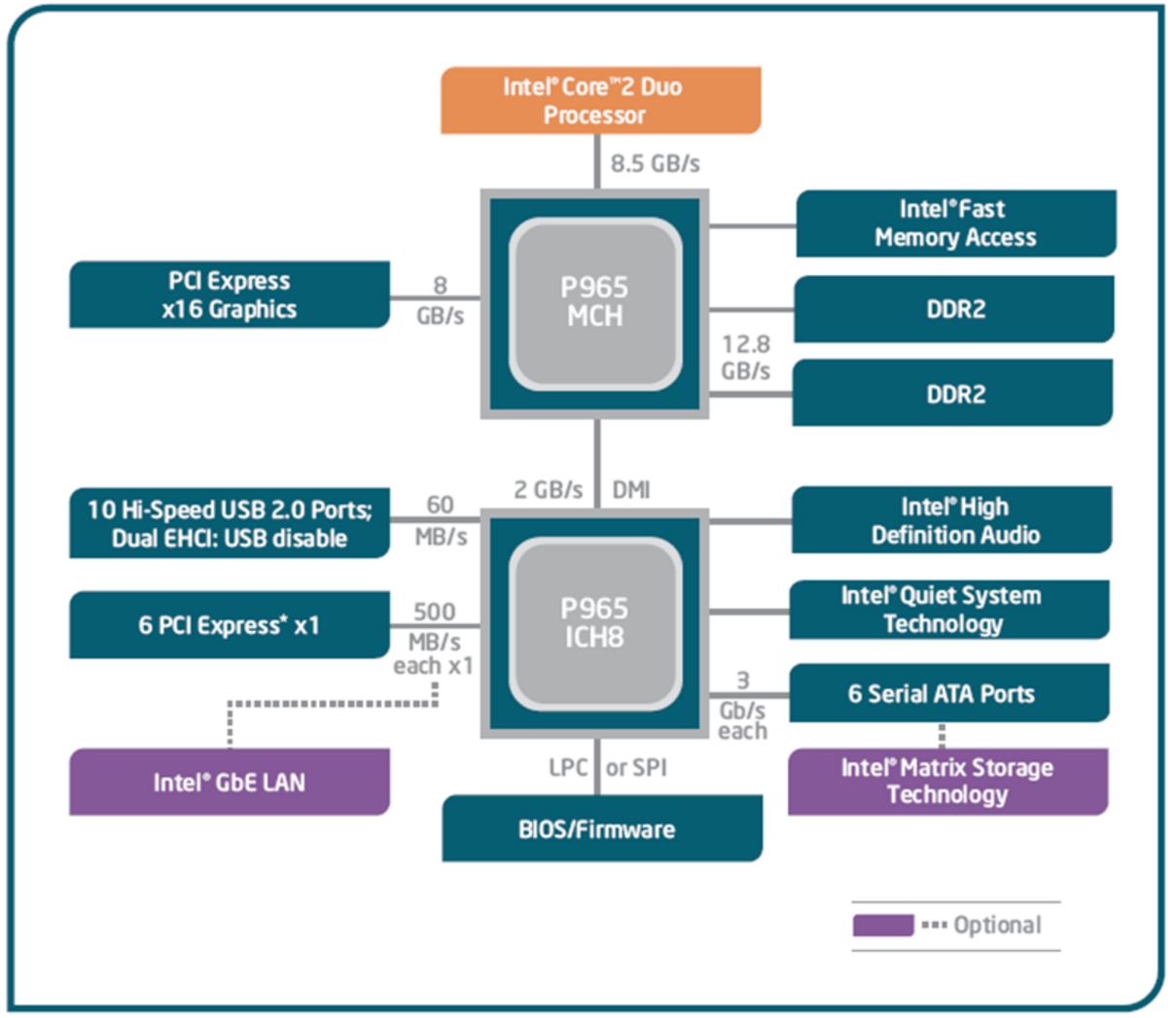
2.26 Intel 965 Express Chipset



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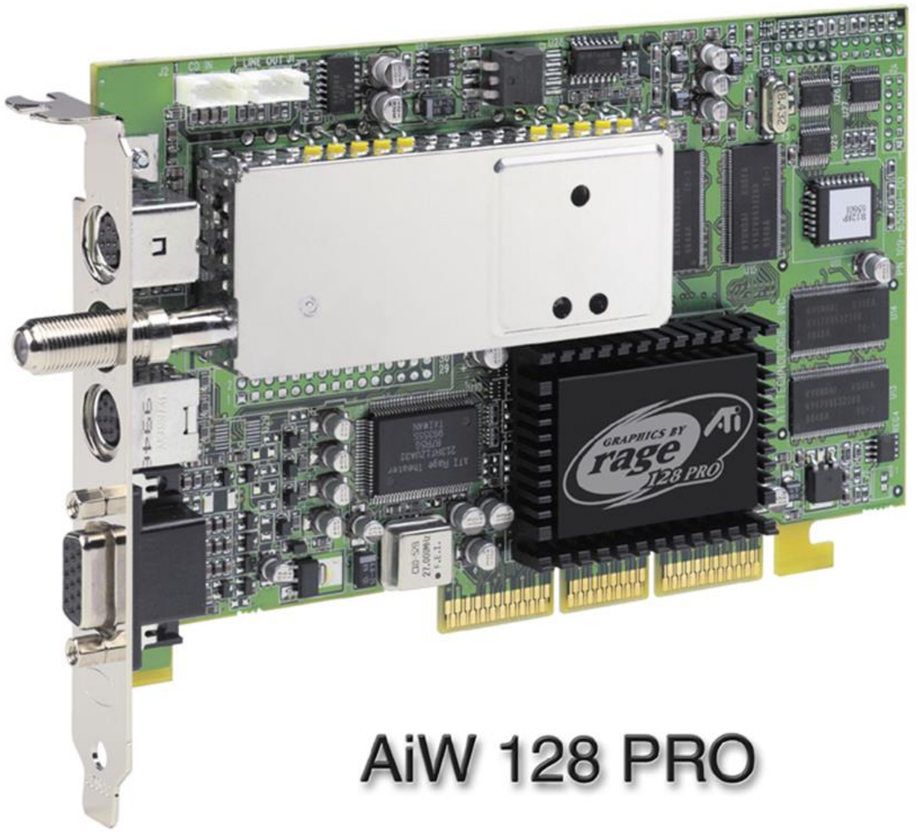
2.27 Video Output

- Video controller
  - On motherboard, or on expansion card
  - AGP (accelerated graphics port technology)
- Video memory (VRAM)
- Video CRT Display
  - Uses raster scanning
  - Horizontal retrace
  - Vertical retrace
- Direct digital LCD monitors
  - No raster scanning required

2.28 Sample Video Controller (ATI Corp.)

- 128-bit 3D graphics performance powered by RAGE™ 128 PRO
- 3D graphics performance
- Intelligent TV-Tuner with Digital VCR
- TV-ON-DEMAND™
- Interactive Program Guide
- Still image and MPEG-2 motion video capture
- Video editing
- Hardware DVD video playback
- Video output to TV or VCR



2.29 Memory

- ROM
  - Read Only Memory
- EPROM
  - Erasable Programmable Read Only Memory
- Dynamic RAM (DRAM)
  - inexpensive; must be refreshed constantly
- Static RAM (SRAM)
  - expensive; used for cache memory; no refresh required
- Video RAM (VRAM)
  - Dual ported; optimized for constant video refresh
- CMOS RAM
  - Complimentary metal-oxide semiconductor
  - System setup information

2.30 Input-Output Ports

- **USB (universal serial bus)**
  - Intelligent high-speed connection to devices
  - Up to 12 megabits/second
  - USB hub connects multiple devices
  - Enumeration: computer queries devices, supports hot connections
- **Parallel**
  - short cable, high speed
  - common for printers
  - bidirectional, parallel data transfer
  - Intel 8255 controller chip
- **Serial**
  - RS-232 serial port
  - One bit at a time
  - Uses long cables and modems
  - 16550 UART (universal asynchronous receiver transmitter)
  - Programmable in assembly language

2.31 Device Interfaces

- ATA host adapters
  - Intelligent drive electronics (hard drive, CDROM)
- SATA (Serial ATA)
  - Inexpensive, fast, bidirectional
- FireWire
  - high speed (800 MB/sec), many devices at once
- Bluetooth
  - Small amounts of data, short distances, low power usage
- Wi-Fi (wireless Ethernet)
  - IEEE 802.11 standard, faster than Bluetooth

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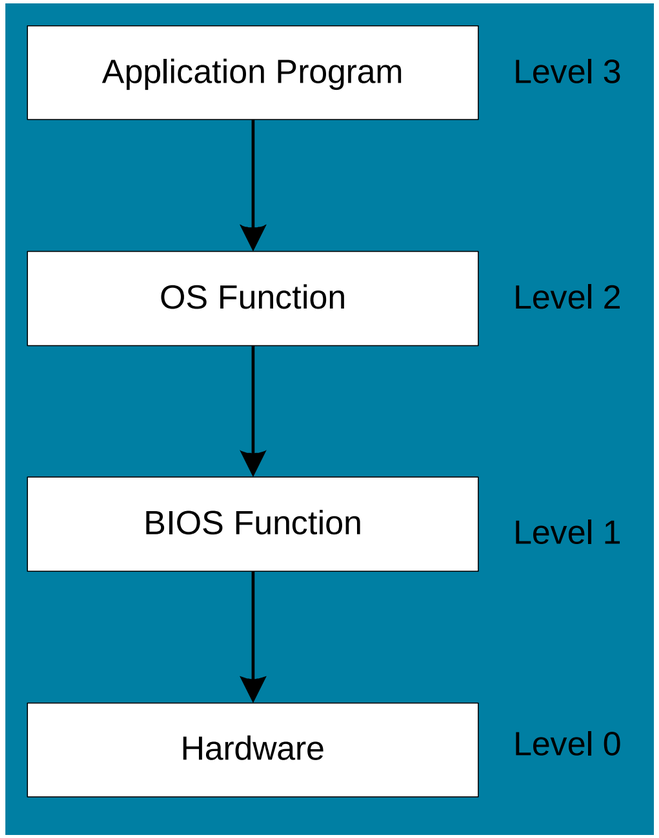
2.32 Levels of Input-Output

- **Level 3:** High-level language function
  - Examples: C++, Java
  - Portable, convenient, not always the fastest
- **Level 2:** Operating system
  - Application Programming Interface (API)
  - Extended capabilities, lots of details to master
- **Level 1:** BIOS
  - Drivers that communicate directly with devices
  - OS security may prevent application-level code from working at this level

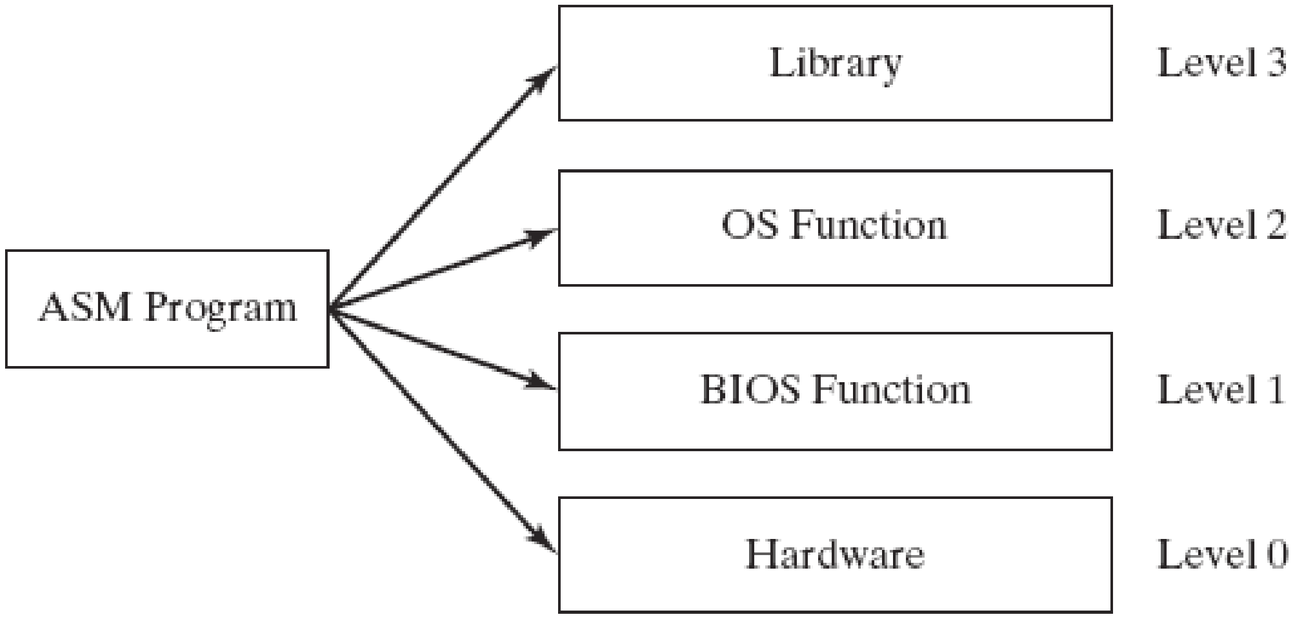
2.33 Displaying a String of Characters

- When a HLL program displays a string of characters, the following steps take place:



2.34 Programming levels

- Assembly language programs can perform input-output at each of the following levels:



2.35 Summary

- Central Processing Unit (CPU)
- Arithmetic Logic Unit (ALU)
- Instruction execution cycle
- Multitasking
- Floating Point Unit (FPU)
- Complex Instruction Set
- Real mode and Protected mode
- Motherboard components
- Memory types
- Input/Output and access levels