data sheet

MH32F103A(C)xxxx

Enhanced, True Random Number, Hardware Encryption Algorithm Unit, 32-bit Core Microcontroller with 128K Bytes to 256K Bytes Flash USB, CAN, 17 Timers, 3 ADCs, 2 DACs, 15 Communication Interfaces

Function:

- Kernel: 32-bit Core
  - Up to 216MHz operating frequency, up to 2.54DMips/MHz (CoreMark1.0)
  - Single-cycle multiplication and hardware division
- memory (unit)
  - 128K/256K/512K/1024K bytes of flash programme memory
  - 32K/64K/96K bytes of SRAM
  - FSMC Static Memory Controller
- Clock, Reset and Power Management
  - 2.0 to 3.6 volt power supply and I/O pins
  - Power On/Power Off Reset (POR/PDR), Programmable Voltage Monitor (PVD)
  - 4～32MHz Crystal Oscillator
  - Embedded factory-tuned 8MHz RC oscillator
  - Embedded 40kHz RC oscillator with calibration
  - 32kHz RTC oscillator with calibration function
- low power
  - Sleep, shutdown and standby modes
  - VBAT supplies power to the RTC and back-up registers
- 3 x 12-bit analogue-to-digital converters with 1us conversion time (up to 16 input channels)
  - Conversion range: 0 to 3.6V
  - Three sets of sample and hold functions
  - temperature sensor
- 2 x 12-bit D/A converters
- DMA: 12-channel DMA controller
  - Supported Peripherals: Timer, ADC, DAC, SDIO SPI, I2S, I2C and USART
- debug mode
  - Serial Single Wire Debug (SWD) and JTAG interfaces
  - Embedded Tracking Module (ETM)
- Up to 51 I/O ports
  - 51 multifunctional bi-directional I/O ports, all of which can be mapped to 16 external interrupts
  - All GPIOs can be forced to configure pull-up and pull-down resistors
- Enhanced CRC Calculation Unit

- 17 timers
  - 10 16-bit timers, each with up to 4 channels for input capture/output compare/PWM or pulse counting and incremental encoder inputs
  - 2 x 16-bit PWM advanced control timers with deadband control and emergency brake for motor control
  - 2 watchdog timers (stand-alone and window type)
  - System time timer: 24-bit self-subtracting counter
  - 2 16-bit basic timers

- Up to 13 communication interfaces
  - Up to 2 I2C interfaces (SMBus/PMBus support)
  - Up to 5 USART interfaces (supports ISO7816, LIN, IrDA interface and modem control)
  - Up to 3 SPI interfaces
    Up to 3 SPI interfaces, 2 with I2S interface multiplexing
  - CAN interface (2.0B active)
  - USB 2.0 full-speed interface (optional internal 1.5K pull-up resistor)
  - SDIO interface

- Hardware encryption algorithm unit
  - Built-in hardware algorithms (DES, AES, SHA, SM1, SM3, SM4, SM7)
  - Provides a complete library of high-performance algorithms

- TRNG: The TRNG unit is used to generate a sequence of true random numbers
  - Four independent true random sources, individually configurable
  - Generates 128BIT random numbers at a time
  - Optional digital post-processing function
  - Attack detection

- SENSOR: Voltage Temperature Sensor Alarm
  - VBAT and VDD voltages can be detected separately
  - Provision of temperature detection sensors
  - Optional reset or interrupt after alarm

- SRAM scrambling
  - Supports address and data scrambling

- One Time Programmable (OTP)
  - Supports 32 Byte

- AES encrypted download (supported by some models):
  - HEX encrypted with AES can be downloaded and decrypted by hardware.
    - Support area encryption, decryption function

MH32F103A(C)xxxx Datasheet

directory (on computer hard drive)

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Figure catalogue

1 present (sb for a job etc)

The contents of the datasheet include the basic configuration of the product (e.g., the capacity of the built-in Flash and RAM, the type and number of peripheral modules, etc.), the number and assignment of pins, electrical characteristics, package information, and ordering codes.

2 Specification

The MH32F103A(C)xxxx series uses a high-performance 32-bit core and operates at a maximum frequency of 216 MHz.

. Built-in memory includes: Maximum 1024K Flash, 96K Sram

The series has up to 2 built-in advanced timers, 10 general-purpose timers, 2 basic timers, 3 12-bit ADCs, 2 12-bit DACs, and also includes standard and advanced communication interfaces including: 3 SPI interfaces, 2 I2S interfaces, 2 I2C interfaces, 5 U(S)ART interfaces, 1 USB2.0 full-speed serial communication interface, 1 CAN bus controller, 1 SDIO interface

The MH32F103A(C)xxxx family operates over a temperature range of -40°C to +85°C with a supply voltage of 2.0 V to 3.6 V. The power-saving mode ensures that low-power applications are required.

Thanks to these peripheral configurations, the MH32F103A(C)xxxx can be used in a variety of application scenarios:

- Industrial applications such as programmable controllers, printers, scanners, etc.
- Motor drives and speed control
- IoT low-power sensor terminals, e.g., sports bracelets
- UAV flight control, gimbal control
- Toy products
- domestic electric appliance
- intelligent robot
- smartwatch

Device List

Table 1 Device Function Configuration Table

range		MH32F103C	MH32F103A			
model number		CBT6	CCT6	RPT6	VET6	VGT6
Flash memory (K bytes)		128	256	256	512	1024
SRAM (K bytes)		32	64	96	96	96
timed (of explosive etc) tool	high level	1	1	2	2	2
	common (use)	4	4	10	10	10
	fundamental	2	2	2	2	2
communications interface	SPI	3	3	3	3	3
	I2S	-	-	2	2	2
	I2C	2	2	2	2	2
	USART/UART	3	3	5	5	5
	USB	1	1	1	1	1
	CAN	1	1	1	1	1
	SDIO	-	-	1	1	1
FSMC		-	-	-	1	1
GPIO port		37	37	51	80	80
12-bit ADC Module (Number of Channels)		2 (10 channels)	2 (10 channels)	3 (16 channels)	3 (16 channels)	3 (16 channels)
12-Bit DAC Module (Number of Channels)		2 (2 channels)	2 (2 channels)	2 (2 channels)	2 (2 channels)	2 (2 channels)
Random number module		adjuvant				
Hardware encryption algorithm unit		adjuvant				
Page size (K bytes)		2	2	2	2	4
CPU frequency		216M				
operating voltage		2.0~3.6V				
operating temperature		-40 to +85℃				
Package form		LQFP48		LQFP64	LQFP100	

outlined

2.1.1 32-bit Core with embedded Flash and SRAM

The 32-bit Core provides the low-cost platform, reduced pin count, and reduced system power consumption needed to implement an MCU, while delivering superior computational performance and advanced interrupt system response.

2.1.2 internal flash memory

Maximum 256K internal flash memory for storing programmes and data. Table 2 Relationship between supply voltage and Flash delay level

Flash Delay	HCLK(MHz)			
hierarchy	1	2	2	
	Voltage Range		Voltage Range	

	2.3V - 3.6V	2.0V - 2.3V
0	0 < HCLK <= 108	0 < HCLK <= 32
1	108 < HCLK <= 216	32 < HCLK <= 64
2	-	64 < HCLK <= 128
3	-	128 < HCLK <= 192
4	-	192 < HCLK <= 216

2.1.3 Memory Protection Unit (MPU)

The Memory Protection Unit (MPU) is used to manage CPU accesses to memory and prevent one task from accidentally corrupting memory or resources used by another active task. The memory is organised into up to 8 protection zones, which can be subdivided sequentially into up to 8 sub-zones. The size of the protected areas can range from 32 bytes to the entire 4 Gbytes of addressable memory.

The MPU is particularly useful if the application has some critical or authenticated code that must be protected from the misbehaviour of other tasks. It is usually managed by an RTOS (Real Time Operating System). If a programme accesses a memory location that is forbidden by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the settings of the MPU area based on the executing process.

2.1.4 Internal SRAM internal flash memory

Up to 96K bytes of internal SRAM that can be accessed (read/write) by the CPU with 0 wait cycles.

2.1.5 Static memory controller (FSMC)

The following modes are supported: PC Card/Flash, SRAM,
PSRAM, NOR and NAND. function overview:

- Three FSMC interrupt lines through logic or connected to NVIC units
- Write to FIFO
- Code execution from external memories

other than NAND flash and PC card For VET6,
only FSMC Bank1 and Bank2 are available.
Bank1 can only support NOR/PSRAM memory, use NE1
selector chip. Bank2 can only support 16/8-bit NAND
flash memory, use NCE2 selector chip.

2.1.6 LCD Parallel Interface

The FSMC can be configured to interface seamlessly with most graphics LCD controllers. It supports Intel 8080 and Motorola 6800 modes and is flexible enough to accommodate specific LCD interfaces.

2.1.7 CRC (Cyclic Redundancy Check) calculation unit

The CRC (Cyclic Redundancy Check) calculation unit generates a CRC code from a 32-bit data word using a fixed polynomial (multiple modes selectable with hardware data processing) generator.

In numerous applications, the CRC-based technique is used to verify the consistency of data transfer or storage. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting errors in flash memory.

2.1.8 Nested Vector Interrupt Controller (NVIC)

Built-in nested vectorial interrupt controller capable of handling up to 71 maskable interrupt channels (excluding 16 Core interrupt lines) and 8 priority levels.

- Tightly coupled NVICs enable low-latency interrupt response processing
- Interrupt vector entry address directly into the kernel
- Tightly coupled NVIC interface
- Allow early processing of interrupts
- Handling late arriving higher priority interrupts
- Support for interrupting the tail link function
- Automatic saving of processor state
- Auto-resume on return from interrupt, no additional instruction overhead required

The module provides flexible interrupt management capabilities with minimal interrupt latency.

2.1.9 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains 19 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its triggering event (rising or falling edge or double edge) and can be individually masked; there is a pending register that maintains the status of all interrupt requests.EXTI can detect pulse widths less than the clock period of the internal APB2. Up to 80 general-purpose I/O port connections can be connected to 16 external interrupt lines.

2.1.10 Clock and start-up

The selection of the system clock is done at startup, the internal 8MHz RC oscillator is selected as the default CPU clock at reset, and an external, failure-monitored 4-32MHz clock can be selected later; when an external clock failure is detected, it is isolated, and the system automatically switches to the internal RC oscillator, and the software receives the appropriate interrupts if they are enabled. Similarly, full interrupt management of the PLL clock can be taken when required (e.g. when an indirectly used external oscillator fails).

Multiple prescalers are used to configure the frequency of the AHB, the high-speed APB (APB2), and the low-speed APB (APB1) regions.The maximum frequency of the AHB and high-speed APB is 216 MHz, and

the maximum frequency of the low-speed APB is 108 MHz.

2.1.11 activation mode

At startup, one of three bootstrap modes can be selected via the bootstrap pin:

- Bootstrapping from Program Flash Memory
- bootstrap from system memory
- Bootstrapping from internal SRAM

The bootloader is stored in system memory and can be reprogrammed to flash memory via USART1.

2.1.12 Power supply programme

- VDD: Supplies power to the I/O pins and internal regulator.
- VSSA, VDDA: Provides power to the analogue parts of the ADC, reset module, RC oscillator and PLL.VDDA and VSSA must be connected to VDD and VSS respectively.
- VBAT: When VDD is turned off, power is supplied (via the internal power switcher) to the RTC, external 32kHz oscillator, and back-up registers.

Note: For each voltage range, refer to Table 9 General Operating Conditions.

2.1.13 Power supply monitor

This product has an internal Power-On Reset (POR)/Power-Down Reset (PDR) circuit, which is always in operation to ensure that the system operates when the power supply exceeds 2V; when VDD falls below the set threshold (VPOR/PDR), it puts the device in reset without the need to use an external reset circuit. There is also a programmable voltage monitor (PVD) in the device, which monitors the VDD/VDDA supply and compares it to the threshold VPVD, generating an interrupt when VDD is below or above the threshold VPVD, and an interrupt handler that can issue a warning message or put the microcontroller into safe mode. the PVD function needs to be enabled programmatically.

2.1.14 Voltage regulator

The regulator has three modes of operation: main mode (MR), low power mode (LPR) and shutdown mode

- Main mode (MR) for normal runtime operations
- Low power mode (LPR) for CPU shutdown mode
- Shutdown mode is used in the standby mode of the CPU: the output of the regulator is high resistance, the power supply to the kernel circuits is cut off, and the regulator is in a zero-consumption state (but the contents of the registers and SRAM will be lost)

The regulator is always active after reset and switches off in standby mode at the high resistance output.

2.1.15 low power mode

- sleep mode

  In sleep mode, only the CPU is stopped, and all peripherals are active and can wake up the CPU in case of an interrupt/event.

- shutdown mode

The shutdown mode achieves the lowest power consumption while maintaining no loss of SRAM and register contents. In shutdown mode, power supply to all internal 1.1V sections is stopped, the PLL, the RC oscillator of the HSI, and the HSE crystal oscillator are switched off, and the regulator can be placed in the

Normal mode or low power mode.

The microcontroller can be woken up from shutdown mode by any of the signals configured as EXTI, which can be one of the 16 external I/O ports, the output of the PVD, an RTC alarm clock, or a USB wake-up signal.

- standby mode

The lowest power consumption can be achieved in standby mode. The internal voltage regulator is switched off, so that the power supply to all internal 1.1V sections is cut off; the PLL, the RC oscillator of the HSI and the HSE crystal oscillator are also switched off; when entering standby mode, the contents of the SRAM and registers are lost, but the contents of the backup registers remain, and the standby circuits are still working. The conditions for exiting from standby mode are an external reset signal on NRST, an IWDG reset, a rising edge on the WKUP pin, or the arrival of an alarm clock on the RTC.

Note: RTC, IWDG and the corresponding clock will not be stopped when entering stop or standby mode.

2.1.16 DMA

Supports up to 12 channels of general-purpose DMA (7 channels for DMA1 and 5 channels for DMA2) can manage memory-to-memory, device-to-memory, and memory-to-device data transfers; the DMA controller supports ring-buffer management, avoiding interrupts generated when the controller transfer reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, while each channel can be triggered by software; the length of the transfer, the source and destination address of the transfer can be set individually by software. DMA can be used for major peripherals: SPI/I2S, I2C, USART, advanced/general/basic timer TIMx, ADC, DAC, SDIO.

2.1.17 RTC (Real Time Clock) and Backup Registers

The RTC and back-up registers are powered through a switch that selects VDD power when VDD is active, otherwise they are powered by the VBAT pin. The back-up registers (42 16-bit registers) can be used to hold 84 bytes of user application data when VDD is turned off.The RTC and back-up registers are not reset by the system or power supply reset source; nor are they reset when woken up from standby mode.

The real time clock has a set of continuously running counters, a calendar clock function that can be provided by appropriate software, and an alarm interrupt and phase interrupt function.The RTC's drive clock can be a 32.768kHz oscillator using an external crystal, an internal low power RC oscillator, or a high speed external clock divided by 128. The internal low-power RC oscillator has a typical frequency of 40 kHz, and to compensate for deviations from the natural crystal, the RTC's clock can be calibrated by outputting a signal at 512 Hz. The RTC has a 32-bit programmable counter, and long-time measurements can be made using a comparison register. There is a 20-bit prescaler for the time base clock, which by default generates a 1-second long time reference when the clock is 32.768kHz.

2.1.18 Timers and Watchdogs

This series contains up to 2 advanced control timers, 4 normal timers, 2 basic timers, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of the Advanced Control Timer, Normal Timer, and Basic Timer:

Table 3 TIM Configuration Table

timers	counter	Counter Type	presharing factor	Generate DMA request	Capture/Compare Channel	complementary output
TIM1	16-bit	Up, down.	Between 1 and 65536	possible	4	there are

TIM8		Up/Down	any integer of			
TIM2 TIM3 TIM4 TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536.	possible	4	hasn't
TIM9 TIM12	16-bit	try to improve oneself	Any integer between 1 and 65536.	may not	2	hasn't
TIM10 TIM11 TIM13 TIM14	16-bit	try to improve oneself	Any integer between 1 and 65536.	may not	1	hasn't
TIM6 TIM7	16-bit	try to improve oneself	Any integer between 1 and 65536.	possible	0	hasn't

Advanced Control Timer (TIM1 and TIM8)

The two advanced control timers (TIM1 and TIM8) can be viewed as three-phase PWM generators assigned to six channels with complementary PWM outputs with deadband insertion, and can also be treated as complete general purpose timers. Four independent channels can be used:

- Input Capture
- Output Comparison
- Generate PWM (edge or centre aligned mode)
- Single pulse output

When configured as a 16-bit standard timer, it has the same functionality as the TIMx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0 to 100%).

In debug mode, the counter can be frozen while the PWM outputs are disabled, thus cutting off the switches controlled by these outputs.

Many of the features are the same as the standard TIM timer, and the internal structure is the same, so the Advanced Control Timer can operate in concert with the TIM timer through the timer linking feature, which provides synchronisation or event linking functionality.

General purpose timers (TIM2, TIM3, TIM4, TIM5)

Four standard timers (TIM2, TIM3, TIM4, TIM5) that can run synchronously are built into this series. Each timer has a 16-bit auto-loading increment/decrement counter, a 16-bit prescaler, and four independent channels, each of which can be used for input capture, output comparison, PWM, and single pulse mode output. They can also work in conjunction with advanced control timers via the timer link function, providing synchronisation or event linking. The counters can be frozen in debug mode. Any of the standard timers can be used to generate PWM

outputs. Each timer has an independent DMA request mechanism.
These timers are also capable of handling signals from incremental encoders
and also digital outputs from 1 to 3 Hall sensors. General purpose timers
(TIM10, TIM11, TIM9)
These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler.The TIM10 and TIM11 have a separate channel, while the TIM9 has two separate channel outputs for input capture/output comparison, PWM or mono-pulse modesThey can be synchronised with the TIM2, TIM3,TIM4,andTIM5 full-featured synchronised general purpose timers. They can also be used as simple time bases.
General purpose timers (TIM13, TIM14, TIM12)
These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler.TIM13 and TIM14 have a separate channel, while TIM12

There are two independent channels for input capture/output comparison, PWM or mono-pulse mode with independent channel outputs they can be used with TIM2,TIM3,
TIM4 and TIM5 full function synchronised general purpose
timers. They can also be used as simple time bases. Independent
Watchdog
The stand-alone watchdog is based on a 12-bit decrement counter and an 8-bit prescaler, which is clocked by an internal, independent 40kHz RC oscillator; because this RC oscillator is independent of the main clock, it can operate in shutdown and standby modes. It can be used as a watchdog to reset the entire system in the event of a problem, or as a free timer to provide timeout management for the application. The option byte can be configured to be a software or hardware initiated watchdog. In debug mode the counter can be frozen.

Basic Timers TIM6 and TIM7
These timers are primarily used for DAC trigger generation. They can
also be used as a general purpose 16-bit time base. Window
Watchdog
The window watchdog contains a 7-bit decrementing counter and can be set to run freely. It can be used as a watchdog to reset the whole system in the event of a problem. It is driven by the master clock and has an early warning interrupt; the counter can be frozen in debug mode. System time base timer

This timer is dedicated to real-time operating systems and can also be used as a standard decrementing counter. It has the following characteristics:

- 24-bit Decrementing Counter
- Auto-reload function
- Generates a maskable system interrupt when the counter is 0.
- Programmable Clock Source

2.1.19 I2C bus

Up to 2 I2C bus interfaces, capable of operating in multi-master or slave mode, supporting standard and fast modes.The I2C interfaces support 7-bit or 10-bit addressing, and dual-slave address addressing in 7-bit slave mode. Built-in hardware CRC generator/checker.

They can use DMA operation and support SMBus bus version 2.0/PMBus bus.

2.1.20 Universal Synchronous/Asynchronous Transceiver (USART)

Three general-purpose synchronous/asynchronous transceivers (USART1, USART2 and USART3) and two general-purpose asynchronous receive transmitters (UART4 and UART5). These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and LIN master/slave functionality.

The USART1 interface communicates at rates up to 13.5 megabits per second.

The USART1, USART2 and USART3 interfaces feature hardware CTS and RTS signal management, ISO7816-compatible smart card mode and SPI-like communication mode.

2.1.21 Serial Peripheral Interface (SPI)

Up to 3 SPI interfaces with full and half duplex communication rates up to 30 Mbit/s in slave or master mode. 3-bit prescaler generates 8 master mode frequencies configurable to 8 or 16 bits per frame. Hardware CRC generation/checksum support for basic SD card and MMC modes.

All SPI interfaces can use DMA operation.

2.1.22 Audio Interface (I2S)

The two standard I2S interfaces (multiplexed with SPI2 and SPI3) can be operated in master or slave mode, and can be configured for 16-bit or 32-bit transfers, as well as for input or output channels, and support audio sampling from 8kHz to 48kHz. when either or both I2S interfaces are configured as master mode, its master clock can be output to an external DAC or CODEC (decoder) at a frequency of 256 times the sampling frequency. When either or both I2S interfaces are configured as master mode, its master clock can be output to an external DAC or CODEC at 256 times the sample rate.

2.1.23 SDIO

The SD/SDIO/MMC host interface can support three different data bus modes: 1-bit (default), 4-bit, and 8-bit in the MMC card system specification version 4.2. The SDIO memory card specification version 2.0 supports two data bus modes: 1-bit (default) and 4-bit. Current chip versions can only support one SD/SDIO/MMC version 4.2 card at a time, but can support multiple MMC version 4.1 or earlier cards simultaneously.

With the exception of SD/SDIO/MMC, this interface is fully compatible with the CE-ATA digital protocol version 1.1.

2.1.24 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active) and has a bit rate of up to 1 megabit per second. It can receive and send standard frames with 11-bit identifiers or extended frames with 29-bit identifiers. Has 3 transmit mailboxes and 2 receive FIFOs, 3 stages with 14 adjustable filters.

2.1.25 Universal Serial Bus (USB)

Embedded a full-speed USB-compatible device controller that follows the full-speed USB device (12 megabits/second) standard, with software-configurable endpoints and standby/wakeup functionality.The USB-specific 48MHz clock is generated directly from the internal master PLL (clock source can be arbitrary).

2.1.26 General Purpose Input Output Interface (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (with or without pull-up or pull-down), or a multiplexed peripheral function port. Most GPIO pins are shared with digital or analogue multiplexed peripherals. All GPIO pins have high-current pass-through capability, except for ports with analogue input functions.

Where required, the peripheral functions of the I/O pins can be locked by a specific operation to avoid accidental writes to the I/O registers. Each I/O can be configured with forced pull-up

and pull-down resistors to save external resistor consumption.

2.1.27 ADC (analogue/digital converter)

Up to three 12-bit analogue/digital converters (ADCs), each sharing up to 16 external channels, are supported for single or scanning conversions. In scan mode, conversion is performed automatically on a selected set of analogue inputs.

Other logical functions on the ADC interface include:

- Synchronised sample and hold
- Cross sample and hold
- Single Sampling

The ADC can use DMA operation.

The analogue watchdog function allows very precise monitoring of one, several or all selected channels, generating an interrupt when the monitored signal exceeds a preset threshold.

Events generated by the standard timers (TIMx) and advanced control timers (TIM1 and TIM8) can be internally cascaded to the ADC start trigger and injection trigger, respectively, and the application program can synchronise the AD conversion with the clock.

2.1.28 DAC (digital/analogue signal converter)

Two 12-bit buffered DAC channels can be used to convert two digital signals into two analogue voltage signals and output them. This dual digital interface supports the following functions:

- Two DAC converters: one output channel each
- 8-bit or 12-bit monotonic output
- Left and right data alignment in 12-bit mode
- Synchronised update function
- create a noise wave
- generate a triangle wave
- Dual DAC channels convert independently or synchronously
- DMA function available for each channel
- External trigger for conversion
- Input reference voltage V REF+

The DAC channel can be triggered by the update output of the timer, and the update output can also be connected to a different DMA channel.

2.1.29 temperature sensor

The temperature sensor produces a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of ADC1_IN16, which is used to convert the output of the sensor to a digital value.

2.1.30 Serial single wire JTAG debug port (SWJ-DP)

The embedded SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging, enables the connection of either a serial single-wire debugging interface or a JTAG interface.The TMS and TCK signals of the JTAG share the same pins with SWDIO and SWCLK, respectively, and a special sequence of signals on the TMS pin is used to toggle between JTAG-DP and SW-DP.

2.1.31 Embedded Tracking Module (ETM)

Using an embedded trace microcell (ETM) connected to an external trace port analysis (TPA) device

via few ETM pins, a compressed stream of data is output from the CPU core at high speed, providing developers with clear information about instruction operation and data flow.The TPA device can be connected to a debug host via USB, Ethernet, or other high-speed channel, and real-time instruction and data flow Real-time instruction and data flow can be recorded by the debug software on the debug host and displayed in the desired format.TPA hardware can be purchased from development tool vendors and is compatible with third-party debug software.

2.1.32 True Random Number Generator (TRNG)

The TRNG unit is used to generate a sequence of true random numbers. A 128-bit true random number sequence is generated in a single operation. Configurable to generate a CPU interrupt request after random number generation.

3 Pin Definitions

LQFP48 package

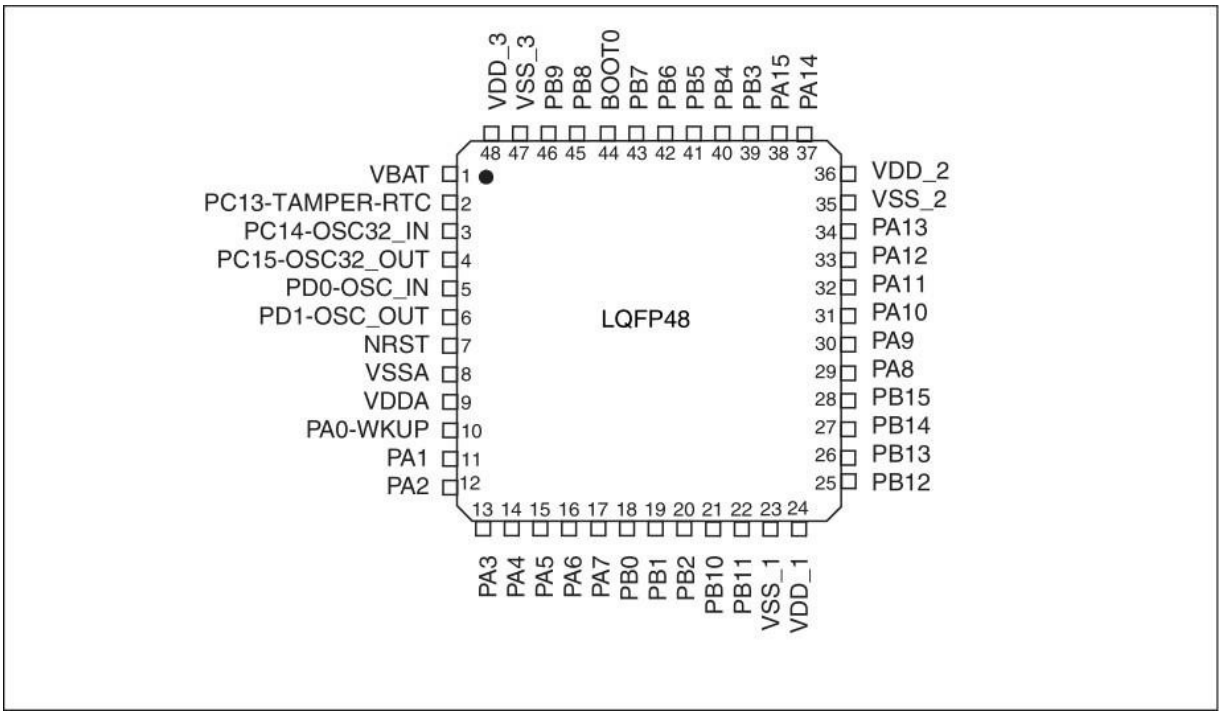


Figure 1 LQFP48 Package

LQFP64 package

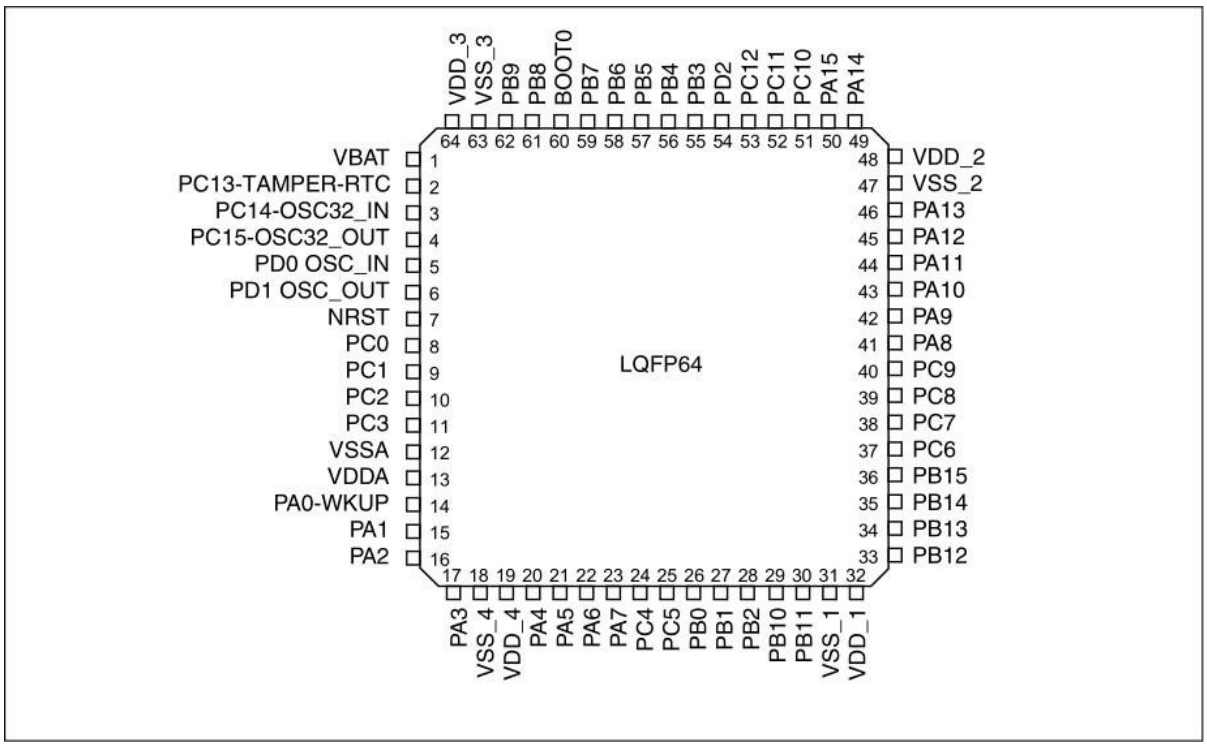


Figure 2 LQFP64 Package

LQFP100 package

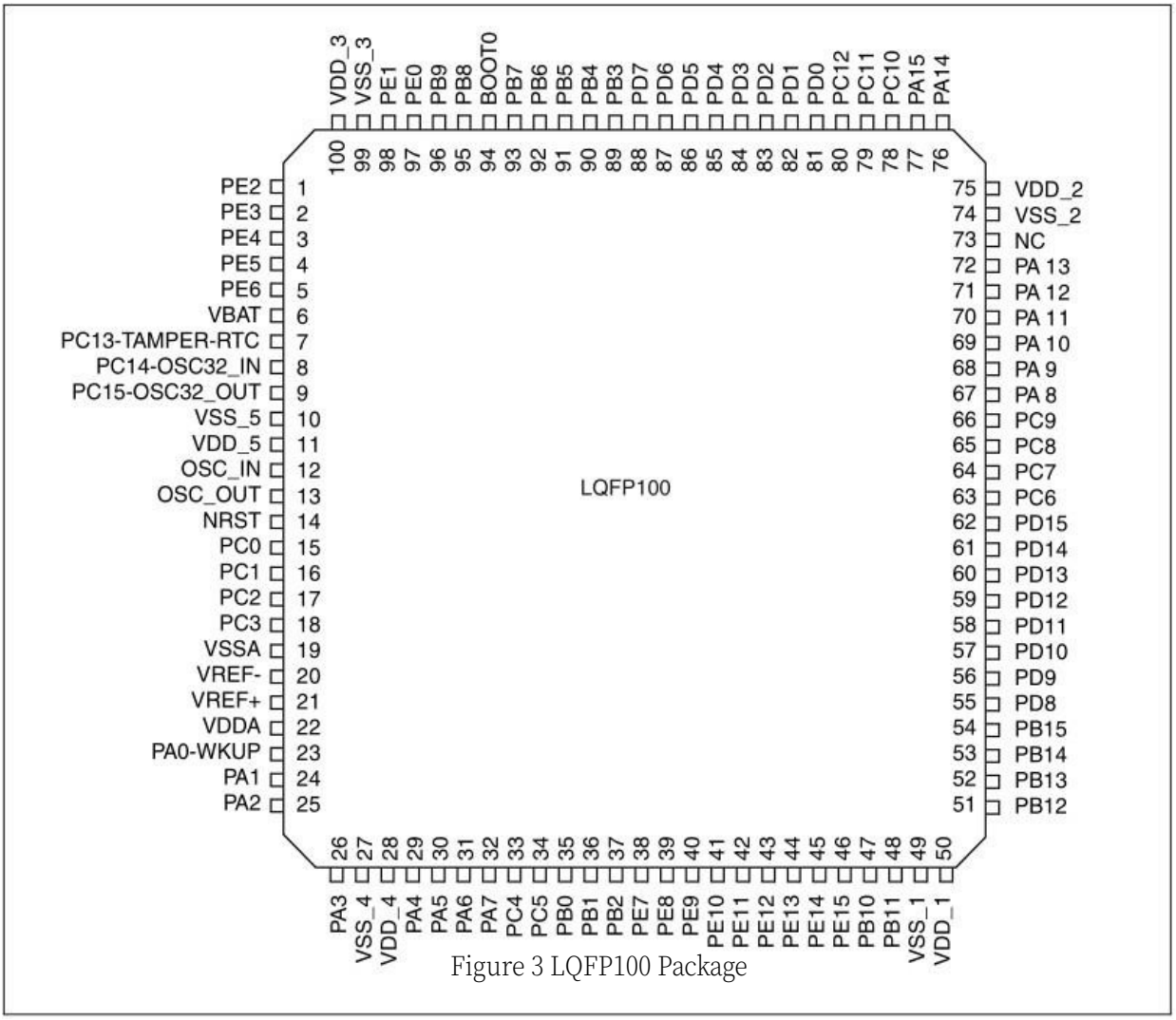


Figure 3 LQFP100 Package

LQFP48 Pin Definition

Table 4 LQFP 48 Pin Definition Configuration Table

LQFP 48	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	VBAT	S	–	VBAT	–	–
2	PC13-TAMPERRTC	I/O	–	PC13	TAMPER-RTC	–
3	PC14-OSC32_IN	I/O	–	PC14	OSC32_IN	–
4	PC15-OSC32_OUT	I/O	–	PC15	OSC32_OUT	–
5	OSC_IN	I/O	–	OSC_IN	–	PD0
6	OSC_OUT	I/O	–	OSC_OUT	–	PD1
7	NRST	I/O	–	NRST	–	–
8	VSSA	S	–	VSSA	–	–
9	VDDA	S	–	VDDA	–	–
10	PA0-WKUP	I/O	–	PA0	WKUP/USART2_CTS/ adc12_in0/tim2_ch1_etr/	–

					TIM5_CH1	
11	PA1	I/O	–	PA1	usart2_rts/adc12_in1/ TIM2_CH2/TIM5_CH2	–
12	PA2	I/O	–	PA2	usart2_tx/adc12_in2/ TIM2_CH3/TIM5_CH3/	–
13	PA3	I/O	–	PA3	usart2_rx/adc12_in3/ tim2_ch4/tim5_ch4/	–
14	PA4	I/O	–	PA4	spi1_nss/usart2_ck/ DAC_OUT1/ADC12_IN4	–
15	PA5	I/O	–	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	–
16	PA6	I/O	–	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1	TIM1_BKIN
17	PA7	I/O	–	PA7	spi1_mosi/adc12_in7/ TIM3_CH2	TIM1_CH1N
18	PB0	I/O	–	PB0	ADC12_IN8/TIM3_CH3	TIM1_CH2N
19	PB1	I/O	–	PB1	ADC12_IN9/TIM3_CH4	TIM1_CH3N
20	PB2	I/O	FT	PB2/BOOT1	–	–
21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
23	VSS_1	S	–	VSS_1	–	–
24	VDD_1	S	–	VDD_1	–	–
25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ usart3_ck/tim1_bkin	–
26	PB13	I/O	FT	PB13	spi2_sck/usart3_cts/ TIM1_CH1N	–
27	PB14	I/O	FT	PB14	spi2_miso/usart3_rts/ TIM1_CH2N	–
28	PB15	I/O	FT	PB15	spi2_mosi/tim1_ch3n	–
29	PA8	I/O	FT	PA8	usart1_ck/tim1_ch1/ MCO	–
30	PA9	I/O	FT	PA9	usart1_tx/tim1_ch2	–
31	PA10	I/O	FT	PA10	usart1_rx/tim1_ch3	–
32	PA11	I/O	–	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	–
33	PA12	I/O	–	PA12	usart1_rts/usbdp/ CAN_TX/TIM1_ETR	–
34	PA13	I/O	FT	JTMS-SWDIO	–	PA13
35	VSS_2	S	–	VSS_2	–	–
36	VDD_2	S	–	VDD_2	–	–
37	PA14	I/O	FT	JTCK-SWCLK	–	PA14
38	PA15	I/O	FT	JTDI	SPI3_NSS	tim2_ch1_etr/pa15/ SPI1_NSS
39	PB3	I/O	FT	JTDO	SPI3_SCK	TIM2_CH2/PB3/ TRACESWO/SPI1_SCK
40	PB4	I/O	FT	NJTRST	SPI3_MISO	TIM3_CH1/PB4/ SPI1_MISO
41	PB5	I/O	–	PB5	I2C1_SMBA/ SPI3_MOSI	TIM3_CH2/SPI1_MOSI
42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
44	BOOT0	I	–	BOOT0	–	–
45	PB8	I/O	FT	PB8	TIM4_CH3	I2C1_SCL/CAN_RX
46	PB9	I/O	FT	PB9	TIM4_CH4	I2C1_SDA/CAN_TX

47	VSS_3	S	–	VSS_3	–	–
48	VDD_3	S	–	VDD_3	–	–

(1) FT = 5V tolerance

LQFP64 Pin Definition

Table 5 LQFP 64 Pin Definition Configuration Table

LQFP 64	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	VBAT	S	–	VBAT	–	–
2	PC13-TAMPERRTC	I/O	–	PC13	TAMPER-RTC	–
3	PC14-OSC32_IN	I/O	–	PC14	OSC32_IN	PD0
4	PC15-OSC32_OUT	I/O	–	PC15	OSC32_OUT	PD1
5	OSC_IN	I/O	–	OSC_IN	–	–
6	OSC_OUT	I/O	–	OSC_OUT	–	–
7	NRST	I/O	–	NRST	–	–
8	PC0	I/O	–	PC0	ADC123_IN10	–
9	PC1	I/O	–	PC1	ADC123_IN11	–
10	PC2	I/O	–	PC2	ADC123_IN12	–
11	PC3	I/O	–	PC3	ADC123_IN13	–
12	VSSA	S	–	VSSA	–	–
13	VDDA	S	–	VDDA	–	–
14	PA0-WKUP	I/O	–	PA0	wkup/usart2_cts/ adc123_in0/tim2_ch1_etr/ tim5_ch1/tim8_etr	–
15	PA1	I/O	–	PA1	usart2_rts/adc123_in1/ TIM2_CH2/TIM5_CH2	–
16	PA2	I/O	–	PA2	usart2_tx/adc123_in2/ tim2_ch3/tim5_ch3/ TIM9_CH1	–
17	PA3	I/O	–	PA3	usart2_rx/adc123_in3/ tim2_ch4/tim5_ch4/ TIM9_CH2	–
18	VSS_4	S	–	VSS_4	–	–
19	VDD_4	S	–	VDD_4	–	–
20	PA4	I/O	–	PA4	spi1_nss/usart2_ck/ DAC_OUT1/ADC12_IN4	–
21	PA5	I/O	–	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	–
22	PA6	I/O	–	PA6	spi1_miso/adc12_in6/ tim3_ch1/tim8_bkin/ TIM13_CH1	TIM1_BKIN
23	PA7	I/O	–	PA7	spi1_mosi/adc12_in7/ tim3_ch2/tim8_ch1n/ TIM14_CH1	TIM1_CH1N
24	PC4	I/O		PC4	ADC12_IN14	–
25	PC5	I/O		PC5	ADC12_IN15	–
26	PB0	I/O	–	PB0	ADC12_IN8/TIM3_CH3/ TIM8_CH2N	TIM1_CH2N
27	PB1	I/O	–	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
28	PB2	I/O	FT	PB2/BOOT1	–	–

29	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
30	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
31	VSS_1	S	–	VSS_1	–	–
32	VDD_1	S	–	VDD_1	–	–
33	PB12	I/O	FT	PB12	spi2_nss/i2s2_ws/ i2C2_smba/usart3_ck/ TIM1_BKIN	–
34	PB13	I/O	FT	PB13	spi2_sck/i2s2_ck/ usart3_cts/tim1_ch1n	–
35	PB14	I/O	FT	PB14	spi2_miso/tim1_ch2n usart3_rts/tim12_ch1	–
36	PB15	I/O	FT	PB15	spi2_mosi/i2s2_sd/ tim1_ch3n/tim12_ch2	–
37	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1/ SDIO_D6	TIM3_CH1
38	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2/ SDIO_D7	TIM3_CH2
39	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
40	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
41	PA8	I/O	FT	PA8	usart1_ck/tim1_ch1/ MCO	–
42	PA9	I/O	FT	PA9	usart1_tx/tim1_ch2	–
43	PA10	I/O	FT	PA10	usart1_rx/tim1_ch3	–
44	PA11	I/O	–	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	–
45	PA12	I/O	–	PA12	usart1_rts/usbdp/ CAN_TX/TIM1_ETR	–
46	PA13	I/O	FT	JTMS-SWDIO	–	PA13
47	VSS_2	S	–	VSS_2	–	–
48	VDD_2	S	–	VDD_2	–	–
49	PA14	I/O	FT	JTCK-SWCLK	–	PA14
50	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS	TIM2_CH1_ETR/PA15/ SPI1_NSS
51	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
52	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
53	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
54	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	
55	PB3	I/O	FT	JTDO	SPI3_SCK/I2S3_CK	PB3/TRACESWO TIM2_CH2/SPI1_SCK
56	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4/TIM3_CH1/ SPI1_MISO
57	PB5	I/O	–	PB5	I2C1_SMBA/SPI3_MOSI /I2S3_SD	TIM3_CH2/SPI1_MOSI
58	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
59	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
60	BOOT0	I	–	BOOT0	–	–
61	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_D4/ TIM10_CH1	I2C1_SCL/CAN_RX
62	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_D5/ TIM11_CH1	I2C1_SDA/CAN_TX
63	VSS_3	S	–	VSS_3	–	–
64	VDD_3	S	–	VDD_3	–	–

(1) FT = 5V tolerance

LQFP100 Pin Definition

Table 6 LQFP 100 Pin Definition Configuration Table

LQFP 64	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	PE2	I/O	FT	PE2	FSMC_A23	–
2	PE3	I/O	FT	PE3	FSMC_A19	–
3	PE4	I/O	FT	PE4	FSMC_A20	–
4	PE5	I/O	FT	PE5	FSMC_A21	–
5	PE6	I/O	FT	PE6	FSMC_A22	–
6	VBAT	S	–	VBAT	–	–
7	PC13-TAMPERRTC	I/O	–	PC13	TAMPER-RTC	–
8	PC14-OSC32_IN	I/O	–	PC14	OSC32_IN	–
9	PC15-OSC32_OUT	I/O	–	PC15	OSC32_OUT	–
10	VSS_5	S	–	VSS_5	–	
11	VDD_5	S	–	VDD_5	–	
12	OSC_IN	I/O	–	OSC_IN	–	–
13	OSC_OUT	I/O	–	OSC_OUT	–	–
14	NRST	I/O	–	NRST	–	–
15	PC0	I/O	–	PC0	ADC123_IN10	–
16	PC1	I/O	–	PC1	ADC123_IN11	–
17	PC2	I/O	–	PC2	ADC123_IN12	–
18	PC3	I/O	–	PC3	ADC123_IN13	–
19	VSSA	S	–	VSSA	–	–
20	Vref-	S	–	Vref-	–	–
21	Vref+	S	–	Vref+	–	–
22	VDDA	S	–	VDDA	–	–
23	PA0-WKUP	I/O	–	PA0	wkup/usart2_cts/ adc123_in0/tim2_ch1_etr/ tim5_ch1/tim8_etr	–
24	PA1	I/O	–	PA1	usart2_rts/adc123_in1/ TIM2_CH2/TIM5_CH2	–
25	PA2	I/O	–	PA2	usart2_tx/adc123_in2/ tim2_ch3/tim5_ch3/ TIM9_CH1	–
26	PA3	I/O	–	PA3	usart2_rx/adc123_in3/ tim2_ch4/tim5_ch4/ TIM9_CH2	–
27	VSS_4	S	–	VSS_4	–	–
28	VDD_4	S	–	VDD_4	–	–
29	PA4	I/O	–	PA4	spi1_nss/usart2_ck/ DAC_OUT1/ADC12_IN4	–
30	PA5	I/O	–	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	–
31	PA6	I/O	–	PA6	spi1_miso/adc12_in6/ tim3_ch1/tim8_bkin/ TIM13_CH1	TIM1_BKIN
32	PA7	I/O	–	PA7	spi1_mosi/adc12_in7/ tim3_ch2/tim8_ch1n/ TIM14_CH1	TIM1_CH1N
33	PC4	I/O		PC4	ADC12_IN14	–

34	PC5	I/O		PC5	ADC12_IN15	–
35	PB0	I/O	–	PB0	ADC12_IN8/TIM3_CH3/ TIM8_CH2N	TIM1_CH2N
36	PB1	I/O	–	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
37	PB2	I/O	FT	PB2/BOOT1	–	–
38	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
39	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
40	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
41	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
42	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
43	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
44	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
45	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
46	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
47	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
48	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
49	VSS_1	S	–	VSS_1	–	–
50	VDD_1	S	–	VDD_1	–	–
51	PB12	I/O	FT	PB12	spi2_nss/i2s2_ws/ i2C2_smba/usart3_ck/ TIM1_BKIN	–
52	PB13	I/O	FT	PB13	spi2_sck/i2s2_ck/ usart3_cts/tim1_ch1n	–
53	PB14	I/O	FT	PB14	spi2_miso/tim1_ch2n usart3_rts/tim12_ch1	–
54	PB15	I/O	FT	PB15	spi2_mosi/i2s2_sd/ tim1_ch3n/tim12_ch2	–
55	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1/USART3_RX
60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
63	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1/ SDIO_D6	TIM3_CH1
64	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2/ SDIO_D7	TIM3_CH2
65	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
66	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
67	PA8	I/O	FT	PA8	usart1_ck/tim1_ch1/ MCO	–
68	PA9	I/O	FT	PA9	usart1_tx/tim1_ch2	–
69	PA10	I/O	FT	PA10	usart1_rx/tim1_ch3	–
70	PA11	I/O	–	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	–
71	PA12	I/O	–	PA12	usart1_rts/usbdp/ CAN_TX/TIM1_ETR	–
72	PA13	I/O	FT	JTMS-SWDIO	–	PA13
73	Not Connected					–
74	VSS_2	S	–	VSS_2	–	–
75	VDD_2	S	–	VDD_2	–	–

76	PA14	I/O	FT	JTCK-SWCLK	–	PA14
77	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS	TIM2_CH1_ETR/PA15/ SPI1_NSS
78	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
79	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
80	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
81	PD0	I/O	FT	PD0	FSMC_D2	CAN_RX
82	PD1	I/O	FT	PD1	FSMC_D3	CAN_TX
83	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	–
84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
87	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
88	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK
89	PB3	I/O	FT	JTDO	SPI3_SCK/I2S3_CK	PB3/TRACESWO TIM2_CH2/SPI1_SCK
90	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4/TIM3_CH1/ SPI1_MISO
91	PB5	I/O	–	PB5	I2C1_SMBA/SPI3_MOSI /I2S3_SD	TIM3_CH2/SPI1_MOSI
92	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
93	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2 / FSMC_NADV	USART1_RX
94	BOOT0	I	–	BOOT0	–	–
95	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_D4/ TIM10_CH1	I2C1_SCL/CAN_RX
96	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_D5/ TIM11_CH1	I2C1_SDA/CAN_TX
97	PE0	I/O	FT	PE0	TIM4_ETR/FSMC_NBL0	–
98	PE1	I/O	FT	PE1	FSMC_NBL1	–
99	VSS_3	S	–	VSS_3	–	–
100	VDD_3	S	–	VDD_3	–	–

(1) FT = 5V tolerance

4 Electrical Characteristics

test condition

All voltage's are referenced to VSS unless otherwise noted.

4.1.1 Minimum and maximum values

Unless otherwise stated, all minimum and maximum values will be guaranteed at the worst ambient temperature, supply voltage and clock frequency conditions by tests performed on 100% of the products at ambient temperature TA=25°C on the production line.

In the notes at the bottom of each table it is stated that the data obtained through comprehensive evaluation, design simulation and/or process characterisation will not be tested on the production line; on the basis of the comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested plus or minus three times the standard distribution (mean ± 3 sigma).

4.1.2 Typical values

Typical data is based on TA=25°C and VDD=3.3 V. These data are for design guidance only and are not tested unless otherwise noted.

Typical ADC accuracy values are obtained by sampling a standard batch, tested over all temperature ranges, with 95% of the products having an error less than or equal to the value given (average ±2 sigma).

4.1.3 typical curve

Typical curves are for design guidance only and are untested unless otherwise noted.

4.1.4 load capacitance

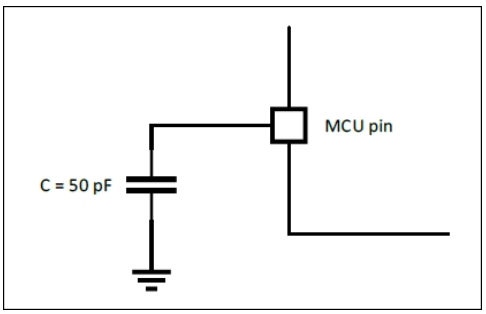


Figure 4 Load Conditions for Pins

4.1.5 Pin Input Voltage

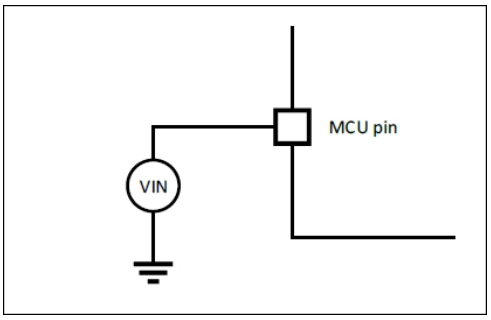


Figure 5 Pin Input Voltage

4.1.6 Power supply programme

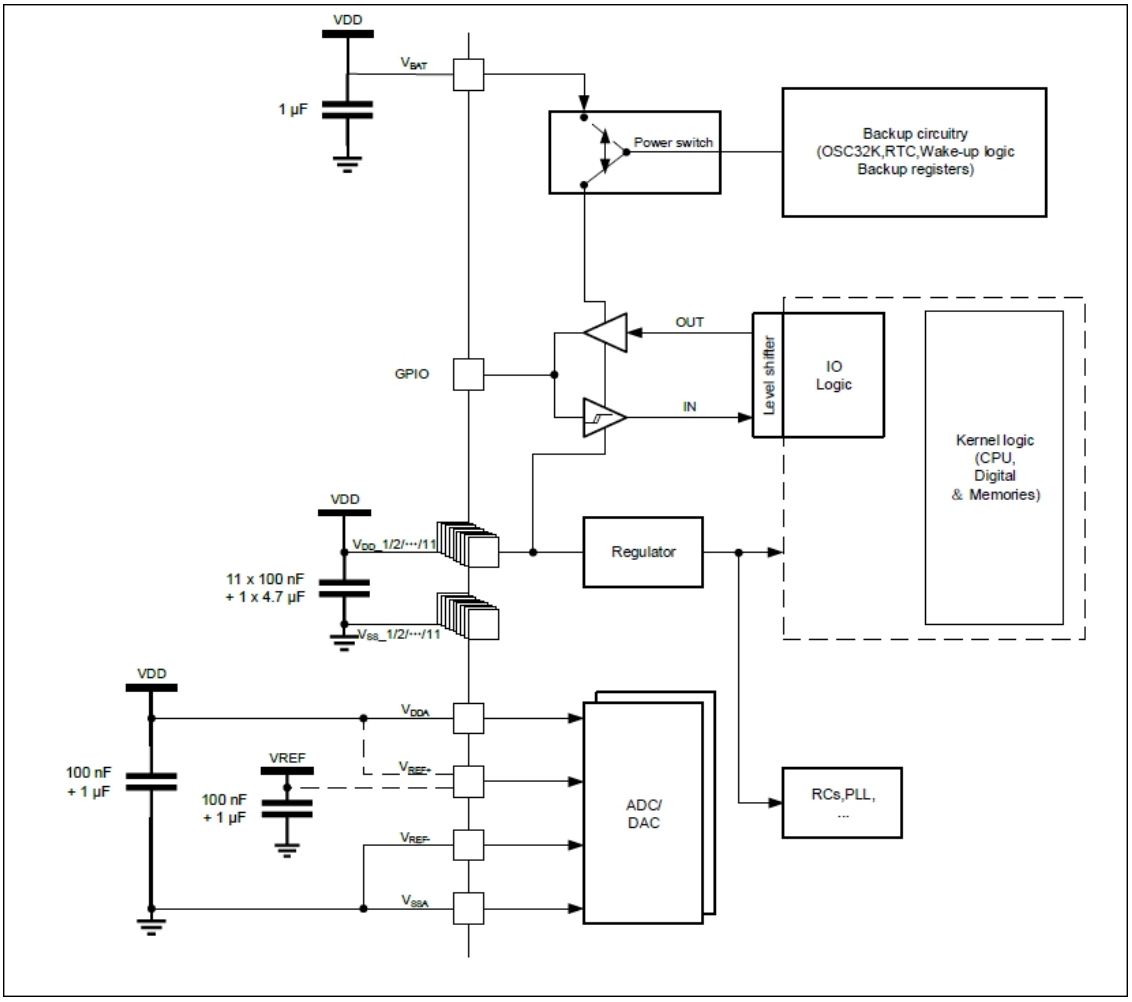
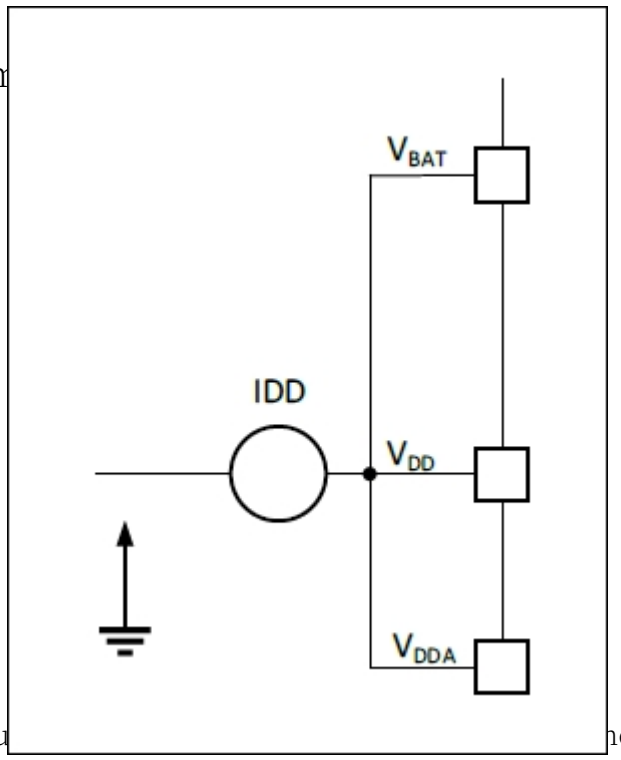


Figure 6 Power supply scheme

4.1.7 Current consumption measurement

Absolute maximum



Figu heme

Loads applied to the device in excess of the values given in the "Absolute Maximum Ratings" list may result in permanent damage to the device. The fact that only the maximum loads that can be withstood are given here does not imply that the device will operate functionally without error under these conditions. Prolonged operation of the device under maximum conditions will affect the reliability of the device.

Table 7 Voltage Characteristics

notation	Description	minimum value	maximum values	unit
VDD - VSS	External mains supply voltage (including VDDA and VDD)(1)	-0.3	4	V
VIN	Input voltage on 5V tolerant pins (2)	Vss-0.3	Vdd+4.0	
	Input voltage on other pins(2)	Vss-0.3	4.0	
|ΔVDDx|	Voltage difference between different supply pins	-	50	mV
|VSSx-VSS|	Voltage difference between different ground pins	-	50	

(1) All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to a power supply system within the external permissible range. (2) Include VREF-pin

Table 8 Current Characteristics

notation	descriptions	Maximum value (1)	unit (of measure)
IVDD	Total current through VDD/VDDA power line (supply current) (1)	150	mA
IVSS	Total current through VSS ground (outgoing current) (1)	150	
IIO	Output sink current on arbitrary I/O and control pins	25	
	Output current on arbitrary I/O and control pins	-25	

(1) All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external permissible range power supply system.

Table 9 Temperature Characteristics

notation	descriptions	numerical value	unit (of measure)
TSTG	Storage temperature range	-65 ~ +150	℃
TJ	Maximum Junction Temperature	105	℃

working conditions

4.1.8 General working conditions

Table 10 General operating conditions

notation	parameters	prerequisite	minimum value	maximum values	unit
fHCLK	Internal AHB clock frequency	-	0	216	MHz
fPCLK1	Internal APB1 clock frequency	-	0	108	
fPCLK2	Internal APB2 clock frequency	-	0	216	
VDD	Standard Operating Voltage	-	2.0	3.6	V
VDDA(1)	Analogue section operating voltage	Must be the same as VDD(2)	2.0	3.6	V
VBAT	Backup section operating voltage	-	1.6	3.6	V
TA	environmental temperature	-	-40	85	℃

(1) It is recommended that the same power supply be used to power both VDD and VDDA.

4.1.9 Operating conditions at power-up and power-down

The parameters given in the following table are based on tests at ambient temperatures listed in the General Operating Conditions.Table 11 Operating conditions at power-up and power-down

notation	parameters	prerequisite	minimum value	maximum values	unit
tVDD	VDD Rise Rate	-	0	∞	us/V
	VDD Decline Rate		20	∞	

4.1.10 Embedded reset and power control module features

The parameters given in the following table are based on testing at the VDD supply voltage listed in the General Operating Conditions.

Table 12 Embedded Reset and Power Control Module Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit
VPVD	Programmable level selection for voltage detectors	PLS[2:0]=000 (rising edge)	2.1	2.16	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.07	2.16	V

		PLS[2:0]=001 (rising edge)	2.19	2.26	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.17	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.35	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.26	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.36	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.55	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.45	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.66	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.57	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.76	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.67	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.85	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.77	2.9	V
VPVDhyst (1)	PVD hysteresis	-	-	100	-	mV
VPOR/PDR	Power-up/power-down reset threshold value	rising edge (of a mountain range)	minimum value	typical value	maximum values	unit (of measure)
		falling edge (of a mountain range)	-	1.90	-	V
		rising edge (of a mountain range)	-	2.02	-	V
VPDRhyst (1)	PDR hysteresis	-	-	30	-	mV
VREFINT	Built-in reference voltage	-40°C < TA < +85°C	1.16	1.20	1.24	V
TRSTTEMPO(1)	Reset Duration	-	-	2	-	ms
TS_vrefint(1)	When reading out the internal parameter ADC sampling time when illuminating the voltage	-	-	5.1	17.1	us

(1) Guaranteed by design, not tested in production.

4.1.11 Built-in reference voltage

The parameters given in the following table are tested at the VDD supply voltage listed in the General Operating Conditions Table 13 Built-in reference voltage parameters prerequisite

(1) The shortest sampling time is obtained by applying multiple cycles in the application.

(2) Guaranteed by design, not tested in production.

4.1.12 Supply Current Characteristics

Current consumption is a combination of a number of parameters and factors, including operating voltage, ambient temperature, load on I/O pins, software configuration of the product, operating frequency, flip-flop rate of I/O pins, location of the programme in memory, and code executed. For a description of how current consumption is measured, see the Current Consumption Test Volume description in the Test Conditions section.

current consumption

The microcontroller is in the following conditions:

- All I/O pins are in analogue input mode.
- All peripherals are off unless otherwise noted.
- When the peripheral is switched on: fPCLK1 = fHCLK/2, fPCLK2 = fHCLK.

Table 14 Current consumption in operating mode

notation	parameters	prerequisite	fHCLK	Typical value(1)		Maximum value (2)		unit (of measure)
				Enable all peripherals	Close all peripherals	Enable all peripherals	Close all peripherals	
IDD	operational mode formal electric supply stream of water or sth. resembling one	external clock (3)	216MHz	36.29	25.49	38.50	27.56	mA
			168MHz	27.71	19.27	29.95	21.35	
			72MHz	13.09	9.38	14.93	11.21	
			48MHz	9.35	6.93	11.18	8.74	
			32MHz	6.88	5.25	8.68	7.04	
			24MHz	5.67	4.46	7.41	6.20	
			16MHz	4.43	3.63	6.16	5.34	
			8MHz	3.28	2.58	4.98	4.54	
		Runs on a high-speed	128MHz	21.64	15.19	23.89	17.27	mA

(1) Typical values are obtained by testing at TA=25°C and VDD=3.3V.

(2) The maximum value was tested at TA=85°C and VDD=3.6V.

(3) The external clock is 8MHz and PLL is enabled when fHCLK > 8MHz.

Table 15 Current Consumption in Sleep Mode with Code Running in Flash

notation	parameters	prerequisite	fHCLK	Typical value(1)		Maximum value (2)		unit (of measure)
				Enable all peripherals	Close all peripherals	Enable all peripherals	Close all peripherals	
IDD	sleep pattern formal electric supply stream of water or	external clock (3)	216MHz	25.72	7.01	27.73	8.70	mA
			168MHz	19.46	4.81	21.49	6.58	
			72MHz	9.53	3.25	11.31	4.92	
			48MHz	6.99	2.81	8.76	4.51	
			32MHz	5.32	2.54	7.07	4.23	
			24MHz	4.50	2.41	6.22	4.09	
			16MHz	3.66	2.28	5.36	3.96	
			8MHz	2.90	2.17	4.57	3.84	
		Runs on reasonable high-speed internal RC oscillator (HSI)	128MHz	15.31	4.14	17.36	5.90	mA
			72MHz	9.47	3.20	11.36	4.93	
			48MHz	6.97	2.80	8.80	4.52	
			32MHz	5.32	2.54	7.11	4.26	
			24MHz	4.49	2.41	6.25	4.12	
			16MHz	3.65	2.27	5.39	3.98	
			8MHz	2.89	2.17	4.61	3.87	
IDD	Supply current in shutdown mode	The regulator is in run mode, low, high Speed and external high-speed oscillator off (no independent watchdog)						uA
		The regulator is in low power mode and low speed, High-speed internal RC oscillator and external high-speed oscillator are off (no independent watchdog)		130		1220		
	standby mode	Low-speed internal RC oscillator,		0.7		2.2		

(1) Typical values are tested at TA=25℃, VDD=3.3V. (2) Maximum value is tested at TA=85℃, VDD=3.6V. (3) External clock is 8MHz, PLL is enabled when fHCLK>8MHz. Table 16 Typical and maximum current consumption in stop and standby modes

		Low-speed internal RC oscillator on , external low-speed oscillator and RTC, IWDG are off	1.0	2.5	
		External low-speed oscillator is on, low-speed internal RC oscillator and RTC, IWDG are off.	1.0	2.6	
		External low-speed oscillator and RTC are on, low-speed internal RC oscillator and IWDG are off.	1.3	2.7	
		Low-speed internal RC oscillator and IWDG on, external low-speed oscillator and RTC off	1.0	2.7	
IDD_VBAT	Supply current in the backup area	External low-speed oscillator and RTC are on	0.9	1.3	

(1) Typical values are tested at TA=25°C, VDD=VBAT=3.3V. (2) Maximum values are obtained by testing at TA=85°C, VDD=VBAT=3.6V. (3) Derived from comprehensive evaluation, not tested in production

Built-in Peripheral Current Consumption The operating conditions of the MCU are as follows:

- All I/O pins are in analogue input mode
- All peripherals are off unless otherwise noted.
- The values given are calculated by measuring the current consumption
  - ◆ Clock off all peripherals
  - ◆ Turning on the clock

of only one peripheral Table 17 Current consumption of built-in peripherals

built-in peripherals		Typical Power Consumption at 25°C	unit (of measure)
peripherals	TIM2	2.08	
	TIM3	2.36	

	USART2	0.56	
	USART3	0.56	
	UART4	0.56	
	UART5	0.56	
	I2C1	1.81	
	I2C2	1.81	
	USB	5.42	
	CAN	1.11	
	SDIO	7.92	
	WWDG	0.24	
	DAC	0.58	
	PWR	0.008	
	BKP	0.11	
APB2	ADC1(1)	5	
	ADC2(1)	5	
	ADC3(1)	5	
	TIM1	3.71	
	TIM8	3.76	
	SPI1	1.83	
	USART1	1.39	

(1) Special conditions for ADC: fHCLK = 56MHz, fAPB1 = fHCLK/2, fAPB2 = fHCLK, fADCCLK = fAPB2/4, ADC_CR2 ADON=1 for the register.

4.1.13 External Clock Source Characteristics

High-speed external user clock generated from an external oscillator source

The characteristics given in the following table were measured using a high-speed external clock source with ambient temperature and supply voltage in accordance with general operating conditions. Table 18 High-Speed External User Clock Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
fHSE_ext	User external clock frequency(1)	-	0.615	8	35	MHz
VHSEH	OSC_IN input pin high voltage		0.48Vdd	-	Vdd	V
VHSEL	OSC_IN input pin low level voltage		Vss	-	0.38Vdd	
tw (HSE) tw (HSE)	Time when OSC_IN is high or low (1)		5	62.5	-	ns

tr(HSE) tf (HSE)	Time for OSC_IN to rise or fall (1)		-	4.1	20	
Cin (HSE)	OSC_IN input tolerance(1)	-	-	5	-	pF
DuCy (HSE)	duty cycle		45	50	55	%

(1) Guaranteed by design, not tested in production.

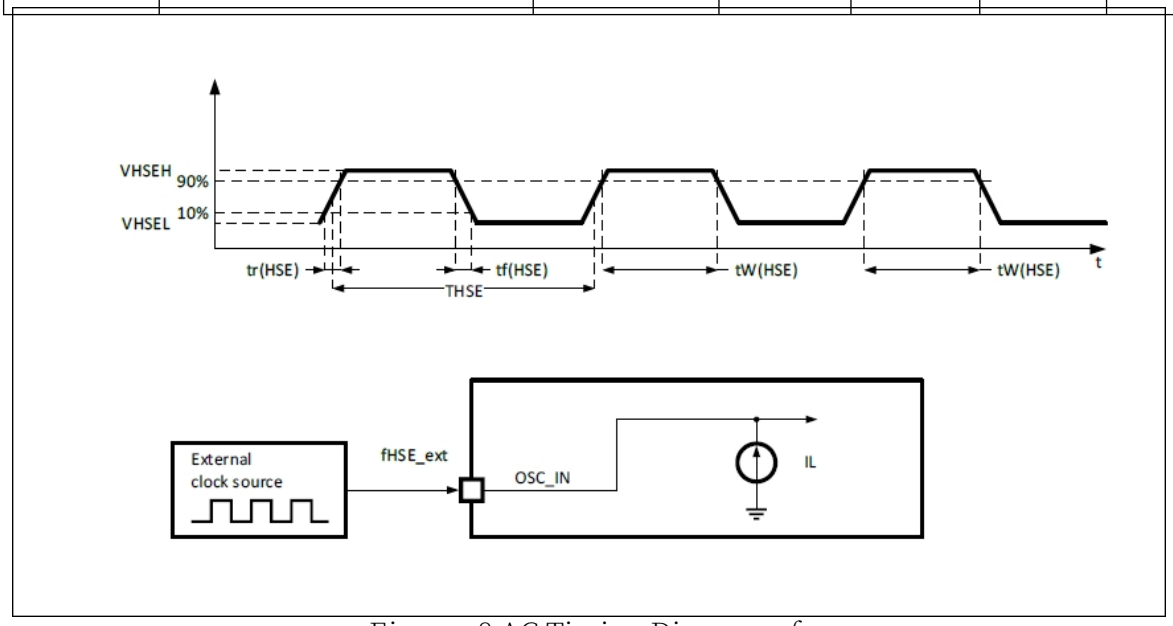


Figure 8 AC Timing Diagram of External High-Speed Clock Source Low-Speed External User Clock Generated from External Oscillator Source

The characteristic parameters given in the following table were measured using a low-speed external clock source, with ambient temperature and supply voltage in accordance with general operating conditions.

Table 19 Low-speed external user clock characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
fHSE_ext	User external clock frequency(1)	-	-	32.768	1000	KHz
VLSEH	OSC32_IN input pin high voltage		0.48Vdd	-	VDD	V
VLSEL	OSC32_IN input pin low level voltage		VSS	-	0.38Vdd	
tw (LSE) tw (LSE)	OSC32_IN high or low time (1)		450	-	-	ns
tr(LSE) tf(LSE)	OSC32_IN rise or fall time (1)		-	-	50	
Cin (LSE)	OSC32_IN input tolerance(1)	-	-	5	-	pF
DuCy (LSE)	duty cycle	-	30	-	70	%

(1) Guaranteed by design and not tested in production.

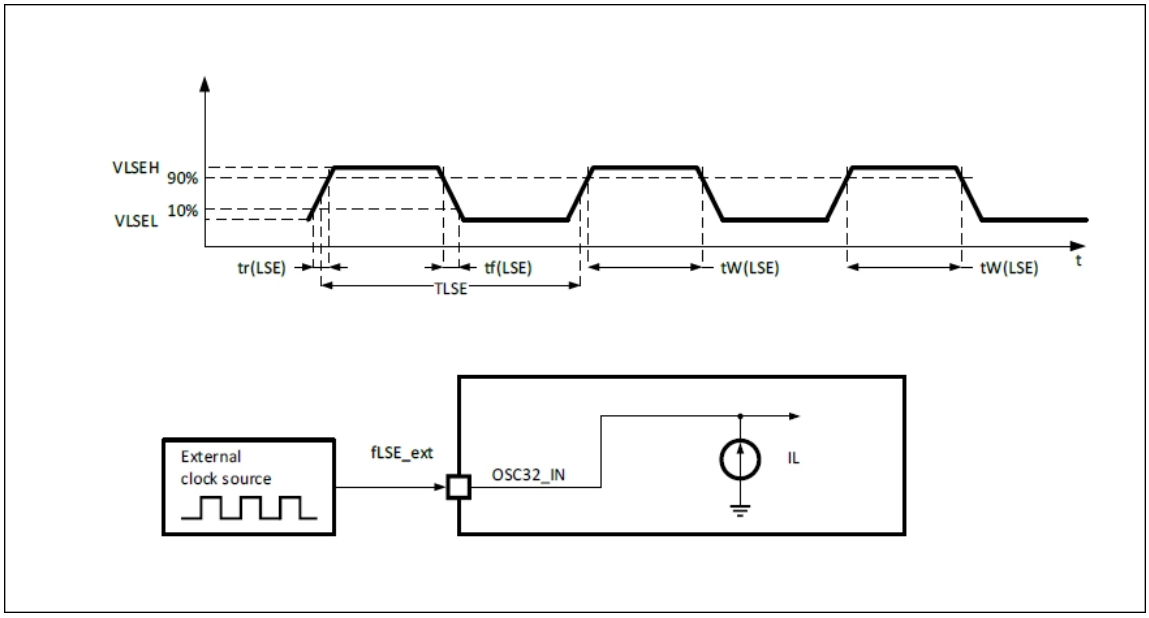


Figure 9 AC Timing Diagram of an External Low-Speed Clock Source High-Speed External Clock Generated Using a Crystal/Ceramic Resonator

The High Speed External Clock (HSE) can be generated using an oscillator consisting of a crystal/ceramic resonator from 4 to 32 MHz. The information given in this section is based on results obtained from a comprehensive characterisation evaluation using typical external components listed in the table below. In the application, the resonator and load capacitance must be placed as close as possible to the oscillator pins to minimise output distortion and stabilisation time at start-up. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the appropriate manufacturer. (Translation: The crystal resonator mentioned here is what we usually call passive crystal oscillator)

Table 20 Characteristics of HSE 4~32MHz oscillator(1)(2)

notation	parameters	prerequisite		minimum value	typical value	maximum values	unit (of measure)
fOSC_IN	oscillator frequency	-		4	8	32	MHz
tSU(HSE)(3)	start-up time	VDD is stable	TA = -40°C	-	790	-	us
			TA = 25°C	-	860	-	
			TA = 85 °C	-	960	-	

(1) Resonator characteristic parameters are given by the crystal/ceramic resonator manufacturer.

(2) Derived from a comprehensive assessment and not tested in production.

(3) tSU(HSE) is the start-up time, measured from the time the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

For CL1 and CL2, it is recommended to use high quality, porcelain dielectric capacitors designed for high frequency applications (typical values are) between 5 pF and 25 pF, and select a crystal or resonator that meets the requirements. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually give the load capacitance parameters as a serial combination of CL1 and CL2. When selecting CL1 and CL2, the capacitance of the PCB and MCU

pins should be taken into account (the capacitance of the pins to the PCB board can be roughly estimated at 10 pF).

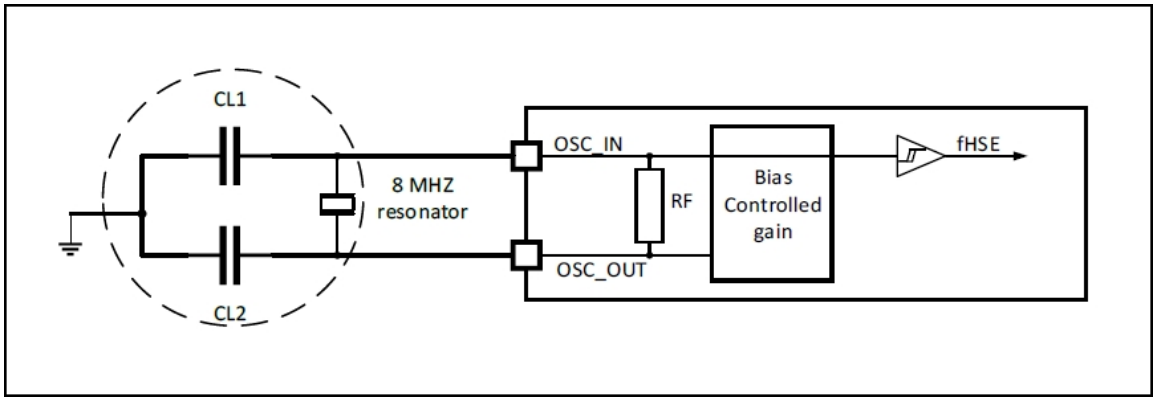


Figure 10 Typical application using an 8MHz crystal using a low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768kHz crystal/ceramic resonator. The information given in this section is the result of a comprehensive characterisation evaluation. In the application, the resonator and load capacitance must be placed as close as possible to the oscillator pins to minimise output distortion and stabilisation time at start-up. For detailed parameters (frequency, package, accuracy, etc.) of crystal resonators, please consult the appropriate manufacturer. (Translation: The crystal resonator mentioned here is what we usually call passive crystal oscillator)

Table 21 LSE oscillator characteristics (fLSE=32.768kHz)(1)

notation	parametric	prerequisite		minimum value	typical value	maximum values	unit (of measure)
tSU(HSE)(2)	start-up time	VDD is stable	TA = -40°C	-	321	-	ms
			TA = 25 °C	-	221	-	
			TA = 85 °C	-	223	-	

(1) Derived from a comprehensive assessment and not tested in production.

For CL1 and CL2, it is recommended to use high-quality ceramic dielectric capacitors between 5 pF and 15 pF, and select a crystal or resonator that meets the requirements of the

. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually give the parameters of the load capacitance as a serial combination of CL1 and CL2. The load capacitance CL is calculated by the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray is the capacitance of the pins and the capacitance associated with the PCB board or PCB, and its typical value is between 2 pF and 7 pF.

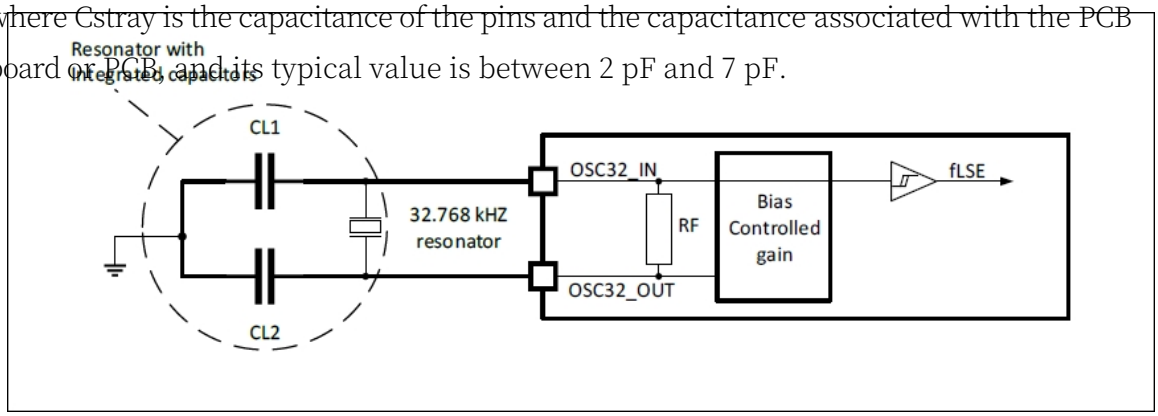


Figure 11 Typical application using a 32.768 KHz crystal

4.1.14 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperatures and supply voltages in accordance with general operating conditions.

High Speed Internal (HSI) RC Oscillator

Table 22 HSI Oscillator Characteristics (1)

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
fHSI	frequency	-	-	8	-	MHz
ACCHSI	Accuracy of HSI oscillators	TA = -40~85°C	-2.5	-	2.5	%
		TA = 0~70°C	-1	-	1	%
		TA = 25°C	-0.5	-	0.5	%
tSU (HSI)	HSI oscillator start-up time	-	-	12	-	us
IDD (HSI)	HSI oscillator power consumption	-	-	3.5	-	uA

(1) VDD = 3.3V, TA = -40 to 85°C, unless otherwise noted. Low Speed Internal (LSI) RC Oscillator

Table 23 LSI Oscillator Characteristics (1)

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
fLSI(2)	frequency	-	33	40	43	kHz
tSU(LSI)(3)	LSI oscillator start-up time	-	-	75	-	us
IDD(LSI)(3)	LSI oscillator power consumption	-	-	0.28	-	uA

(1) VDD = 3.3V, TA = -40 to 85°C, unless otherwise noted.

(2) Derived from comprehensive assessment, not tested in production

(3) Guaranteed by design, not tested in production

4.1.15 Wake-up time from low-power mode

The wake-up times listed in the table below were measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used for wake-up depends on the current operating mode:

- Stop or standby mode: clock source is RC oscillator
- Sleep mode: the clock source is the clock used when entering sleep mode

All times are measured using ambient temperatures and supply voltages in accordance with common operating conditions.

Table 24 Wake-up times for low-power modes

notation	parameters	typical value	unit (of measure)
tWUSLEEP(1)	Wake from sleep mode	10	CPU clock cycle
tWUSTOP(1)	Wake-up from shutdown mode (regulator is in low-power mode)	12	us
tWUSTDBY(1)	Wake up from standby mode	1600(2)/260(3)	us

(1) The wake-up time is measured from the start of the wake-up event until the user programme reads the first instruction.

(2) For MH32F103A series

(3) For MH32F103C series

4.1.16 PLL Characteristics

The parameters listed in the following table were measured using ambient temperature and supply voltage in accordance with general purpose operating conditions. Table 25 PLL Characteristics

notation	parameters	numerical value			unit (of measure)
		minimum value	typical value	Maximum value (1)	
fPLL_IN	PLL input clock(2)	2	8	32	MHz
	PLL Input Clock Duty Cycle	40	-	60	%
fPLL_OUT	PLL multiplier output clock	4	-	216	MHz
tLOCK	PLL phase lock time	-	51.2	87.8	us
Jitter	Cyclic jitter	-	-	200	ps

(1) Derived from a comprehensive assessment and not tested in production.

(2) Care needs to be taken to use the correct multiplication factor so that fPLL_OUT is within the allowable range based on the PLL input clock frequency.

4.1.17 Memory Characteristics

flash memory

All characteristic parameters were obtained at TA = -40 to 85°C unless otherwise noted. Table 26 Flash memory characteristics

notation	parametric	prerequisite	typical value	unit (of measure)
tPROG	16-bit programming time	-	50us	us
tERASE	Page Erase Time	-	25	ms
tME	Whole chip erase time	-	3	s

Table 27 Flash memory life and data retention period

notation	parameters	prerequisite	Minimum(1)	typical value	maximum values	unit (of measure)
NEND	Lifetime (translation: number of erasures)	TA = -40~85°C	100	-	-	thousand times
tRET	Data retention period	TA = 105°C	20	-	-	surname Nian

(1) Derived from a comprehensive assessment and not tested in production.

4.1.18 Absolute maximum (electrical sensitivity)

Electrostatic Discharge (ESD)

An electrostatic discharge (a positive pulse followed by a negative pulse one second apart) was applied to all pins of all samples, and the samples' large
Small in relation to the number of power supply pins on the chip (3 slices x (n+1) power supply pins). This test complies with the JEDEC EIA/JESD22-A114 standard. Table 28 ESD Absolute Maximum Values

notation	Parameters	prerequisite	typology	Maximum value (1)	unit (of measure)
VESD (HBM)	Electrostatic discharge voltage (human body) Modelling)	T A = +25 °C in accordance with JEDEC EIA/JESD22-A114	3A	4000	V

(1) Derived from a comprehensive assessment and not tested in production.

4.1.19 I/O Port Characteristics

General Input/Output Characteristics

Unless otherwise noted, the parameters listed in the following table were measured in accordance with general-purpose operating conditions. All I/O ports are CMOS and TTL compatible. Table 29 I/O Static Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
VIL	Input Low Level Voltage	-		-	1.38	V
VIH	Standard I/O pin, input high level current push down		1.59	-	-	
	FT I/O pin (1), input high input voltage		1.59	-	-	
Vhys	Standard I/O Pin Schmitt Trigger Voltage hysteresis(2)	-	-	0.21	-	V
	5V Tolerant I/O Pin Schmitt Trigger Voltage hysteresis (2)		-	0.21	-	V
Ilkg	Input leakage current(4)	VSS ≤ VIN ≤ VDD Standard I/O Ports	-	-	±0.5	uA
		VIN = 5V. 5V tolerance port	-	-	±1	
RPU	Weak pull-up equivalent resistance(5)	VIN = VSS	37	-	38.5	kΩ

output voltage

Unless otherwise specified, the parameters listed in the table below were measured using ambient temperature and VDD supply voltage in accordance with general operating conditions. All The I/O ports are both CMOS and

TTL compatible. Table 30

Output Voltage Characteristics

notation	parameters	prerequisite	minimum value	maximum values	unit (of measure)
VOL	Output Low Level	TTL port, I_{IO} = +12mA VDD=3.3V		0.4	V
VOH	Output High Level		2.9		
VOL	Output Low Level	CMOS port, I_{IO} = +14mA VDD=3.3V		0.4	
VOH	Output High Level		2.9		
VOL	Output Low Level	I_{IO} = +34mA VDD = 3.3V		1.3	
VOH	Output High Level		2		

4.1.20 NRST Pin Characteristics

The NRST pin input driver uses a CMOS process which connects a pull-up resistor that cannot be disconnected.

Unless otherwise noted, the parameters listed in the following table were measured using ambient temperatures and supply voltages consistent with general purpose operating conditions. Table 31 NRST Pin Characteristics

notation	parametric	Prerequisite	minimum value	typical value	maximum values	unit (of measure)
VIL(NRST)(1)	NRST Input Low Voltage	-	-	1.31	-	V
VIH (NRST)(1)	NRST input high voltage	-	-	1.57	-	
Vhys (NRST)	NRST Schmitt Trigger Voltage Hysteresis	-	-	260	-	mV
RPU	Weak pull-up equivalent resistance(2)	VIN=VSS	-	37	-	kΩ
VF(NRST)(1)	NRST input filter pulse	-	-	120	-	ns
VNF (NRST) (1)	NRST input unfiltered pulse	-	25	-	-	ns

(1) Guaranteed by design, not tested in production.

Recommended NRST pin protection

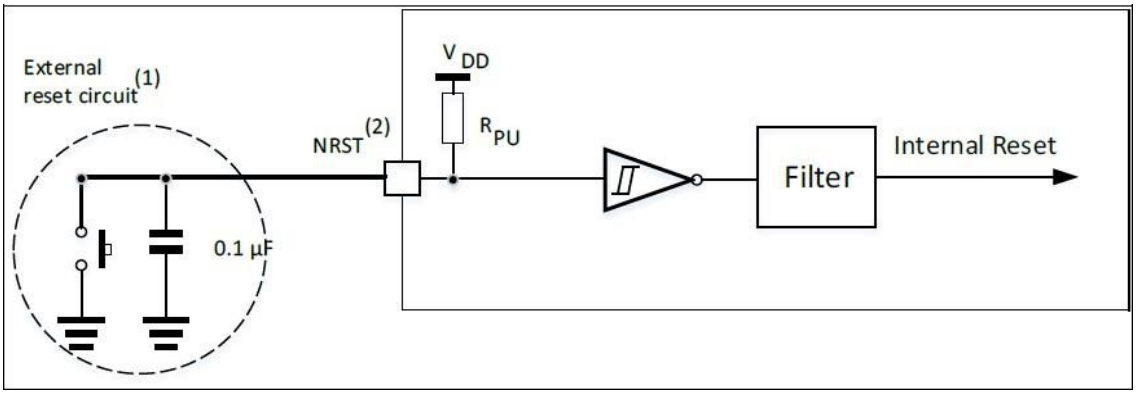


Figure 12 Recommended NRST Pin Protection

(1) The reset network is designed to prevent parasitic resets.

(2) The user must ensure that the potential of the NRST pin can be below the maximum VIL(NRST), otherwise the MCU cannot get reset.

4.1.21 TIM Timer Characteristics

The parameters listed in the following table are guaranteed by design.

Table 32 TIMx characteristics

notation	parameters	minimum value	maximum values	unit (of measure)
tres(TIM)	Timer Resolution Time	1	-	tTIMxCLK
fEXT	Timer external time for CH1 to CH4 clock frequency	0	FTIMCLK/2	MHz
ResTIM	Timer Resolution	-	16	classifier for honorific people
tCOUNTER	When the internal clock is selected, 16 Bit Counter Clock Period	1	65535	tTIMxCLK
tMAX_COUNT	Maximum possible count	-	65535*65535	tTIMxCLK

4.1.22 CAN (Controller Area Network) interface

For details on the characteristics of the input-output multiplexing function pins (CAN_TX and CAN_RX), see the IO Port Characteristics section.

4.1.23 12-bit ADC Characteristics

Unless otherwise noted, the parameters in the following table were obtained using ambient temperature, fPCLK2 frequency and VDDA supply voltage measurements that conform to general-purpose operating conditions.

Note: It is recommended that a

calibration be performed at each power-up. Table 33 ADC Characteristics

VDDA	Supply Voltage	-	2.3	3.3	3.6	V
VREF+	Positive reference voltage	-	2.3	-	VDDA	V
fADC	ADC Clock Frequency	-	0.6	-	14	MHz
fS(2)	sampling rate	-	0.05	-	1	MHz
fTRIG(2)	External Trigger Frequency	fADC = 14MHz	-	-	823	kHz
VAIN	Conversion voltage range(3)	-	0		VREF+	V
RAIN(2)	External Input Impedance	-	-	-	50	kΩ
RADC(2)	Sampling Switch Resistor	-	-	-	1	kΩ
CADC(2)	Internal Sample and Hold countenance	-	-	-		pF
tCAL(2)	calibration time	fADC = 14MHz	5.9			us
			83			1/fADC
tlat(2)	Injection Trigger Conversion Delay late	fADC = 14MHz	-	-	0.214	us
			-	-	3	1/fADC
tlatr(2)	Regular Trigger Transition Delay late	fADC = 14MHz	-	-	0.143	us
			-	-	2	1/fADC
tS(2)	sampling time	fADC = 14MHz	0.107	-	17.1	us
			1.5	-	239.5	1/fADC
tSTAB(2)	power-up time		0	0	1	us
tCONV(2)	Total conversion time (packages)	fADC = 14MHz			18	us
	(including sampling time)		14 to 252 (ts+ 12.5 for successive approximations)			1/fADC

(1) Assured by comprehensive evaluation, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Depending on the package, VREF+ can be internally connected to VDDA and VREF- can be internally connected to VSSA. See Chapter 3 for details.

(4) For external triggering, a delay 1/fPCLK2 must be added to the delays listed in Table 32.

Table 34 Maximum RAIN at fADC=14MHz(1)

TS (cycle)	tS(us)	Maximum RAIN (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4

28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	-
239.5	17.11	-

(1) Guaranteed by design, not tested in production.

4.1.24 DAC Electrical Parameters

Table 35 DAC Characteristics

notation	parameters	minimum value	typical value	maximum values	unit (of measure)	exegesis
VDDA	Analogue supply voltage	2.0	-	3.6V	V	
VREF+	reference voltage	2.0	-	3.6V	V	VREF+ must always be lower than V DDA
VSSA	earth (wire)	0	-	0	V	-
RLOAD(1)	Load when buffer is open resistive	5	-	-	kΩ	-
RO(2)	Output when buffer is closed (electrical) impedance	-	-	15	kΩ	-
CLOAD(1)	load capacitance	-	-	50	pF	on the DAC_OUT pin. Large capacitance (when buffer is on)
DAC_OUT small(1)	The buffer opens with the low end of the DAC_OUT Voltage	50	-	-	mV	Gives the maximum DAC output span
DAC_OUT large (1)	High-end when the buffer is open DAC_OUT Voltage	-	-	VREF+ - 0.2	V	
DAC_OUT small(1)	The low side of the buffer when it is turned off DAC_OUT Voltage	-	0.5	-	mV	Gives the maximum DAC output span
DAC_OUT large (1)	High-end when the buffer is turned off	-	-	VREF+	V	

INL(2)	Non-linear accumulation (in code i The connection between the value measured at the time and the code DAC_OUT large and code DAC_OUT small (Deviation between the two)	-	-	+-4	LSB	DAC configured for 12-bit
Offset error(2)	Offset error (code 0x800) Values measured at deviation from the ideal value V REF+ /2)	-	15	25	mV	DAC when VREF+ = 3.3 V Configured as a 12-bit
tSETTLING	Setting time (full range: 10 The bit input code changes from a small value to a large value and DAC_OUT reaches ±1 LSB of its final value)	-	3	4	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
refresh rate	When the input code is a smaller variable When changing from value i to i+1 LSB, the large frequency of the correct DAC_OUT is obtained.	-	-	1	MS/s	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
tWAKEUP	Wake-up time from off state (set ENx bit in DAC control register)	-	6.5	10	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ Input code between small and large can be Between energy values

PSRR+ (1)	Supply rejection ratio (relative to V DDA) (static DC measurement)	–	-60	-50	dB	No R LOAD , C LOAD ≤ 50 pF

(1) Assured by design, not tested in production. (2) Guaranteed by comprehensive evaluation, not tested in production.

4.1.25 Temperature Sensor Characteristics

Table 36 Temperature Sensor Characteristics

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
Avg_Slope(1)	average slope	-	5	-	mV/°C
V25(1)	Voltage at 25°C	-	1.43(4)/ 1.18(5)	-	V
tSTART(2)	Establishment time	-	-	10	us
TS_temp(2)(3)	ADC sampling time when reading temperature	-	-	17.1	us

(1) Assured by comprehensive evaluation, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) The minimum sampling time can be determined by the application through multiple cycles.

(4) For MH32F103A series

(5) For MH321F03C series

Use the following formula to derive the temperature:

Temperature (°C) = {(V25 - VSENSE) / Avg_Slope} + 25

Here (1):

V25 = VSENSE at 25 °C

Avg_Slope = average slope of the temperature vs. VSENSE curve (in mV/°C)

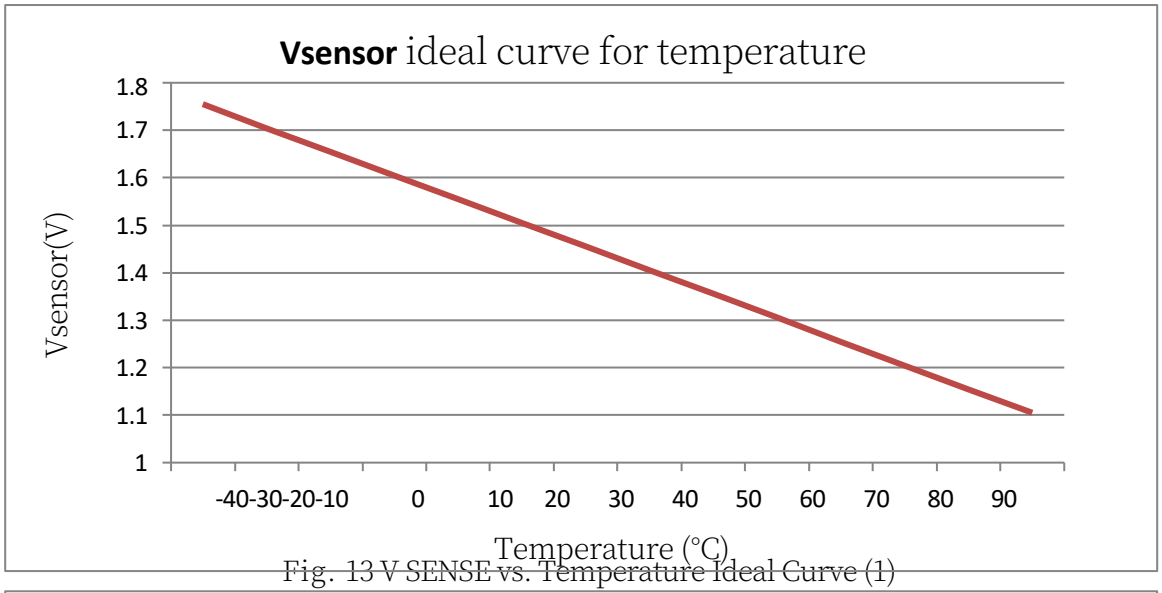


Fig. 13 V SENSE vs. Temperature Ideal Curve (1)

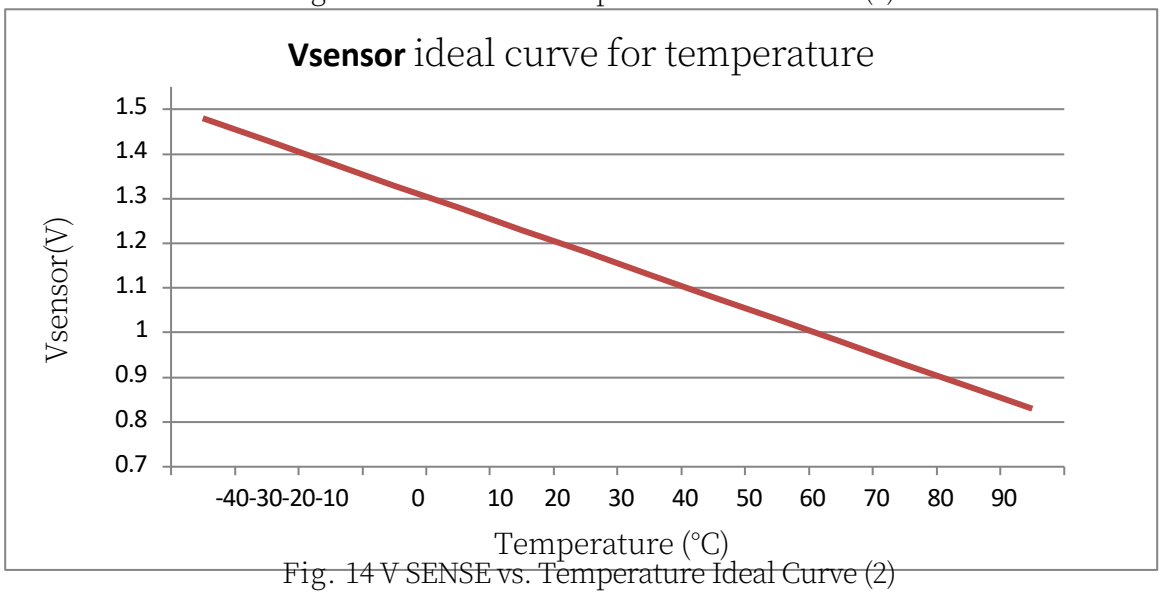
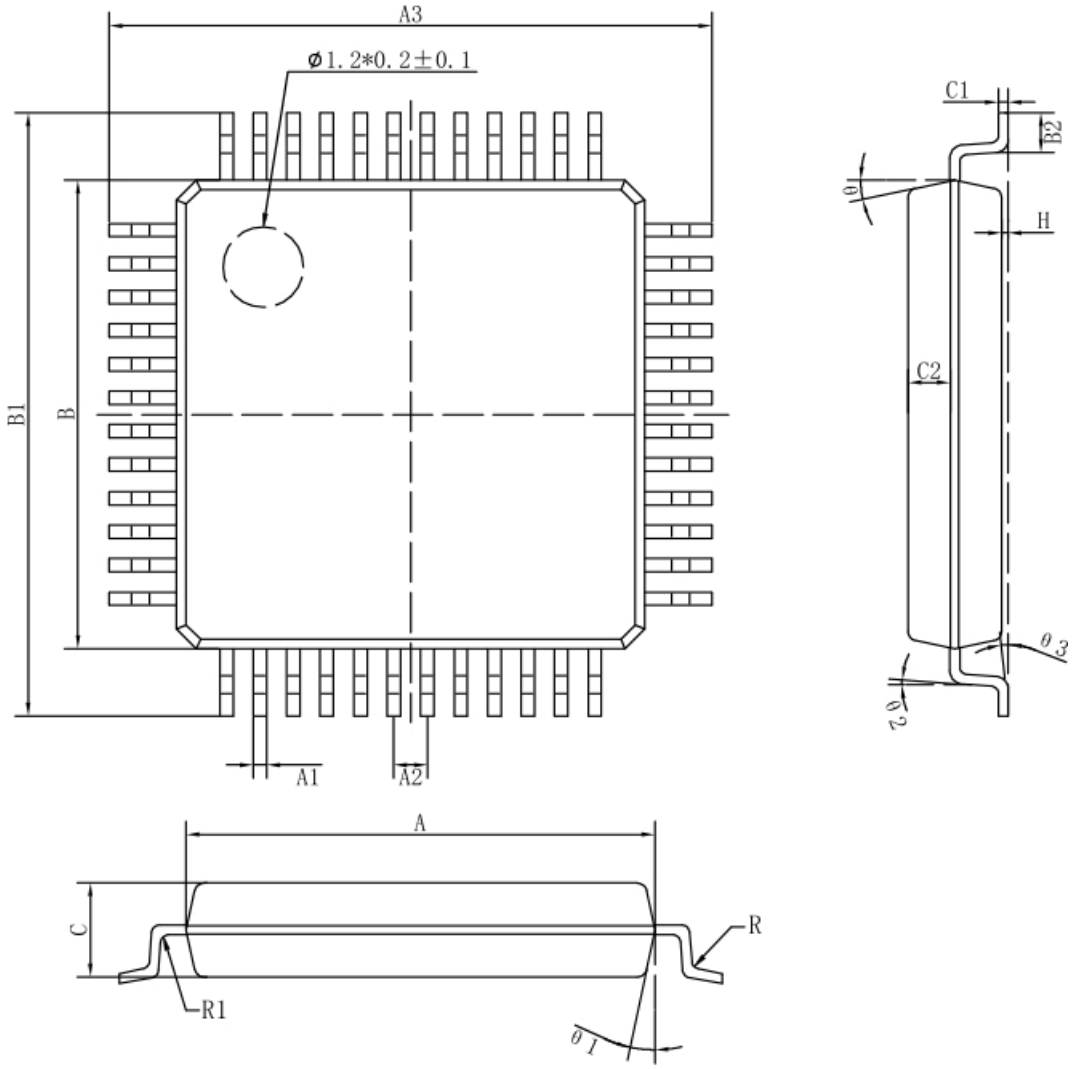


Fig. 14 V SENSE vs. Temperature Ideal Curve (2)

5 Package Characteristics

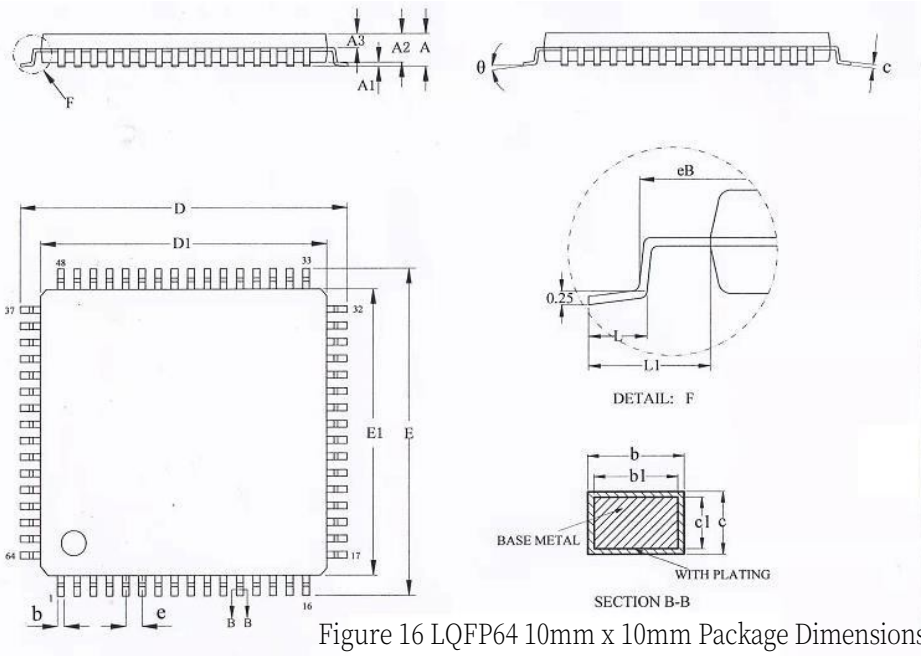
LQFP48 package



尺寸 / 标注	最小(mm)	最大(mm)	尺寸 / 标注	最小(mm)	最大(mm)
A	6.90	7.10	C2	0.636TYP	
A1	0.20TYP		H	0.05	0.15
A2	0.50TYP		θ	12° TYP4	
A3	8.80	9.20	θ1	12° TYP4	
B	6.90	7.10	θ2	4° TYP	
B1	8.80	9.20	θ3	0° ～ 5°	
B2	0.50	0.80	R	0.15TYP	
C	1.30	1.50	R1	0.12TYP	
C1	0.127	0.16			

Figure 15 LQFP48 7mm x 7mm Package Dimensions

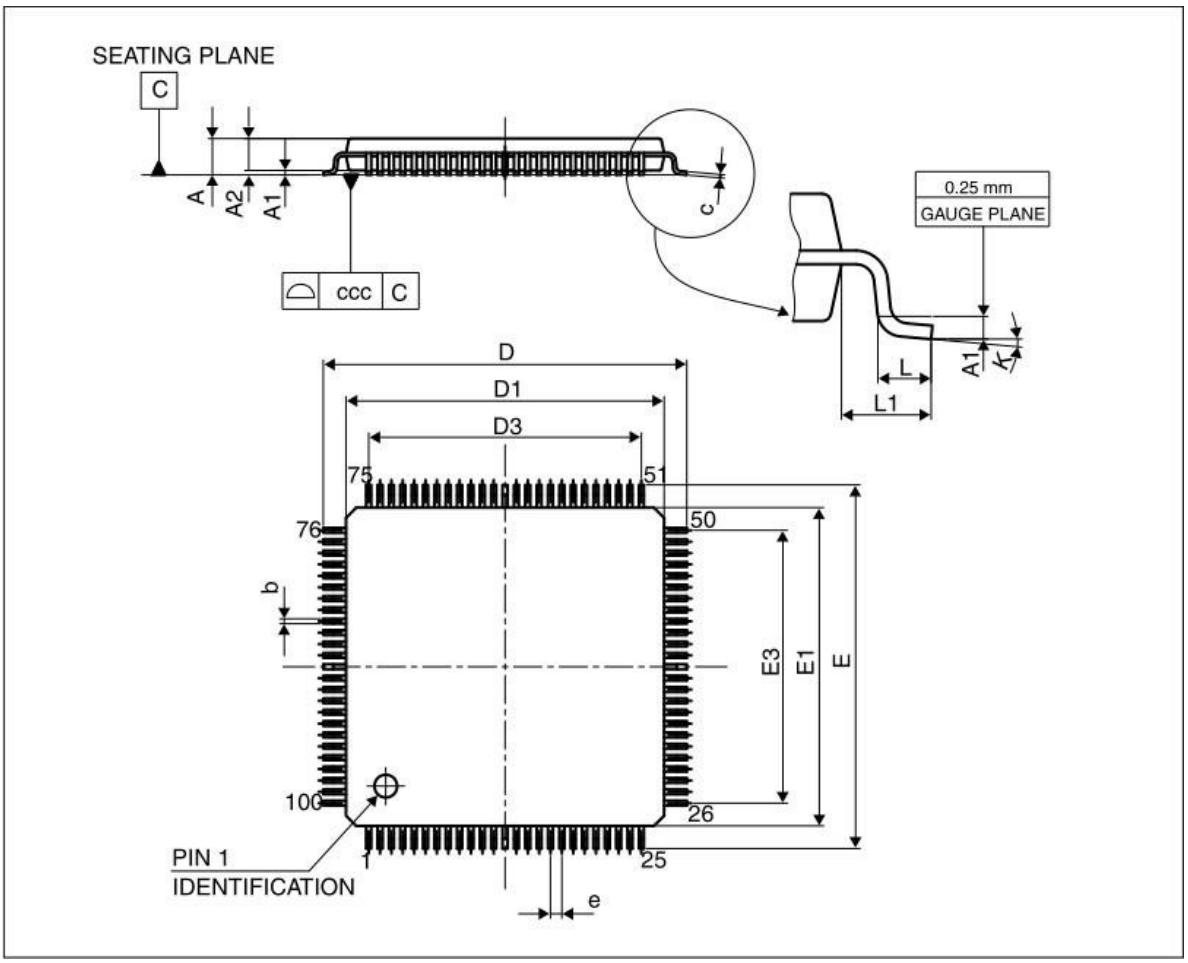
LQFP64 package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	—	11.25
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 16 LQFP64 10mm x 10mm Package Dimensions

LQFP100 package



Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

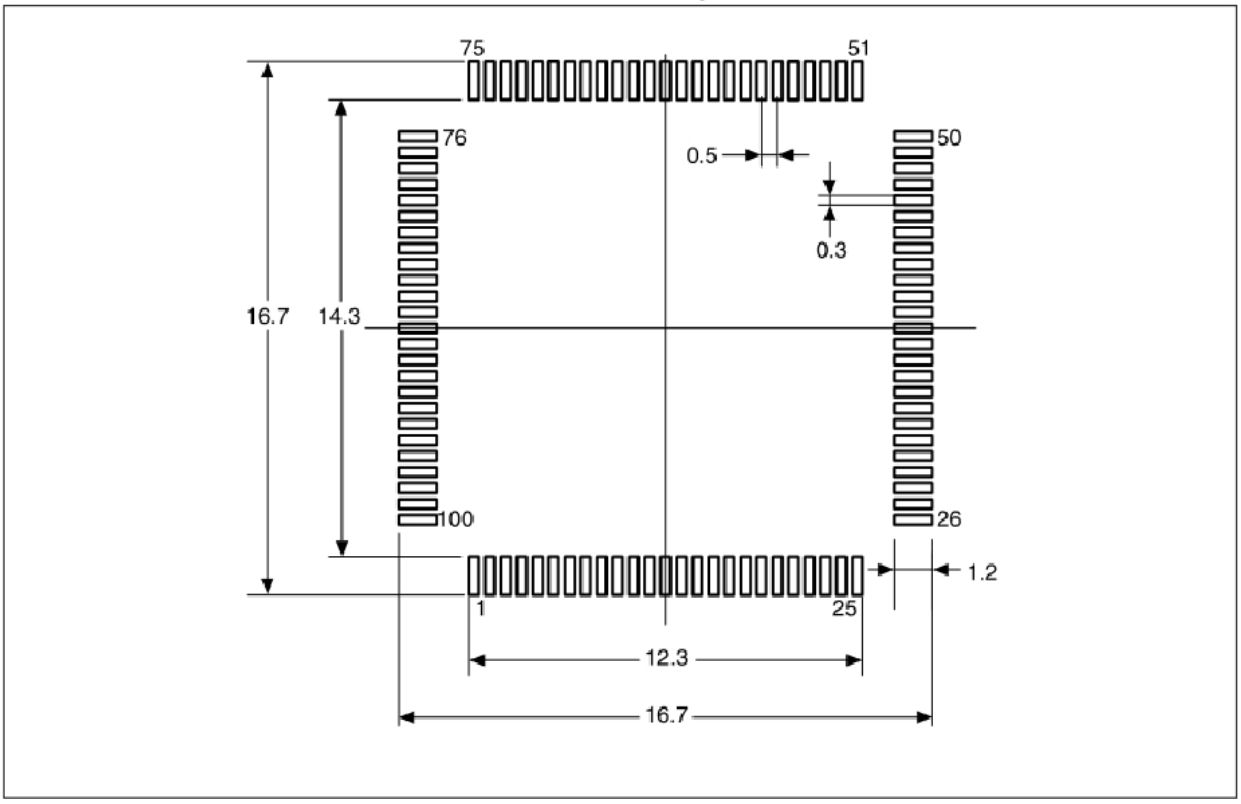
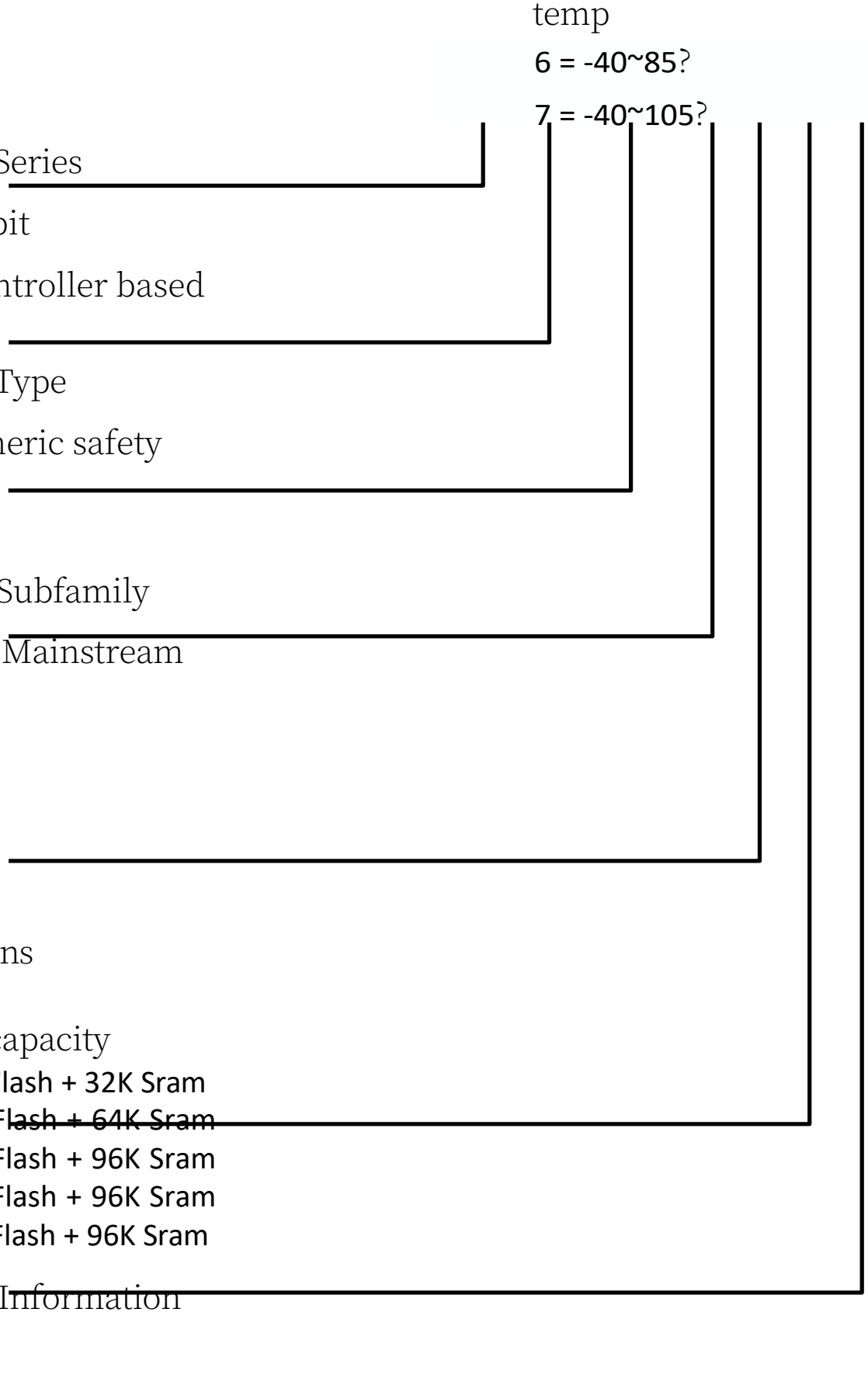


Figure 17 LQFP100 14mm x 14mm Package Size

6 Order Code

Table 37 MH32F103A(C) Series Ordering Code Information Graphic

Example:



mh 32f103a c b t 6

7 appendice

Table 38 Document version history

dates	releases	modify
2021-1-17	1.00	initial version
2022-5-28	1.01	Add LQFP100 package description