Data sheet

AIR32F103xxxx

Enhanced, true random number, hardware encryption algorithm unit,32core belt128KBytes to 256KByte flash microcontrollerUSB,CAN,17timer,3indivualADC,2indivualDAC,15communication interface

Function:

■ Kernel:32bitCore

- Highest216MHzWorking frequency, up to 2.54DMips/MHz(CoreMark1.0)
- Single-cycle multiplication and hardware division

■ Memory

- 128K/256Kbytes of flash program memory
- 32K/64K/96KBytesSRAM

■ Clock, reset and power management

- 2.0~3.6volt power supply andI/Opin
- Power-on/power-off reset (POR/PDR), programmable voltage monitor (PVD)
- 4~32MHzcrystal oscillator
- Built-in factory-tuned8MHzofRCOscillator
- Built-in calibrated40kHzofRCOscillator
- With calibration function32kHzRTCOscillator

■ Low power consumption

- Sleep, shutdown and standby modes
- VBATforRTCand backup register power

■ 3indivual12bit analog-to-digital converter,1usConversion time (up to16 input channels)

- Conversion range:0to3.6V
- Three sets of sample and hold functions
- Temperature Sensor

■ 2indivual12BitD/Aconverter

■ DMA:12aisleDMAcontroller

- Supported peripherals: timer,ADC,DAC , SDIO,SPI,I2S,I2CandUSART

■ Debug mode

- Serial single wire debugging (SWD)andJTAGinterface
- Embedded tracking module (ETM)

■ as many as51indivualI/Oport

- 51multifunctional two-wayI/Omouth, allI/OThe mouth can be mapped to16external interrupt
- allGPIOThe pull-up and pull-down resistors can be forced to be configured.

■ EnhancedCRCcomputing unit

■ 17timers

- 10indivual16bit timers, each timer has up to4indivual for input capture/output comparison/PWMor pulse meter number of channels and incremental encoder input
- 2indivual16Bit with dead zone control and emergency brake for motor controlPWMAdvanced control timer
- 2Watchdog timers (independent and windowed)
- System timer:twenty fourBit decrement counter
- 2indivual16bit basic timer

■ as many as13communication interface

- Up to2indivualI2CInterface (supportSMBus/PMBus)
- Up to5indivualUSARTInterface (supportISO7816, LIN,IrDAinterface and modem control)
- Up to3indivualSPIinterface,2a beltI2Sinterface multiplexing
- CANinterface(2.0Binitiative)
- USB 2.0Full speed interface (optional internal1.5KPull-up resistor)
- SDIOinterface

■ Hardware encryption algorithm unit

- Built-in hardware algorithm (DES, AES, SHA, SM1, SM3, SM4, SM7)
- Provides a complete high-performance algorithm library

■ TRNG:TRNGUnit used to generate truly random number sequences

- Four independent true random sources, individually configurable
- Can be produced once128BITrandom number
- Optional digital post-processing function
- Attack detection

■ SENSOR: Voltage temperature sensor alarm

- Can be tested individuallyVBATandVDDVoltage
- Provide temperature detection sensor
- Optional reset or interrupt after alarm

■ SRAMScramble

- Support address and data scrambling

■ One-time programmable (OTP)

- support32 Bytes

■ AESEncrypted download (supported by some models):

- Can be downloaded and usedAESencryptedHEX, the hardware performs Decryption execution
- Support regional encryption and decryption functions

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1 Introduction

The content in the data sheet includes: the basic configuration of the product (such as the capacity of built-in Flash and RAM, the type and quantity of peripheral modules, etc.), management

Pin quantity and assignment, electrical characteristics, packaging information, and ordering codes, etc.

2 Specifications

The AIR32F103xxxx series uses a high-performance 32-bit core with a maximum operating frequency of 216 MHz.

Built-in memory includes: maximum 256K Flash, 96K SRAM

This series has built-in up to 2 advanced timers, 10 general-purpose timers, 2 basic timers, 3 12-bit ADCs, and 2 12-bit ADCs.

DAC also includes standard and advanced communication interfaces including: 3 SPI interfaces, 2 I2S interfaces, 2 I2C interfaces, 5 U(S)ART interfaces

port, 1 USB2.0 full-speed serial communication interface, 1 CAN bus controller, 1 SDIO interface

The AIR32F103xxxx series operates in the temperature range of -40°C to +85°C, with a supply voltage of 2.0 V to 3.6 V, and a power-saving mode to ensure low power consumption.

application requirements.

Due to these peripheral configurations, AIR32F103xxxx can be applied to a variety of application scenarios:

• Industrial applications such as programmable controllers, printers, scanners, etc.

• Motor drive and speed control

• IoT low-power sensor terminals, such as sports bracelets, etc.

• UAV flight control and gimbal control

• Toy products

• Household appliances

• smart robot

• smart watch

Device overview

Table 1 Device function configuration table

series		Air32F103		
model		CBT6	CCT6	RPT6
Flash memory (K bytes)		128	256	256
SRAM(K bytes)		32	64	96
Certainty hour device	advanced	1	1	2
	universal	4	4	10
	basic	2	2	2
Pass letter catch mouth	SPI	3	3	3
	I2S	-	-	2
	I2C	2	2	2
	USART/UART	3	3	5
	USB	1	1	1
	CAN	1	1	1
	SDIO	-	-	1
GPIO port		37	37	51
12-bit ADC module (number of channels)		2(10 channels)	2(10 channels)	3(16 channels)
12-bit DAC module (number of channels)		2(2 channels)	2(2 channels)	2(2 channels)
Random number module		support		
Hardware encryption algorithm unit		support		
Page size (K bytes)		1	2	2
CPU frequency		216M		
Operating Voltage		2.0~3.6V		
Operating temperature		– 40 to +85℃		
Package form		LQFP48		LQFP64

Overview

2.1.1 32-bit Core with embedded flash memory and SRAM

The 32-bit Core provides a low-cost platform, reduced pin count, reduced system power consumption, and excellent

Superior computing performance and advanced interrupt system response.

2.1.2 Built-in flash memory

Up to 256K of built-in flash memory for storing programs and data.

Table 2 Matching relationship between power supply voltage and Flash Delay level

Flash Delay grade	HCLK(MHz)	

	Voltage Range 2.3V-3.6V	Voltage Range 2.0V-2.3V
0	0 < HCLK <= 108	0 < HCLK <= 32
1	108 < HCLK <= 216	32 < HCLK <= 64
2	-	64 < HCLK <= 128
3	-	128 < HCLK <= 192
4	-	192 < HCLK <= 216

2.1.3 Memory Protection Unit (MPU)

The Memory Protection Unit (MPU) is used to manage the CPU's access to memory to prevent one task from accidentally damaging another active task.

memory or resources. This storage area is organized into up to 8 protected areas, which in turn can be subdivided into up to 8 sub-areas. The size of the protected area can be

from 32 bytes to the entire 4 Gbytes of addressable memory.

MPUs are especially useful if there is some critical or certified code in the application that must be protected from erroneous behavior of other tasks.

use. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and

Take action. In an RTOS environment, the kernel can dynamically update the settings of the MPU area based on the executing process.

2.1.4 Built-in SRAM built-in flash memory

Built-in SRAM with a maximum of 96K bytes, the CPU can access (read/write) with 0 wait cycles.

2.1.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit uses a fixed polynomial (selectable multiple modes, and can perform hardware data processing) to generate

processor, generates a CRC code from a 32-bit data word.

In numerous applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of EN/IEC 60335-1 standard

Within the scope, it provides a means of detecting flash memory errors.

2.1.6 Nested Vectored Interrupt Controller (NVIC)

Built-in nested vectored interrupt controller, capable of handling up to 71 maskable interrupt channels (excluding 16 Core interrupt lines) and 8

priority.

●Tightly coupled NVIC can achieve low-latency interrupt response processing

● The interrupt vector entry address directly enters the kernel

●Tightly coupled NVIC interface

● Allow early handling of interrupts

● Handle late arriving higher priority interrupts

● Support interrupt tail link function

● Automatically save processor status

● Automatically resumes when interrupt returns, no additional instruction overhead required

This module provides flexible interrupt management capabilities with minimal interrupt latency.

2.1.7 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 19 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently It triggers events (rising edge or falling edge or both edges) and can be masked individually; there is a pending register to maintain all interrupt requests request status. EXTI can detect a pulse width smaller than the internal APB2 clock period. Up to 80 general-purpose I/O ports can be connected to 16 an external interrupt line.

2.1.8 Clock and startup

The system clock is selected at startup. The internal 8MHz RC oscillator is selected as the default CPU clock at reset, and can be selected later. External, 4~32MHz clock with failure monitoring; when the external clock failure is detected, it will be isolated and the system will automatically switch to Internal RC oscillator, if interrupts are enabled, software can receive corresponding interrupts. Likewise, the need for PLL can be taken when Complete interrupt management of the clock (e.g. when an indirectly used external oscillator fails).

Multiple prescalers are used to configure the AHB frequency, high-speed APB (APB2) and low-speed APB (APB1) regions. Maximum frequency of AHB and high-speed APB is 216MHz, and the highest frequency of low-speed APB is 108MHz.

2.1.9 Startup mode

At startup, one of three bootstrap modes can be selected via the bootstrap pin:

● Boot from program flash memory

● Boot from system memory

● Boot from internal SRAM

The bootloader is stored in the system memory, and the flash memory can be reprogrammed through USART1.

2.1.10 Power supply solution

● VDD: supplies power to I/O pins and internal voltage regulator.

● VSSA, VDDA: Provide power for the ADC, reset module, RC oscillator and the analog part of the PLL. VDDA and VSSA must be connected separately to VDD and VSS.

● VBAT: When VDD is turned off, power is supplied (via the internal power switch) to the RTC, external 32kHz oscillator and backup registers.

Note: Please refer to Table 9 for general working conditions for each voltage range.

2.1.11 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit. This circuit is always in working condition to ensure that the system is powered on.

It works when it exceeds 2V; when VDD is lower than the set threshold (VPOR/PDR), the device is placed in the reset state without using an external reset circuit.

road. There is also a programmable voltage monitor (PVD) in the device, which monitors the VDD/VDDA supply and compares it with the threshold VPVD. When VDD is lower than

Or an interrupt is generated when it is higher than the threshold VPVD. The interrupt handler can issue a warning message or transfer the microcontroller to a safe mode. PVD function

Need to be enabled through program.

2.1.12 Voltage regulator

The voltage regulator has three operating modes: main mode (MR), low power mode (LPR) and shutdown mode

● Main mode (MR) is used for normal operation

● Low power mode (LPR) is used for CPU shutdown mode

● Shutdown mode is used in the standby mode of the CPU: the output of the voltage regulator is in a high-impedance state, the power supply to the core circuit is cut off, and the voltage regulator is at zero

Consumes state (but the contents of registers and SRAM will be lost)

The regulator is always active after reset and shuts down in standby mode with a high-impedance output.

2.1.13 Low power mode

● Sleep mode

In sleep mode, only the CPU is stopped, all peripherals are in working state and can wake up the CPU when an interrupt/event occurs.

● Stop mode

Stop mode can achieve the lowest power consumption without losing SRAM and register contents. In shutdown mode,

Stop the power supply of all internal 1.1V parts, the PLL, HSI RC oscillator and HSE crystal oscillator are turned off, and the voltage regulator can be set

in normal mode or low power mode.

The microcontroller can be woken up from shutdown mode through any signal configured as EXTI. The EXTI signal can be 16 external I/O ports.

1. PVD output, RTC alarm clock or USB wake-up signal.

● Standby mode

The lowest power consumption can be achieved in standby mode. The internal voltage regulator is turned off, so all internal 1.1V section supplies

The power is cut off; the RC oscillator of PLL, HSI and HSE crystal oscillator are also turned off; after entering standby mode, the SRAM and register

The contents will disappear, but the contents of the backup register will still be retained and the standby circuit will still work. The conditions for exiting from standby mode are:

An external reset signal on NRST, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm timeout.

Note: RTC, IWDG and corresponding clocks will not be stopped when entering shutdown or standby mode

2.1.14 DMA

Supports up to 12 channels of general DMA (DMA1 is 7 channels, DMA2 is 5 channels) and can manage memory to memory, device to memory and storage

Data transfer from device to device; the DMA controller supports ring buffer management, which avoids the error caused when the controller transfer reaches the end of the buffer.

A sudden interruption.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software; the length of the transfer, the source address of the transfer

and target address can be set individually through software. DMA can be used for major peripherals: SPI/I2S, I2C, USART, advanced/general purpose

/Basic timer TIMx, ADC, DAC, SDIO.

2.1.15 RTC (real-time clock) and backup register

The RTC and backup registers are powered by a switch that selects VDD power supply when VDD is valid, otherwise it is powered by the VBAT pin. reserve

Registers (42 16-bit registers) can be used to save 84 bytes of user application data when VDD is turned off. RTC and backup register

Will not be reset by system or power reset sources; nor will it be reset when waking from standby mode.

A real-time clock has a set of continuously running counters and can provide calendar clock functionality with appropriate software, as well as alarm interrupts and steps.

Segment interrupt function. The driving clock of the RTC can be a 32.768kHz oscillator using an external crystal or an internal low-power RC oscillator.

Or a high-speed external clock divided by 128. The internal low-power RC oscillator has a typical frequency of 40kHz. To compensate for deviations in natural crystals, it is possible to

To calibrate the RTC clock by outputting a 512Hz signal. The RTC has a 32-bit programmable counter that uses a compare register

The memory allows long-term measurements. There is a 20-bit prescaler for the time base clock, the default clock is 32.768kHz

, it will produce a 1 second long time base.

2.1.16 Timers and watchdogs

This series of products contains up to 2 advanced control timers, 4 ordinary timers, 2 basic timers, 2 watchdog timers and 1

System tick timer.

The following table compares the functionality of advanced control timers, normal timers, and basic timers:

Table 3 TIM configuration table

timer	Counter resolution	Counter type	Prescaler coefficient	Generate DMA request	capture/compare channels	complementary output
TIM1 TIM8	16 bit	upward, toward down, up/ Down	1~65536 any whole time number	Can	4	have
TIM2 TIM3 TIM4 TIM5	16 bit	upward, toward down, up/ Down	1~65536 any whole time number	Can	4	No
TIM9 TIM12	16 bit	up	1~65536 any whole time number	Can't	2	No
TIM10 TIM11 TIM13 TIM14	16 bit	up	1~65536 any whole time number	Can't	1	No
TIM6 TIM7	16 bit	up	1~65536 any whole time number	Can	0	No

Advanced control timers (TIM1 and TIM8)

The two advanced control timers (TIM1 and TIM8) can be viewed as three-phase PWM generators assigned to 6 channels, which have dead zones

The inserted complementary PWM output can also be used as a complete general-purpose timer. Four independent channels can be used for:

● Input capture

● Output comparison

● Generate PWM (edge or center aligned mode)

●Single pulse output

When configured as a 16-bit standard timer, it has the same functionality as the TIMx timer. When configured as a 16-bit PWM generator, it has fully adjustable control ability (0~100%).

In debug mode, the counters can be frozen and the PWM outputs disabled, thereby turning off the switches controlled by these outputs.

Many functions are the same as the standard TIM timer, and the internal structure is also the same, so advanced control timers can be used through the timer link function. Can cooperate with TIM timer to provide synchronization or event linking function.

General timer (TIM2, TIM3, TIM4, TIM5)

This series of products has built-in 4 standard timers (TIM2, TIM3, TIM4, TIM5) that can run synchronously. Each timer has a A 16-bit auto-loading up/down counter, a 16-bit prescaler and 4 independent channels, each channel can be used for input Capture, output compare, PWM and single pulse mode outputs. They also work with advanced control timers through the timer linking feature operation, providing synchronization or event linking functions. In debug mode, counters can be frozen. Any standard timer can be used to generate PWM output. Each timer has an independent DMA request mechanism.

These timers are also capable of processing the signals of incremental encoders, as well as the digital outputs of 1 to 3 Hall sensors.

General timer (TIM10, TIM11, TIM9)

These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler. TIM10 and TIM11 have an independent channel, while TIM9 There are two independent channel outputs for input capture/output compare, PWM or single pulse mode. They can be used with TIM2, TIM3, TIM4, TIM5 full-featured synchronous universal timer. They can also be used as simple time bases.

General timer (TIM13, TIM14, TIM12)

These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler. TIM13 and TIM14 have an independent channel, while TIM12 has two independent channels for input capture/output compare, independent channel outputs in PWM or single pulse mode. They can be used with TIM2, TIM3, TIM4, TIM5 full-function synchronous universal timers. They can also be used as simple time bases.

independent watchdog

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler, which is powered by an internal independent 40kHz RC oscillator. The RC oscillator provides the clock; because this RC oscillator is independent of the main clock, it can operate in shutdown and standby modes. it can be viewed as The watchdog is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for applications. by option word Section can be configured to be a software or hardware enabled watchdog. In debug mode, counters can be frozen.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC flip-flop generation. They can also be used as a general purpose 16-bit time base.

window watchdog

There is a 7-bit down counter in the window watchdog and can be set to free running. It can be used as a watchdog when problems occur Reset the entire system when the problem occurs. It is driven by the main clock and has an early warning interrupt function; in debug mode, the counter can be frozen.

System time base timer

This timer is dedicated to real-time operating systems and can also be used as a standard down counter. It has the following characteristics:

● 24-bit down counter

● Automatic reloading function

● A maskable system interrupt can be generated when the counter reaches 0

● Programmable clock source

2.1.17 I2C bus

Up to 2 I2C bus interfaces, capable of working in multi-master mode or slave mode, supporting standard and fast modes. I2C interface supports 7-bit or 10-bit

Addressing, dual slave address addressing is supported in 7-bit slave mode. Built-in hardware CRC generator/checker.

They can operate using DMA and support SMBus version 2.0/PMBus bus.

2.1.18 Universal Synchronous/Asynchronous Receiver-Transmitter (USART)

3 universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and 2 universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multi-processor communication mode, single-wire half-duplex communication mode and LIN host/

from function.

The USART1 interface communication rate can reach 13.5 Mbit/s.

The USART1, USART2, and USART3 interfaces feature hardware-based CTS and RTS signal management, ISO7816-compliant smart card mode, and SPI-like communication

model.

2.1.19 Serial Peripheral Interface (SPI)

Up to 3 SPI interfaces, in slave or master mode, full-duplex and half-duplex communication rates up to 30 Mbit/s. The 3-bit prescaler can

Generates 8 master mode frequencies, configurable to 8 or 16 bits per frame. Hardware CRC generation/checking supports basic SD card and MMC modes.

All SPI interfaces can use DMA operations.

2.1.20 Audio interface (I2S)

Two standard IS interfaces (multiplexed with SPI2 and SPI3) can work in master or slave mode. These two interfaces can be configured as 16-bit or 32-bit transmission.

input or output channel, supporting audio sampling frequency from 8kHz to 48kHz. When either or both I2S interfaces are configured as

In master mode, its main clock can be output to an external DAC or CODEC (decoder) at 256 times the sampling frequency.

2.1.21 SDIO

The SD/SDIO/MMC host interface can support 3 different data bus modes in the MMC card system specification version 4.2: 1-bit (default), 4-bit and

8 bits. Version 2.0 of the SDIO Memory Card Specification supports two data bus modes: 1-bit (default) and 4-bit. The current chip version can only be supported once

One SD/SDIO/MMC version 4.2 card, but can support multiple MMC version 4.1 or earlier cards at the same time.

In addition to SD/SDIO/MMC, this interface is fully compatible with CE-ATA digital protocol version 1.1.

2.1.22 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active) with bit rates up to 1 Mbit/s. It can receive and send standard 11-bit identifiers

frames, and can also receive and send extended frames with a 29-bit identifier. It has 3 sending mailboxes and 2 receiving FIFOs, and 14 adjustable filters at 3 levels.

wave device.

2.1.23 Universal Serial Bus (USB)

Embedded with a full-speed USB compatible device controller, it complies with the full-speed USB device (12 Mbit/s) standard. The endpoints are software configurable and have

Standby/wake function. The USB-specific 48MHz clock is directly generated by the internal main PLL (the clock source can be arbitrary).

2.1.24 General purpose input and output interface (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), input (with or without pull-up or pull-down), or a multiplexed peripheral function

port. Most GPIO pins are shared with multiplexed digital or analog peripherals. Except for ports with analog input capabilities, all GPIO pins

Both feet have the ability to pass large currents.

If desired, the peripheral function of an I/O pin can be locked by a specific operation to avoid accidental writes to the I/O registers.

Each I/O can be configured with forced pull-up and pull-down resistors to save external resistor consumption.

2.1.25 ADC (Analog/Digital Converter)

Supports up to three 12-bit analog/digital converters (ADCs). Each ADC shares up to 16 external channels and can achieve single or scan conversion.

Change. In scan mode, conversion on a selected set of analog inputs is performed automatically.

Other logic functions on the ADC interface include:

● Synchronous sample and hold

● Interleaved sample and hold

●Single sampling

The ADC can operate using DMA.

Analog watchdog function allows very precise monitoring of one, multiple or all selected channels when the monitored signal exceeds a preset threshold

, an interrupt will be generated.

Events generated by the standard timer (TIMx) and the advanced control timer (TIM1 and TIM8) can be internally cascaded to the ADC's start trigger respectively.

With triggering and injection, the application can synchronize AD conversions to the clock.

2.1.26 DAC (digital/analog signal converter)

Two 12-bit buffered DAC channels can be used to convert 2 digital signals into 2 analog voltage signals and output them.

This dual digital interface supports the following functions:

● Two DAC converters: one output channel each

● 8-bit or 12-bit monotonic output

● Left and right data alignment in 12-bit mode

● Synchronous update function

● Generate noise waves

● Generate triangular waves

●Dual DAC channels independent or simultaneous conversion

● DMA function available for each channel

● External trigger for conversion

●Input reference voltage V REF+

The DAC channel can be triggered by the update output of the timer, and the update output can also be connected to different DMA channels.

2.1.27 Temperature sensor

The temperature sensor generates a voltage that changes linearly with temperature. The temperature sensor is internally connected to the input channel of ADC1_IN16,

Used to convert sensor output into digital values.

2.1.28 Serial single-wire JTAG debug port (SWJ-DP)

Embedded SWJ-DP interface, which is an interface that combines JTAG and serial single-wire debugging, can implement serial single-wire debugging interface or JTAG

Interface connection. The TMS and TCK signals of JTAG share pins with SWDIO and SWCLK respectively. A special signal sequence on the TMS pin is used

Used to switch between JTAG-DP and SW-DP.

2.1.29 Embedded Tracking Module (ETM)

Using the Embedded Trace Microunit (ETM), which connects to an external Trace Port Analysis (TPA) device via very few ETM pins, from the CPU core

Outputting compressed data streams at high speed provides developers with clear information about command execution and data flow. TPA devices can pass

USB, Ethernet or other high-speed channel connection to the debug host, real-time instructions and data flow to the debug software on the debug host

Record it and display it in the required format. TPA hardware can be purchased from development tool vendors and can be used with third-party debuggers

Software compatible.

2.1.30 True Random Number Generator (TRNG)

The TRNG unit is used to generate a true random number sequence. One job generates a 128-bit true random number sequence.

Configurable random number generation generates a CPU interrupt request.

3 pin definition

LQFP48 package

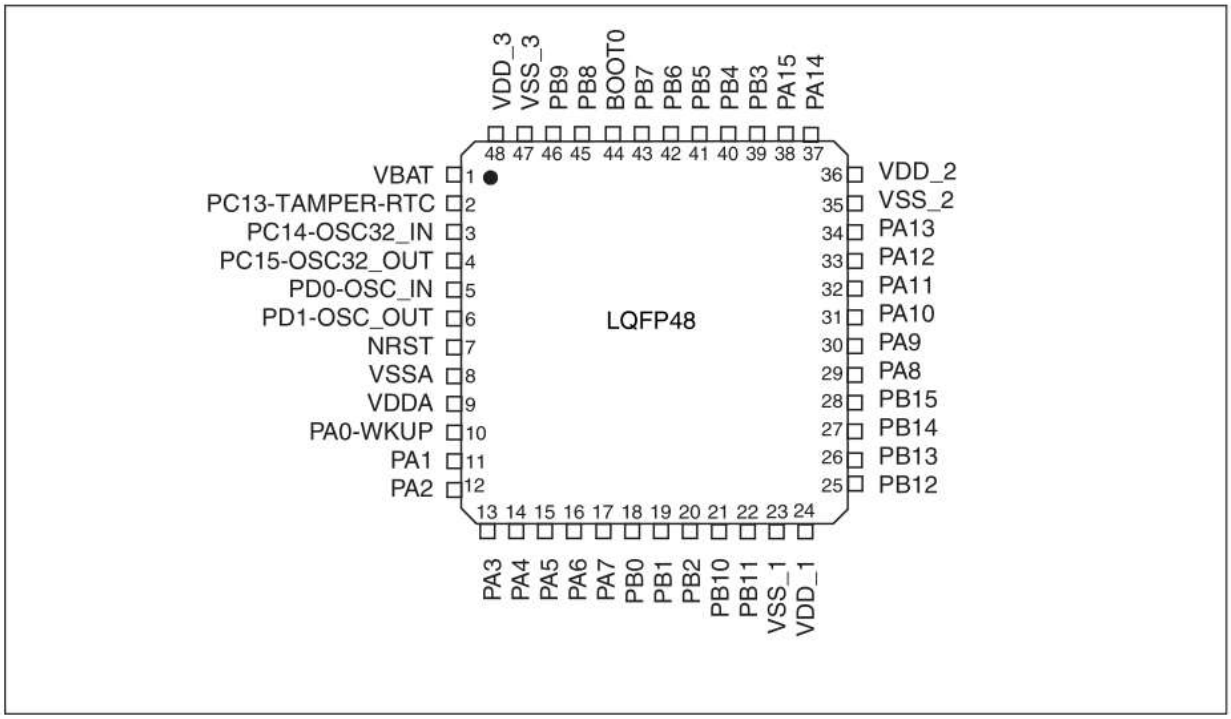


Figure 1 LQFP48 package

LQFP64 package

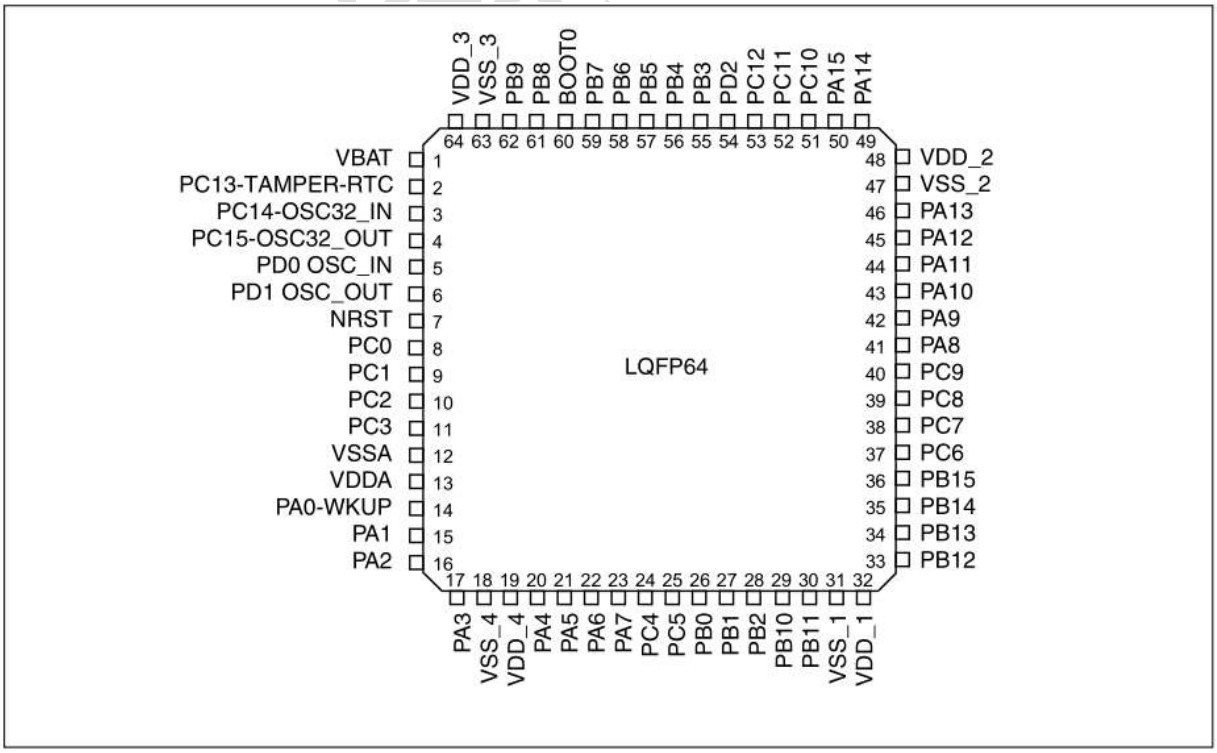


Figure 2 LQFP64 package

LQFP48 pin definition

Table 4 LQFP 48 pin definition configuration table

LQFP 48	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	VBAT	S	–	VBAT	–	–
2	PC13-TAMPERRTC	I/O	–	PC13	TAMPER-RTC	–
3	PC14-OSC32_IN	I/O	–	PC14	OSC32_IN	–
4	PC15-OSC32_OUT	I/O	–	PC15	OSC32_OUT	–
5	OSC_IN	I/O	–	OSC_IN	–	PD0
6	OSC_OUT	I/O	–	OSC_OUT	–	PD1
7	NRST	I/O	–	NRST	-	-
8	VSSA	S	–	VSSA	-	-
9	VDD	S	–	VDD	-	-
10	PA0-WKUP	I/O	–	PA0	WKUP/USART2_CTS/ ADC12_IN0/TIM2_CH1_ETR/ TIM5_CH1	-
11	PA1	I/O	–	PA1	USART2_RTS/ADC12_IN1/ TIM2_CH2/TIM5_CH2	-
12	PA2	I/O	–	PA2	USART2_TX/ADC12_IN2/ TIM2_CH3/TIM5_CH3/	-
13	PA3	I/O	–	PA3	USART2_RX/ADC12_IN3/ TIM2_CH4/TIM5_CH4/	-
14	PA4	I/O	–	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
15	PA5	I/O	–	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
16	PA6	I/O	–	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1	TIM1_BKIN
17	PA7	I/O	–	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2	TIM1_CH1N
18	PB0	I/O	–	PB0	ADC12_IN8/TIM3_CH3	TIM1_CH2N
19	PB1	I/O	–	PB1	ADC12_IN9/TIM3_CH4	TIM1_CH3N
20	PB2	I/O	FT	PB2/BOOT1	-	-
twenty one	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
twenty two	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
twenty three	VSS_1	S	–	VSS_1	–	–
twenty four	VDD_1	S	–	VDD_1	–	–
25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/TIM1_BKIN	–
26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ TIM1_CH1N	–
27	PB14	I/O	FT	PB14	SPI2_MISO/USART3_RTS/ TIM1_CH2N	–
28	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N	–
29	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ MCO	–
30	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2	–
31	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3	–

32	PA11	I/O	-	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	–
33	PA12	I/O	-	PA12	USART1_RTS/USBDP/ CAN_TX/TIM1_ETR	–
34	PA13	I/O	FT	JTMS-SWDIO	–	PA13
35	VSS_2	S	–	VSS_2	–	–
36	VDD_2	S	–	VDD_2	–	–
37	PA14	I/O	FT	JTCK-SWCLK	–	PA14
38	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/PA15/ SPI1_NSS
39	PB3	I/O	FT	JTDO	SPI3_SCK	TIM2_CH2/PB3/ TRACESWO/SPI1_SCK
40	PB4	I/O	FT	NJTRST	SPI3_MISO	TIM3_CH1/PB4/ SPI1_MISO
41	PB5	I/O	–	PB5	I2C1_SMBA/SPI3_MOSI	TIM3_CH2/SPI1_MOSI
42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
44	BOOT0	I	–	BOOT0	-	-
45	PB8	I/O	FT	PB8	TIM4_CH3	I2C1_SCL/CAN_RX
46	PB9	I/O	FT	PB9	TIM4_CH4	I2C1_SDA/CAN_TX
47	VSS_3	S	–	VSS_3	-	-
48	VDD_3	S	–	VDD_3	-	-

(1)FT = 5V tolerance

LQFP64 pin definition

Table 5 LQFP 64 pin definition configuration table

LQFP 64	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	VBAT	S	–	VBAT	-	-
2	PC13- TAMPERRTC	I/O	–	PC13	TAMPER-RTC	-
3	PC14-OSC32_IN	I/O	–	PC14	OSC32_IN	PD0
4	PC15- OSC32_OUT	I/O	–	PC15	OSC32_OUT	PD1
5	OSC_IN	I/O	–	OSC_IN	-	-
6	OSC_OUT	I/O	–	OSC_OUT	-	-
7	NRST	I/O	–	NRST	-	-
8	PC0	I/O	–	PC0	ADC123_IN10	-
9	PC1	I/O	–	PC1	ADC123_IN11	-
10	PC2	I/O	–	PC2	ADC123_IN12	-
11	PC3	I/O	–	PC3	ADC123_IN13	-
12	VSSA	S	–	VSSA	-	-
13	VDD	S	–	VDD	-	-
14	PA0-WKUP	I/O	–	PA0	WKUP/USART2_CTS/ ADC123_IN0/TIM2_CH1_ETR / TIM5_CH1/TIM8_ETR	-
15	PA1	I/O	–	PA1	USART2_RTS/ADC123_IN1/ TIM2_CH2/TIM5_CH2	-
16	PA2	I/O	–	PA2	USART2_TX/ADC123_IN2/	-

					TIM2_CH3/TIM5_CH3/ TIM9_CH1	
17	PA3	I/O	–	PA3	USART2_RX/ADC123_IN3/ TIM2_CH4/TIM5_CH4/ TIM9_CH2	-
18	VSS_4	S	–	VSS_4	-	-
19	VDD_4	S	–	VDD_4	-	-
20	PA4	I/O	–	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
twenty one	PA5	I/O	–	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
twenty two	PA6	I/O	–	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1/TIM8_BKIN/ TIM13_CH1	TIM1_BKIN
twenty three	PA7	I/O	–	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2/TIM8_CH1N/ TIM14_CH1	TIM1_CH1N
twenty four	PC4	I/O		PC4	ADC12_IN14	-
25	PC5	I/O		PC5	ADC12_IN15	-
26	PB0	I/O	–	PB0	ADC12_IN8/TIM3_CH3/ TIM8_CH2N	TIM1_CH2N
27	PB1	I/O	–	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
28	PB2	I/O	FT	PB2/BOOT1	-	-
29	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
30	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
31	VSS_1	S	–	VSS_1	-	-
32	VDD_1	S	–	VDD_1	-	-
33	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/USART3_CK/ TIM1_BKIN	-
34	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK/ USART3_CTS/TIM1_CH1N	-
35	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS/TIM12_CH1	-
36	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD/ TIM1_CH3N/TIM12_CH2	-
37	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1/ SDIO_D6	TIM3_CH1
38	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2/ SDIO_D7	TIM3_CH2
39	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
40	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
41	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ MCO	-
42	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2	-
43	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3	-
44	PA11	I/O	-	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	-
45	PA12	I/O	-	PA12	USART1_RTS/USBDP/ CAN_TX/TIM1_ETR	-
46	PA13	I/O	FT	JTMS- SWDIO	-	PA13
47	VSS_2	S	–	VSS_2	-	-

48	VDD_2	S	–	VDD_2	-	-
49	PA14	I/O	FT	JTCK-SWCLK	-	PA14
50	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS	TIM2_CH1_ETR/PA15 / SPI1_NSS
51	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
52	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
53	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
54	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	
55	PB3	I/O	FT	JTDO	SPI3_SCK/I2S3_CK	PB3/TRACESWO TIM2_CH2/SPI1_SCK
56	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4/TIM3_CH1/ SPI1_MISO
57	PB5	I/O	–	PB5	I2C1_SMBA/SPI3_MOSI /I2S3_SD	TIM3_CH2/SPI1_MOSI
58	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
59	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
60	BOOT0	I	–	BOOT0	-	–
61	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_D4/ TIM10_CH1	I2C1_SCL/CAN_RX
62	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_D5/ TIM11_CH1	I2C1_SDA/CAN_TX
63	VSS_3	S	–	VSS_3	-	-
64	VDD_3	S	–	VDD_3	-	-

(1)FT = 5V tolerance

Test Conditions

Unless otherwise stated, all voltages are based on VSS.

4.1.1 Minimum and maximum values

Unless otherwise stated, all minimum and maximum

Values are guaranteed under worst-case ambient temperature, supply voltage, and clock frequency conditions.

The notes below each table indicate that data obtained through comprehensive evaluation, design simulation, and/or process characterization will not be used in production.

Test online; on the basis of comprehensive evaluation, the minimum and maximum values are calculated after passing the sample test, and then take the average value plus minus three times the standard distribution (mean ±3Σ) is obtained.

4.1.2 Typical values

Unless otherwise stated, typical data is based on TA=25℃ and VDD=3.3V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are obtained by sampling a standard batch and testing over all temperature ranges, with an error of 95% of the product.

Less than or equal to the given value (average ±2Σ).

4.1.3 Typical curve

Unless otherwise stated, typical curves are for design guidance only and have not been tested.

4.1.4 Load capacitance

The load conditions when measuring pin parameters are shown in Figure 4

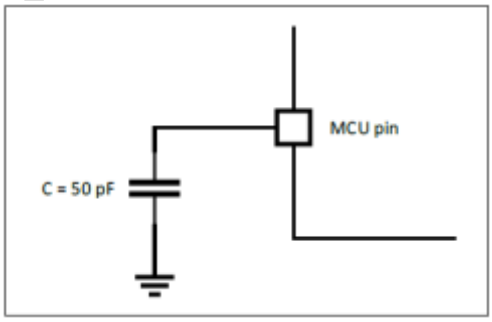


Figure 3 Load conditions of pins

4.1.5 Pin input voltage

How the input voltage on the pin is measured is shown in Figure 5

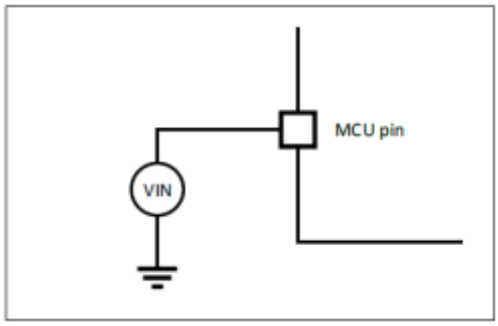


Figure 4 Pin input voltage

4.1.6 Power supply scheme

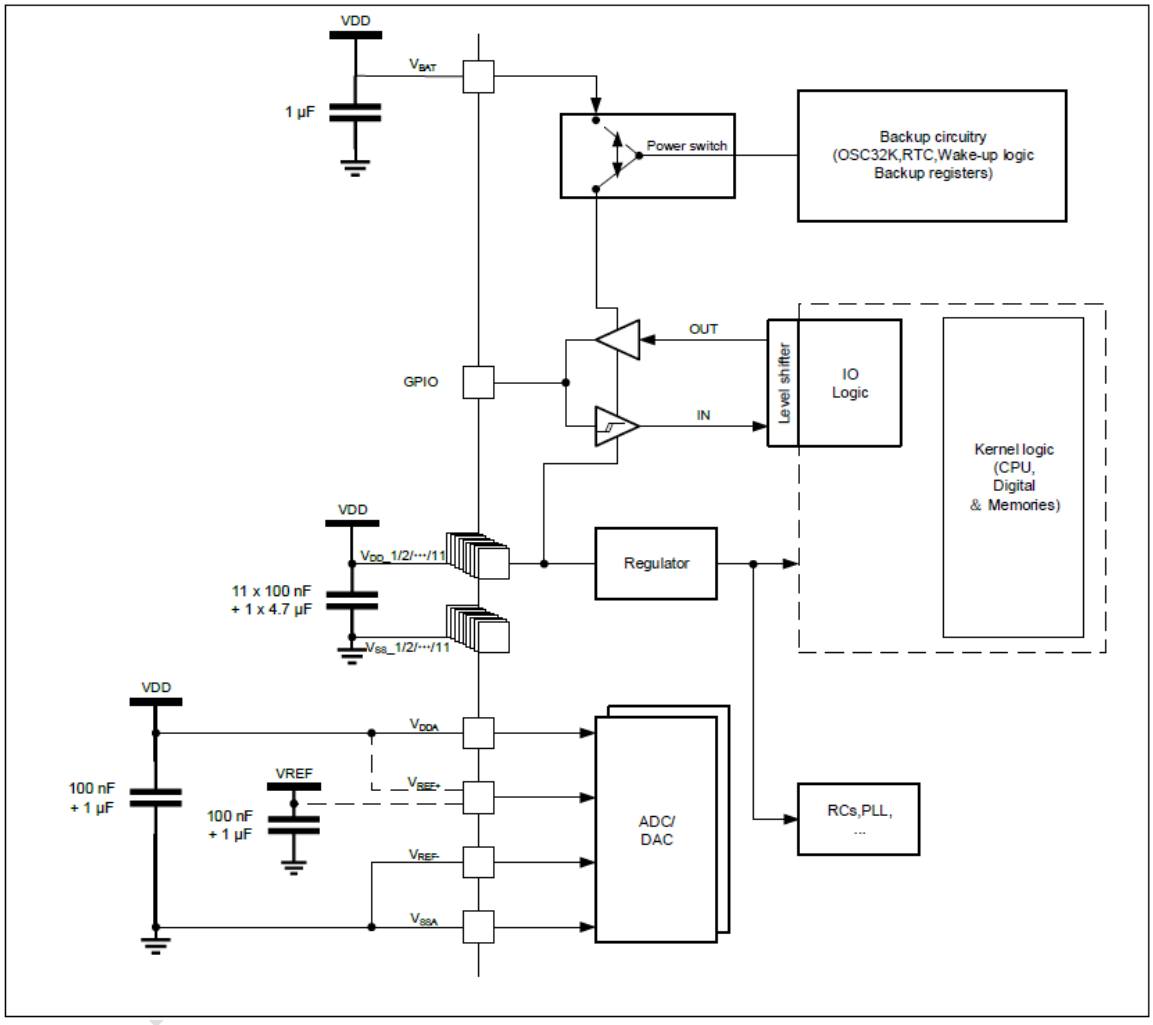


Figure 5 Power supply scheme

4.1.7 Current consumption measurement

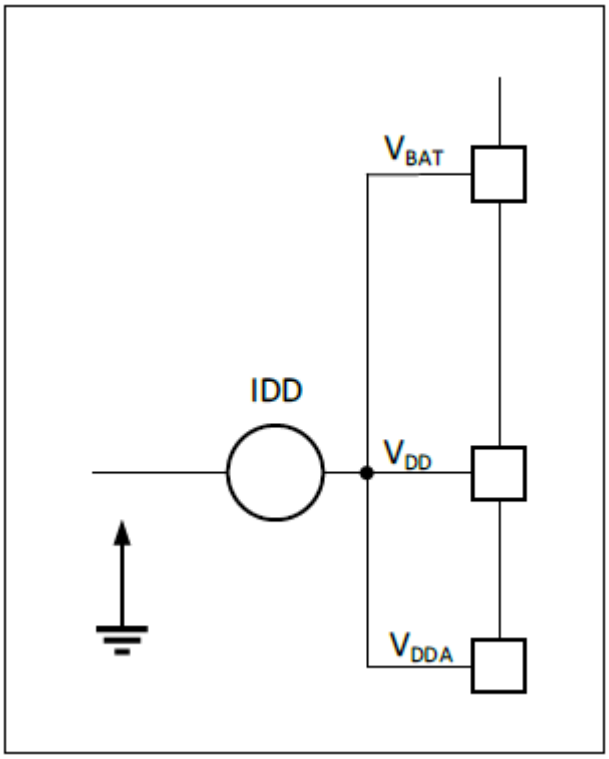


Figure 6 Current consumption measurement scheme

absolute maximum ratings

Loads applied to the device that exceed the values given in the 'Absolute Maximum Ratings' list (Tables 6, 7, 8) may cause the device to permanently fail. permanently damaged. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device is correct under this condition. device Operating the device under maximum conditions for a long time will affect the reliability of the device.

Table 6 Voltage characteristics

symbol	describe	minimum value	maximum value	unit
VDD-VSS	External main supply voltage (including VDDA and VDD)(1)	- 0.3	4	V
VIN	Input voltage on 5V tolerant pin(2)	Vss-0.3	Vdd+4.0	
	Input voltage on other pins(2)	Vss-0.3	4.0	
|ΔVDDx|	The voltage difference between different supply pins	—	50	mV
|VSSx-VSS|	The voltage difference between different ground pins	—	50	

(1) All power supply (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply system within the allowed range.

(2) Contains VREF-feet

Table 7 Current Characteristics

symbol	describe	max(1)	unit
IVDD	Total current through the VDD/VDDA power lines (supply current) (1)	150	mA
IVSS	Total current through VSS ground (outgoing current) (1)	150	
IIO	Output sink current on any I/O and control pins	25	
	Output current on any I/O and control pins	- 25	

(1) All power supply (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply system within the allowed range.

Table 8 Temperature characteristics

symbol	describe	numerical value	unit
TSTG	Storage temperature range	- 65 ~ +150	℃
TJ	maximum junction temperature	105	℃

working conditions

4.1.8 General working conditions

Table 9 General working conditions

symbol	parameter	condition	minimum value	maximum value	unit
htK	Internal AHB clock frequency	—	0	216	MHz
fPCLK1	Internal APB1 clock frequency	—	0	108	
fPCLK2	Internal APB2 clock frequency	—	0	216	
VDD	Standard working voltage	—	2.0	3.6	V
VDDA(1)	Analog part working voltage	Must be the same as VDD(2)	2.0	3.6	V
VBAT	Backup part of the working voltage		1.6	3.6	V
TA	ambient temperature	—	- 40	85	℃

(1) It is recommended to use the same power supply to power VDD and VDDA,

4.1.9 Working conditions during power-on and power-off

The parameters given in the table below are based on testing at the ambient temperatures listed in Table 8.

Table 10 Operating conditions when powering on and off

symbol	parameter	condition	minimum value	maximum value	unit
tV	VDD rising rate	—	0	∞	us/V
	VDD falling rate		20	∞	

4.1.10 Embedded reset and power control module features

The parameters given in the table below are based on the ambient temperature listed in Table 8 and the VDD supply voltage listed in Table 6.

Table 11 Embedded reset and power control module characteristics

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
VPVD	Programmable voltage detection	PLS[2:0]=000 (rising edge)	2.1	2.16	2.26	V

	Detector level selection	PLS[2:0]=000 (falling edge)	2	2.07	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.26	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.17	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.35	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.26	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.36	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.55	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.45	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.66	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.57	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.76	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.67	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.85	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.77	2.9	V
VPVDhyst(1)	PVD hysteresis	—	—	100	—	mV
VPOR/PDR	Power on/power down reset threshold	falling edge	—	1.90	—	V
		rising edge	—	2.02	—	V
VPDRhyst(1)	PDR hysteresis	—	—	30	—	mV
TRSTTEMPO(1)	reset duration	—	—	2	—	ms

(1) Guaranteed by design and not tested in production.

4.1.11 Built-in reference voltage

The parameters given in the table below are based on the ambient temperature listed in Table 8 and the VDD supply voltage listed in Table 6.

Table 12 Built-in reference voltage

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
VREFINT	Built-in reference voltage	- 40℃ < TA < +85℃	1.16	1.20	1.24	V
TS_vrefint(1)	When reading the internal parameters, When illuminating the voltage, the ADC sampling time	—	-	5.1	17.1	us

TCoeff (2)	Temperature Coefficient	—	—	—	100	ppm/℃

(1) The shortest sampling time is obtained through multiple loops in the application.

(2) Guaranteed by design and not tested in production.

4.1.12 Supply current characteristics

Current consumption is a comprehensive indicator of multiple parameters and factors, including operating voltage, ambient temperature, I/O pin Load, product software configuration, operating frequency, I/O pin toggle rate, program location in memory, and executed code wait.

For the current consumption measurement method description, please refer to the current consumption test quantity description in the test conditions chapter for details.

Current consumption

The microcontroller is under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are turned off unless otherwise stated.
- When peripherals are turned on: fPCLK1 = fHCLK/2, fPCLK2 = fHCLK.

Table 13 Current consumption in running mode

symbol	parameter	condition	htK	Typical value(1)		max(2)		one Bit
				enable all peripherals	Close all peripherals	enable all peripherals	Close all peripherals	
IDD	Run mode under the formula supply electricity flow	external clock (3)	216MHz	36.29	25.49	38.50	27.56	mA
			168MHz	27.71	19.27	29.95	21.35	
			72MHz	13.09	9.38	14.93	11.21	
			48MHz	9.35	6.93	11.18	8.74	
			32MHz	6.88	5.25	8.68	7.04	
			24MHz	5.67	4.46	7.41	6.20	
			16MHz	4.43	3.63	6.16	5.34	
			8MHz	3.28	2.58	4.98	4.54	
		running on high Speed internal RC Oscillator (HSI)	128MHz	21.64	15.19	23.89	17.27	mA
			72MHz	13.03	9.39	15.03	11.31	
			48MHz	9.34	6.92	11.26	8.78	
			32MHz	7.55	5.73	8.73	7.08	
			24MHz	5.69	4.49	7.74	6.24	
			16MHz	4.45	3.66	6.21	5.39	
			8MHz	3.30	2.88	5.02	4.57	

(1) Typical values are measured at TA=25℃ and VDD=3.3V.

(2) The maximum value is measured when TA=85℃ and VDD=3.6V.

(3) The external clock is 8MHz, and the PLL is enabled when fHCLK>8MHz.

Table 14 Current consumption in sleep mode, code running in Flash

symbol	parameter	condition	htK	Typical value(1)		max(2)		one Bit
				enable all peripherals	closing There are peripherals	enable all peripherals	Close all peripherals	
IDD	sleep mode under the formula supply electricity flow	external clock (3)	216MHz	25.72	7.01	27.73	8.70	mA
			168MHz	19.46	4.81	21.49	6.58	
			72MHz	9.53	3.25	11.31	4.92	
			48MHz	6.99	2.81	8.76	4.51	
			32MHz	5.32	2.54	7.07	4.23	
			24MHz	4.50	2.41	6.22	4.09	
			16MHz	3.66	2.28	5.36	3.96	
			8MHz	2.90	2.17	4.57	3.84	
		running on high Speed internal RC Oscillator (HSI)	128MHz	15.31	4.14	17.36	5.90	mA
			72MHz	9.47	3.20	11.36	4.93	
			48MHz	6.97	2.80	8.80	4.52	
			32MHz	5.32	2.54	7.11	4.26	
			24MHz	4.49	2.41	6.25	4.12	
			16MHz	3.65	2.27	5.39	3.98	
			8MHz	2.89	2.17	4.61	3.87	

(1) Typical values are measured when TA=25℃ and VDD=3.3V.

(2) The maximum value is measured when TA=85℃ and VDD=3.6V.

(3) The external clock is 8MHz, and the PLL is enabled when fHCLK>8MHz.

Table 15 Typical and maximum current consumption in shutdown and standby modes

symbol	parameter	condition	Typical value(1)	max(2)	unit
IDD	In shutdown mode supply current	The regulator is in run mode, low speed, high speed high-speed internal RC oscillator and external high-speed oscillator The machine is closed (no independent gate dog)	210	1290	uA
		The regulator is in low power mode, low speed, High-speed internal RC oscillator and external high-speed oscillator oscillator is off (no independent viewing guard dog)	130	1220	

	In standby mode supply current	Low-speed internal RC oscillator, external low-speed oscillator The oscillator, RTC and IWDG are closed	0.7	2.2	
		The low-speed internal RC oscillator is on status, external low-speed oscillator and RTC, IWDG is down	1.0	2.5	
		The external low-speed oscillator is on, Low-speed internal RC oscillator and RTC, IWDG is closed	1.0	2.6	
		External low speed oscillator and RTC are on status, low-speed internal RC oscillator and IWDG is closed	1.3	2.7	
		The low speed internal RC oscillator and IWDG are on on state, external low-speed oscillator and RTC is closed	1.0	2.7	
IDD_VBAT	backup area supply current	External low speed oscillator and RTC are on state	0.9	1.3	

(1) Typical values are measured when TA=25℃, VDD=VBAT=3.3V.

(2) The maximum value is measured when TA=85℃, VDD=VBAT=3.6V.

(3) Based on comprehensive evaluation and not tested in production

Built-in peripheral current consumption

The working conditions of the MCU are as follows:

- All I/O pins are in analog input mode
- All peripherals are turned off unless otherwise stated.
- The values given are calculated by measuring the current consumption
  - Turn off clocks to all peripherals
  - Only turn on the clock of one peripheral

Table 16 Current consumption of built-in peripherals

Built-in peripherals		Typical power consumption at 25℃	unit
APB1	TIM2	2.08	uA/MHz
	TIM3	2.36	
	TIM4	2.22	
	TIM5	2.08	
	TIM6	0.14	

	TIM7	0.14	
	SPI2/I2S	0.97	
	SPI3/I2S	0.83	
	USART2	0.56	
	USART3	0.56	
	UART4	0.56	
	UART5	0.56	
	I2C1	1.81	
	I2C2	1.81	
	USB	5.42	
	CAN	1.11	
	SDIO	7.92	
	WWDG	0.24	
	DAC	0.58	
	PWR	0.008	
	BKP	0.11	
APB2	ADC1(1)	5	
	ADC2(1)	5	
	ADC3(1)	5	
	TIM1	3.71	
	TIM8	3.76	
	SPI1	1.83	
	USART1	1.39	

(1) Special conditions for ADC: fHCLK=56MHz, fAPB1 = fHCLK/2, fAPB2 = fHCLK, fADCCLK = fAPB2/4,

ADC_CR2

ADON=1 in the register.

4.1.13 External clock source characteristics

High-speed external user clock generated from external oscillator source

The characteristic parameters given in the following table are measured using a high-speed external clock source. The ambient temperature and supply voltage comply with Table 6 and Table 8.

condition.

Table 17 High-speed external user clock characteristics

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
fHSE_ext	User external clock frequency(1)	—	0.615	8	35	MHz

VHSEH	OSC_IN input pin high level voltage press		0.48Vdd	—	Vdd	V
VHSEL	OSC_IN input pin low level voltage press		Vss	—	0.38Vdd	
tw(HSE) tw(HSE)	OSC_IN high or low time(1)		5	62.5	—	ns
tr(HSE) tf(HSE)	OSC_IN rise or fall time (1)		—	4.1	20	
Cin(HSE)	OSC_IN input capacitive reactance(1)	—	—	5	—	pF
DuCy(HSE)	duty cycle	—	45	50	55	%

(1) Guaranteed by design and not tested in production.

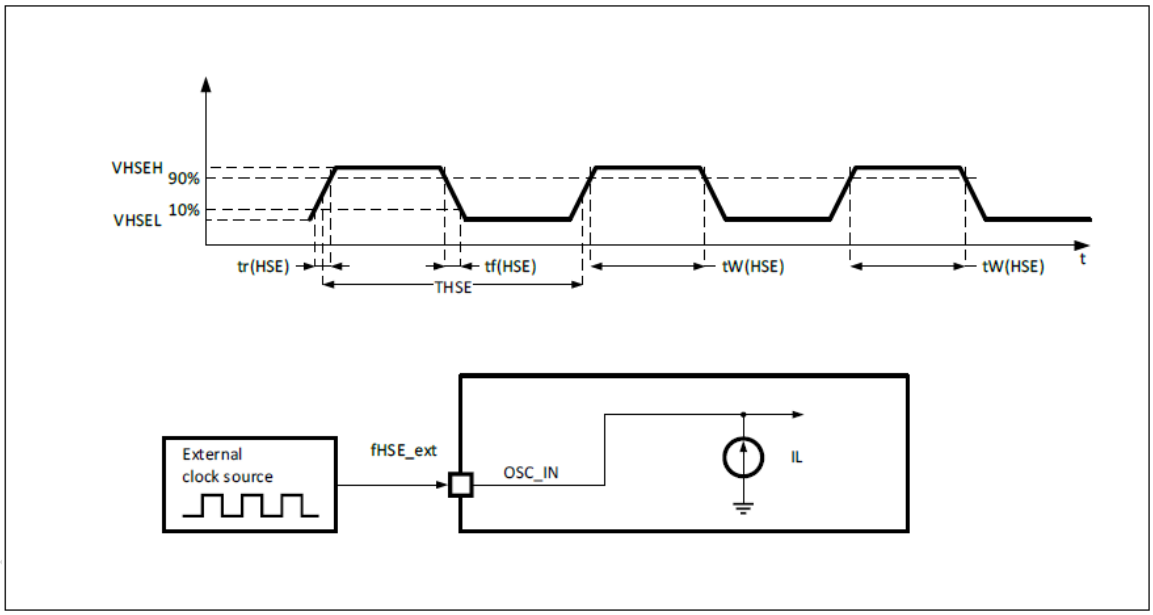


Figure 7 AC timing diagram of external high-speed clock source

Low-speed external user clock generated from external oscillator source

The characteristic parameters given in the following table are measured using a low-speed external clock source. The ambient temperature and supply voltage comply with Table 6 and Table 8.

condition.

Table 18 Low-speed external user clock characteristics

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
fHSE_ext	User external clock frequency(1)	—	—	32.768	1000	KHz
vLSE	OSC32_IN input pin high level voltage		0.48Vdd	—	VDD	V
VLSEL	OSC32_IN input pin low level voltage		VSS	—	0.38Vdd	
tw(LSE) tw(LSE)	OSC32_IN high or low time(1)		450	—	—	ns

tr(LSE) tf(LSE)	OSC32_IN rise or fall time (1)		—	—	50	
Cin(LSE)	OSC32_IN input capacitive reactance(1)	—	—	5	—	pF
DuCy(LSE)	duty cycle	—	30	—	70	%

(1) Guaranteed by design, not tested in production.

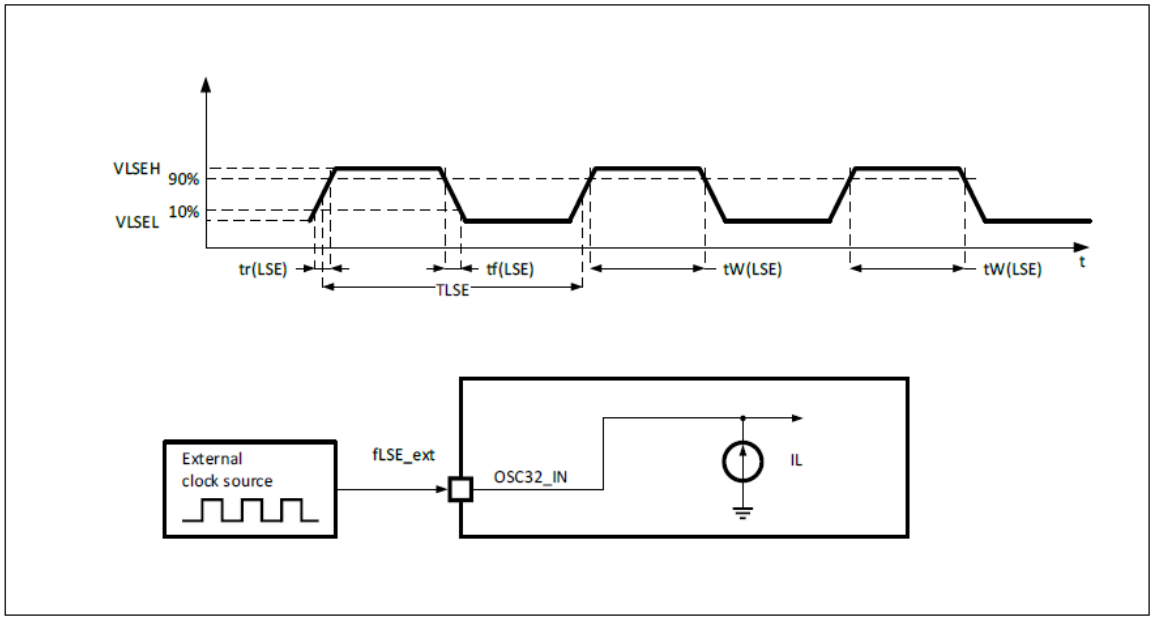


Figure 8 AC timing diagram of external low-speed clock source

High-speed external clock generated using a crystal/ceramic resonator

The high-speed external clock (HSE) can be generated using a 4~32MHz crystal/ceramic resonator oscillator. The letter given in this section Information is based on a comprehensive characteristic evaluation using typical external components listed in the table below. In applications, resonators and The load capacitor must be placed as close as possible to the oscillator pins to reduce output distortion and settling time at startup. About crystal resonators For detailed parameters (frequency, packaging, accuracy, etc.), please consult the corresponding manufacturer. (Annotation: The crystal resonator mentioned here is me We usually call passive crystal oscillator)

Table 19 HSE 4~32MHz oscillator characteristics (1) (2)

symbol	parameter	condition		minimum value	Typical value	maximum value	unit
fOSC_IN	Oscillator frequency	—		4	8	32	MHz
tSU(HSE)(5)	Start Time	VDD is stable of	TA = -40℃	—	790	—	us
			TA = 25℃	—	860	—	
			TA = 85℃	—	960	—	

(1) Characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

(2) Derived from comprehensive evaluation and not tested in production.

(3) tSU(HSE) is the startup time, which is measured from when the software enables HSE until a stable 8MHz oscillation is obtained. This number

Values are measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For CL1 and CL2, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications (typically) between 5 pF and 25 pF.

device,

And select a crystal or resonator that meets the requirements. Usually CL1 and CL2 have the same parameters. Crystal manufacturers typically designate CL1 and CL2 as serial

The combination gives the parameters of the load capacitance. When selecting CL1 and CL2, the capacitive reactance of the PCB and MCU pins should be taken into account (this can be roughly

lead

The capacitance between the pin and the PCB board is estimated to be 10 pF).

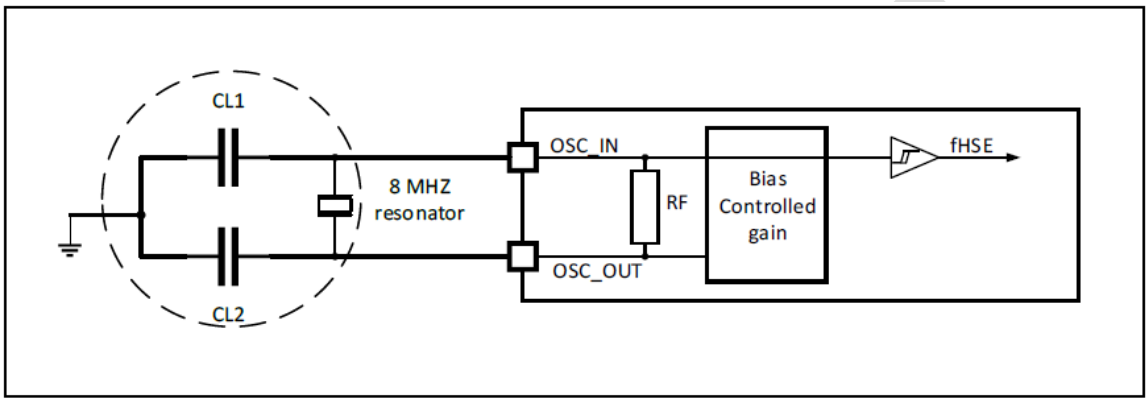


Figure 9 Typical application using 8MHz crystal

Low speed external clock generated using a crystal/ceramic resonator

The low-speed external clock (LSE) can be generated using a 32.768kHz crystal/ceramic resonator oscillator. given in this section

Information is the result of a comprehensive property evaluation. In the application, the resonator and load capacitor must be as close as possible to the oscillator leads.

pin to reduce output distortion and settling time at startup. For detailed parameters of the crystal resonator (frequency, packaging, accuracy, etc.), please consult

Consult the appropriate manufacturer. (Annotation: mentioned herecrystal resonator That's what we usually sayPassive crystal oscillator)

Table 20 LSE oscillator characteristics (fLSE=32.768kHz)(1)

symbol	parameter	condition		smallest value	typical value	maximum value	unit
tSU(HSE)(5)	Start Time	VDD is stable of	TA = -40℃	—	321	—	ms
			TA = 25℃	—	221	—	
			TA = 85℃	—	223	—	

(1) Based on comprehensive evaluation and not tested in production.

For CL1 and CL2, it is recommended to use high-quality ceramic capacitors between 5 pF and 15 pF, and select a crystal or resonance that meets the requirements.

device. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually specify the load capacitance as a serial combination of CL1 and CL2.

The load capacitance CL is calculated by: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray is the capacitance of the pin and

PCB board or PCB related capacitance, its typical value is between 2 pF and 7 pF.

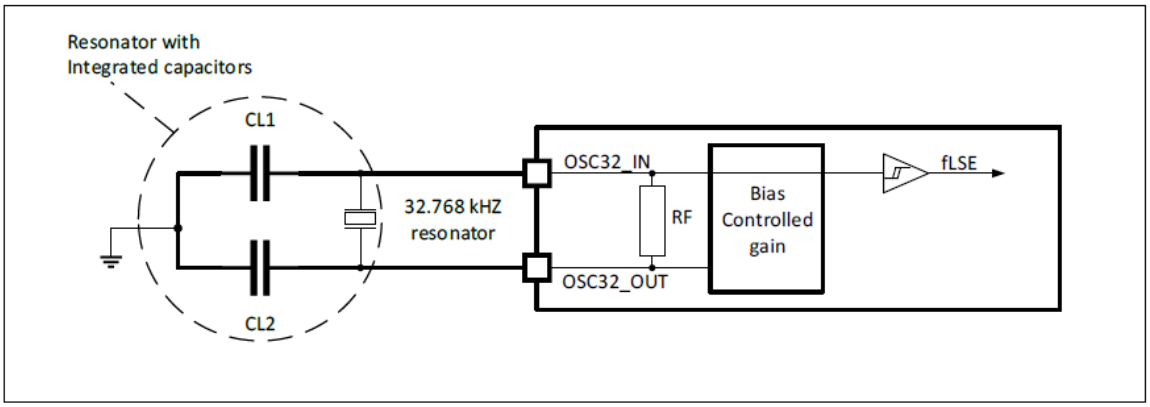


Figure 10 Typical application using 32.768KHz crystal

4.1.14 Internal clock source characteristics

The characteristic parameters given in the following table are measured using the conditions of ambient temperature and supply voltage that comply with Table 8 and Table 6.

High Speed Internal (HSI) RC Oscillator

Table 21 HSI Oscillator Characteristics(1)

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
fHS	frequency	—	—	8	—	MHz
ACCHSI	HSI Oscillator Accuracy	TA = -40~85℃	- 2.5	—	2.5	%
		TA = 0~70℃	- 1	—	1	%
		TA = 25℃	- 0.5	—	0.5	%
tSU(HSI)	When the HSI oscillator starts between	—	—	12	—	us
IDD(HSI)	HSI oscillator power consumption	—	—	3.5	—	uA

(1) VDD = 3.3V, TA = -40~85℃, unless otherwise specified.

Low Speed Internal (LSI) RC Oscillator

Table 22 LSI oscillator characteristics (1)

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
fLSI(2)	frequency	—	33	40	43	kHz
tSU(LSI)(3)	When LSI oscillator starts between	—	—	75	—	us
IDD(LSI)(3)	LSI oscillator power consumption	—	—	0.28	—	uA

(1) VDD = 3.3V, TA = -40~85℃, unless otherwise specified.

(2) Based on comprehensive evaluation and not tested in production

(3) Guaranteed by design, not tested in production

4.1.15 Time to wake up from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up should be

Depends on the previous operating mode:

- Stop or standby mode: clock source is RC oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage conditions consistent with Table 8 and Table 6.

Table 23 Wake-up time in low power mode

symbol	parameter	Typical value	unit
tWUSLEEP(1)	Wake up from sleep mode	10	CPU clock cycle
tWUSTOP(1)	Wake up from shutdown mode (regulator is in low power mode)	12	us
tWUSTDBY(1)	Wake up from standby mode	1600(2)/260(3)	us

(1) The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

(2) For large capacity series

(3) For small capacity series

4.1.16 PLL characteristics

The parameters listed in the following table are measured using the conditions of ambient temperature and power supply voltage consistent with Table 8 and Table 6.

Table 24 PLL characteristics

symbol	parameter	numerical value			unit
		minimum value	Typical value	max(1)	
fPLL_IN	PLL input clock(2)	2	8	32	MHz
	PLL input clock duty cycle	40	—	60	%
fPLL_OUT	PLL multiplied output clock	4	—	216	MHz
tLOCK	PLL phase lock time	—	51.2	87.8	us
Jitter	cycle jitter	—	—	200	PS

(1) Based on comprehensive evaluation and not tested in production.

(2) It is necessary to pay attention to using the correct frequency multiplication factor so that fPLL_OUT is within the allowable range according to the PLL input clock frequency.

4.1.17 Memory characteristics

flash memory

Unless otherwise stated, all characteristic parameters are obtained at TA = -40~85℃.

Table 25 Flash memory characteristics

symbol	parameter	condition	Typical value	unit
tPROG	16-bit programming time	—	50us	us
tERASE	Page erase time	—	25	ms
tME	Whole chip erase time	—	3	s

Table 26 Flash memory life and data retention period

symbol	parameter	condition	minimum(1)	typical value	maximum value	unit
NEND	Lifespan (Annotation: erasing times number)	TA = -40~85℃	100	—	—	Thousands of times
tRET	Data retention period	TA = 105℃	20	—	—	Year

(1) Based on comprehensive evaluation and not tested in production.

4.1.18 Absolute maximum value (electrical sensitivity)

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse after one second) is applied to all pins of all samples.

The small size is related to the number of power supply pins on the chip (3 pieces x (n+1) power supply pins). This test complies with the JEDEC EIA/JESD22-A114 standard.

Table 27 ESD absolute maximum values

symbol	parameter	condition	type	maximum value**(1)**	unit
VESD(HBM)	Electrostatic discharge voltage (human body Model)	TA = +25 °C, conforming to JEDEC EIA/JESD22-A114	3A	4000	V

(1) Based on comprehensive evaluation and not tested in production.

4.1.19 I/O port characteristics

Universal input/output features

Unless otherwise specified, the parameters listed in the following table are measured in accordance with the conditions in Table 8 and Table 6. All I/O ports are CMOS and TTL compatible.

Table 28 I/O static characteristics

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
VIL	Input low level voltage	—		—	1.38	V
VIH	Standard I/O pin, input high level Voltage		1.59	—	—	

	FT I/O pin (1), input high power flat voltage		1.59	—	—	
Vhys	Standard I/O pin Schmitt trigger Voltage hysteresis(2)	—	—	0.21	—	V
	5V tolerant I/O pin Schmitt trigger device voltage hysteresis(2)		—	0.21	—	V
Ilkg	Input leakage current(4)	VSS ≤ VIN ≤ VDD Standard I/O port	—	—	±0.5	uA
		VIN = 5V, 5V tolerant port	—	—	±1	
RPU	Weak pull-up equivalent resistance(5)	VIN = VSS	37	—	38.5	kΩ
RPD	Weak pull-down equivalent resistance(5)	VIN = VDD	43.7	—	45.7	kΩ
CIO	I/O pin capacitance			5		pF

The output voltage

Unless otherwise specified, the parameters listed in the following table are measured using the conditions of ambient temperature and VDD supply voltage consistent with Table 8 and Table 6. all

All I/O ports are CMOS and TTL compatible.

Table 29 Output voltage characteristics

symbol	parameter	condition	minimum value	maximum value	unit
VOL	Output low level	TTL port, I_{IO}= +12mA		0.4	V
VOH	Output high level	VDD=3.3V	2.9		
VOL	Output low level	CMOS port, I_{IO}= +14mA		0.4	
VOH	Output high level	VDD=3.3V	2.9		
VOL	Output low level	I_{IO}= +34mA		1.3	
VOH	Output high level	VDD=3.3V	2		

4.1.20 NRST pin characteristics

The NRST pin input driver uses CMOS technology and is connected to a pull-up resistor, RPU, that cannot be disconnected (see Table 27).

Unless otherwise specified, the parameters listed in the following table are measured using the conditions of ambient temperature and supply voltage consistent with Table 8 and Table 6.

Table 30 NRST pin characteristics

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
VIL(NRST)(1)	NRST input low level voltage	—	—	1.31	—	V
VIH(NRST)(1)	NRST input high level voltage	—	—	1.57	—	
Vhys(NRST)	NRST Schmitt trigger voltage hysteresis	—	—	260	—	mV
RPU	Weak pull-up equivalent resistance(2)	VIN=VSS	—	37	—	kΩ
VF(NRST)(1)	NRST input filter pulse	—	—	120	—	ns
VNF(NRST)(1)	NRST input unfiltered pulse	—	25	—	—	ns

(1) Guaranteed by design and not tested in production.

Recommended NRST pin protection

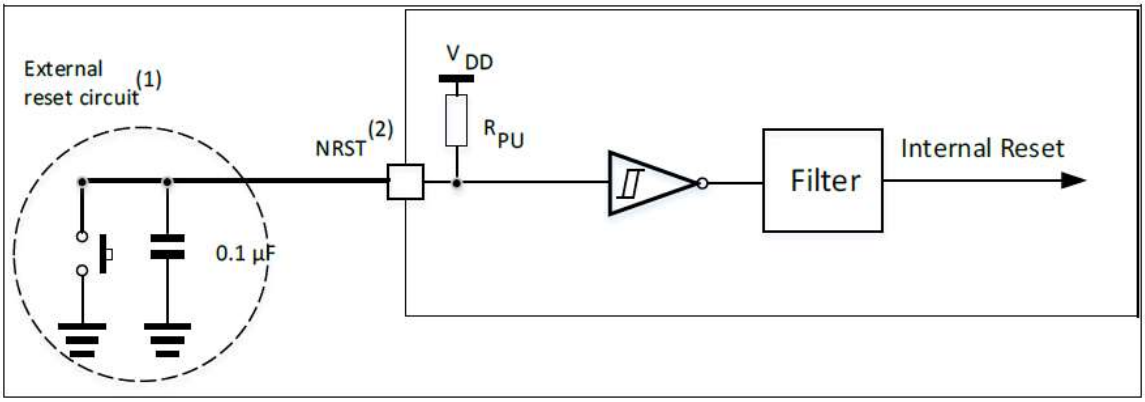


Figure 11 Recommended NRST pin protection

(1) The reset network is to prevent spurious resets.

(2) The user must ensure that the potential of the NRST pin can be lower than the maximum VIL (NRST) listed in Table 30, otherwise the MCU cannot be restored.

Bit.

4.1.21 TIM timer characteristics

The parameters listed in the table below are guaranteed by design.

Table 31 TIMx characteristics

symbol	parameter	minimum value	maximum value	unit
tres(TIM)	timer resolution time	1	—	tTIMxCLK
fEXT	When the timer of CH1 to CH4 is external clock frequency	0	FTIMCLK/2	MHz
ResTIM	Timer resolution	—	16	Bit

tCOUNTER	When the internal clock is selected, 16 bit counter clock period	1	65535	tTIMxCLK
tMAX_COUNT	maximum possible count	—	65535*65535	tTIMxCLK

4.1.22 CAN (Controller Area Network) interface

Regarding input and output multiplex function pins (CAN_TXandCAN_RX)For details on the features, see the IO port features chapter.

4.1.23 12-bit ADC characteristics

Unless otherwise specified, the parameters in the following table are measured using the ambient temperature, fPCLK2 frequency and VDDA supply voltage that comply with the conditions of Table 8 and Table 6.

The amount is obtained.

Note: It is recommended to perform a calibration at each power-up.

Table 32 ADC characteristics

symbol	parameter	condition	minimum value	Typical value	maximum value	unit
VDD	Supply voltage	—	2.3	3.3	3.6	V
VREF+	Positive reference voltage	—	2.3	—	VDD	V
fADC	ADC clock frequency	—	0.6	—	14	MHz
fS(2)	Sampling rate	—	0.05	—	1	MHz
fTRIG(2)	External trigger frequency	fADC = 14MHz	—	—	823	kHz
VAIN	Conversion voltage range(3)	—	0		VREF+	V
RAIN(2)	External input impedance	—	—	—	50	kΩ
RADC(2)	Sampling switch resistance	—	—	—	1	kΩ
CADC(2)	Internal sample and hold circuits Allow	—	—	—		pF
tCAL(2)	Calibration time	fADC = 14MHz	5.9			us
			83			1/fADC
tlat(2)	Injection trigger conversion delay Late	fADC = 14MHz	—	—	0.214	us
			—	—	3	1/fADC
tlatr(2)	Normal Trigger Conversion Delay Late	fADC = 14MHz	—	—	0.143	us
			—	—	2	1/fADC
tS(2)	sampling time	fADC = 14MHz	0.107	—	17.1	us

			1.5	—	239.5	1/fADC
tSTAB(2)	Power on time	—	0	0	1	us
tCONV(2)	Total conversion time (including (including sampling time)	fADC = 14MHz			18	us
			14 to 252 (ts+ 12.5 for successive forcing close)			1/fADC

(1) Guaranteed by comprehensive evaluation and not tested in production.

(2) Guaranteed by design and not tested in production.

(3) Depending on the package, VREF+ can be connected internally to VDDA, and VREF- can be connected internally to VSSA. See Chapter 3 for details.

(4) For external triggering, a delay of 1/fPCLK2 must be added to the delays listed in Table 32.

Table 33 Maximum RAIN when fADC=14MHz(1)

TS(period)	tS(us)	Maximum RAIN(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	-
239.5	17.11	-

(1) Guaranteed by design and not tested in production.

4.1.24 DAC electrical parameters

Table 34 DAC characteristics

symbol	parameter	smallest value	typical value	maximum value	unit	Comment
VDD	Analog supply voltage	2.0	-	3.6V	V	
VREF+	Reference voltage	2.0	-	3.6V	V	VREF+ must always be lower than vDDA
VSSA	Ground wire	0	-	0	V	-
RLOAD(1)	Load with buffer open resistance	5	-	-	kΩ	-
RO(2)	Output with buffer closed impedance	-	-	15	kΩ	-

CLOAD(1)	load capacitance	-	-	50	pF	on the DAC_OUT pin Large capacitor (buffer on hour)
DAC_OUT small(1)	The buffer is open when the low-end DAC_OUT voltage	50	-	-	mV	gives the maximum DAC output out span
DAC_OUTlarge(1)	When the buffer is turned on, the high-end DAC_OUT voltage	-	-	VREF+ - 0.2	V	
DAC_OUT small(1)	The buffer is closed when the low-end DAC_OUT voltage	-	0.5	-	mV	gives the maximum DAC output out span
DAC_OUTlarge(1)	The buffer is closed when the high-end DAC_OUT voltage	-	-	VREF+ - 0.03	V	
I	In static mode (standby mode (Formula) DAC DC consumption	-	-	1.2	mA	No load, output Code for x800
DNL(2)	Non-linear distortion (2 consecutive Deviation between codes-1LSB)	-	-	+ - 2	LSB	DAC configured as 12-bit
INL(2)	Nonlinear accumulation (in code i Values and codes measured at the time DAC_OUT Yamato code The connection between DAC_OUT deviation between)	-	-	+ - 4	LSB	DAC configured as 12-bit
Offset error(2)	Offset error (code 0x800 value measured at With the ideal value V REF+ /2 deviation between	-	15	25	mV	VREF+ = 3.3 V, DAC configured as 12-bit
tSETTLING	Set time (full range: 10 bit input code to convert from small value becomes a large value, DAC_OUT reaches ±1 of its final value LSB)	-	3	4	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
update rate	When the input code is smaller, the When changing (from value i to i+1 LSB), get the correct Maximum frequency of DAC_OUT	-	-	1	MS/s	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
tWAKEUP	When waking up from off state	-	6.5	10	us	C LOAD ≤ 50 pF,

	time (set DAC control register ENx bit in the register)					R LOAD ≥ 5kΩlose Enter code between small and large Can between values
PSRR+ (1)	Supply Rejection Ratio (relative to V DDA) (static DC measurement)	-	- 60	- 50	dB	No R LOAD, C LOAD ≤ 50 pF

(1) Guaranteed by design, not tested in production.

(2) Guaranteed by comprehensive evaluation and not tested in production.

4.1.25 Temperature sensor characteristics

Table 35 Temperature sensor characteristics

symbol	parameter	minimum value	Typical value	maximum value	unit
Avg_Slope(1)	average slope	—	5	—	mV/°C
V25(1)	Voltage at 25°C	—	1.43(4)/ 1.18(5)	—	V
tSTART(2)	Setup time	—	—	10	us
TS_temp(2)(3)	When reading the temperature, the ADC sampling time	—	—	17.1	us

(1) Guaranteed by comprehensive evaluation and not tested in production.

(2) Guaranteed by design and not tested in production.

(3) The shortest sampling time can be determined by the application program through multiple loops.

(4) For large capacity series

(5) For small capacity series

Use the following formula to find the temperature:

Temperature (°C) = {(V25 – VSENSE) / Avg_Slope} + 25

Here(1):

V25 = VSENSE value at 25 °C

Avg_Slope = average slope of temperature vs. VSENSE curve (unit is mV/°C)

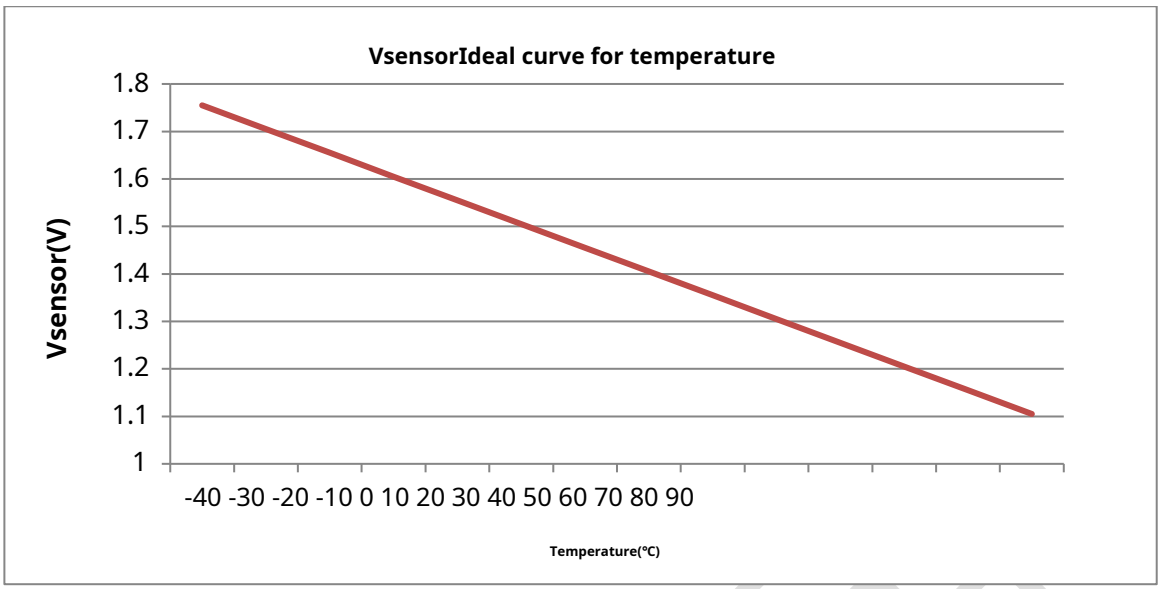


Figure 12 V SENSE versus temperature ideal curve (1)

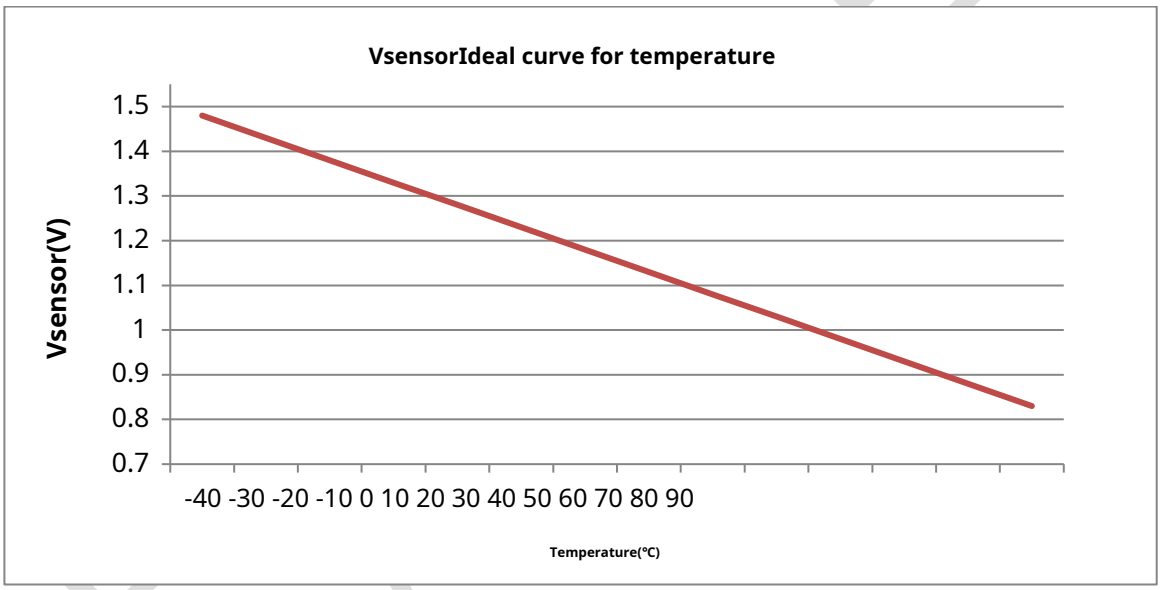
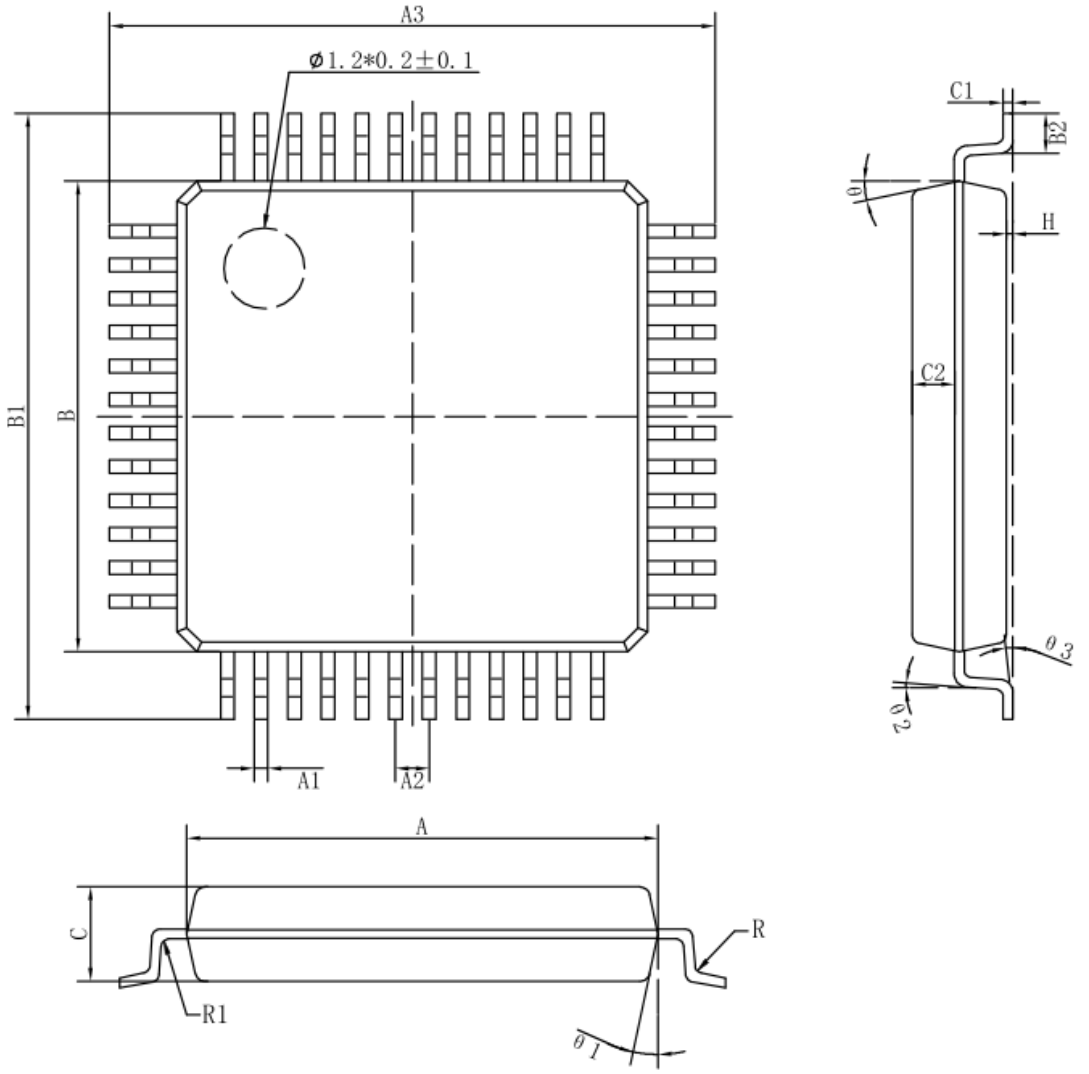


Figure 13 V SENSE versus temperature ideal curve (2)

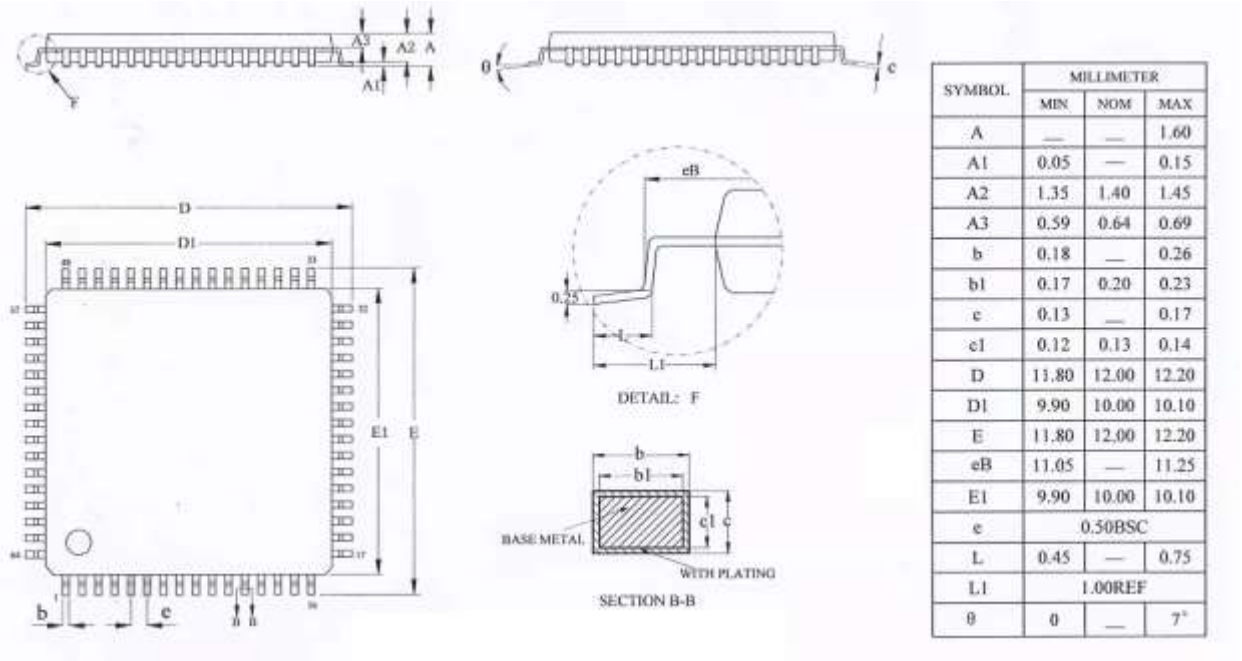
LQFP48 package



尺寸 / 标注	最小(mm)	最大(mm)	尺寸 / 标注	最小(mm)	最大(mm)
A	6.90	7.10	C2	0.636TYP	
A1	0.20TYP		H	0.05	0.15
A2	0.50TYP		θ	12° TYP4	
A3	8.80	9.20	θ1	12° TYP4	
B	6.90	7.10	θ2	4° TYP	
B1	8.80	9.20	θ3	0° ~ 5°	
B2	0.50	0.80	R	0.15TYP	
C	1.30	1.50	R1	0.12TYP	
C1	0.127	0.16			

Figure 14 LQFP48 7mm×7mm package size

LQFP64 package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	—	11.25
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 15 LQFP64 10mm×10mm package size

6appendix

Table 36 Document version history

date	Version	change
2022-06-01	1.00	initial version