Datasheet

cks32f103x8
cks32f103xb

32-bit ARM core-based standard microcontrollers with 64 or 128K bytes of flash memory

functionality

■Core: ARM 32-bit Cortex™-M3 core

- Up to 72MHz operating frequency, up to 1.25DMips/MHz at 0 wait-cycle memory access (Dhrystone2.1)
- Single-cycle multiplication and hardware division

■memory (unit)

- 64KB or 128KB Program Flash
- 20KB SRAM

■Clock, reset and power management

- 2.0 to 3.6 volt power supply and I/O pins
- Power On/Power Off Reset (POR/PDR), Programmable Voltage Monitor (PVD)
- 4～16MHz Crystal Oscillator
- Embedded factory-tuned 8MHz high-speed RC oscillator
- Embedded 40kHz low-speed RC oscillator with calibration
- PLL for generating CPU clock
- 32kHz RTC oscillator with calibration function

■Two 12-bit ADCs with 1μs conversion time (up to 16 input channels)

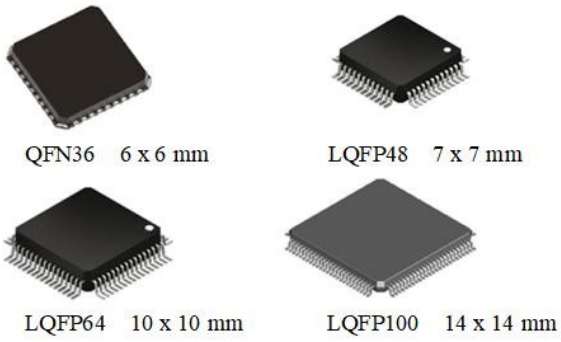
- Conversion range: 0 to 3.6V
- Dual sample and hold function
- temperature sensor

■DMA:

- 7-Channel DMA Controller
- Supported peripherals: Timer, ADC, SPI, I2C and USART

■low power

- Sleep, shutdown and standby modes
- VBAT supplies power to the RTC and backup registers



■Up to 80 fast I/O ports

- 26/37/51/80 I/O ports, all I/O ports can be mapped to 16 external interrupts; almost all ports can withstand 5V signals

■debug mode

- Serial Single Wire Debug (SWD) and JTAG interfaces

■7 timers

- Three 16-bit timers, each with up to four channels for input capture/output compare/PWM or pulse counting and incremental encoder inputs
- 1 x 16-bit PWM Advanced Control Timer with Deadband Control and Emergency Brake for motor control
- 2 watchdog timers (standalone and windowed)
- System time timer: 24-bit self-subtracting counter

■Up to 9 communication interfaces

- Up to 2 I2C interfaces (SMBus/PMBus support)
- Up to 3 USART interfaces (supports ISO7816 interface, LIN. IrDA interface and modem control)
- Up to 2 SPI interfaces (18M bits/sec)
- CAN interface (2.0B active)
- USB 2.0 Full Speed Interface

- **CRC calculation unit, 96-bit chip unique identifier**

CKS32F103x8 and CKS32F103xB, a series of 32-bit MCUs from Semiconductor Manufacturing Corp.

Device Comparison

CKS32F103x8(B) Product Features and Peripheral Configuration

Peripheral Interface \ Product Model		CKS32F103T8/TB	CKS32F103C8/CB		CKS32F103R8/RB		CKS32F103VB
Flash memory - K bytes		64	64	128	64	128	128
SRAM- K bytes		20	20		20		20
timed (of explosive etc) tool	general purpose	3	3		3		3
	Advanced Controls	1	1		1		1
communications interface	SPI	1	2		2		2
	I2C	1	2		2		2
	USART	2	3		3		3
	USB	1	1		1		1
	CAN	1	1		1		1
GPIO ports (number of channels)		26	37		51		80
12-bit Synchronous ADC (Number of channels)		2 10 channels	2 10 channels		2 16 channels		2 16 channels
CPU frequency		72 MHz					
operating voltage		2.0V ~3.6V					
operating temperature		Ambient temperature: -40℃~ +85℃/-40℃~+105℃ Junction temperature: -40℃~+125℃					
seal inside		QFN36	LQFP48		LQFP64		LQFP100

Ordering Information

palletized

Product Model	Package form	Number of trays	boxed tray	Number of boxes	boxed	cartons
CKS32F103T8T6	QFN36	490PCS/Tray	10 trays/box	4900PCS/box	6 boxes/carton	29400PCS/Carton
CKS32F103TBT6	QFN36	490PCS/Tray	10 trays/box	4900PCS/box	6 boxes/carton	29400PCS/Carton
CKS32F103C8T6	LQFP48	250PCS/Tray	10 trays/box	2500PCS/box	6 boxes/carton	15000PCS/Carton
CKS32F103CBT6	LQFP48	250 PCS/tray	10 trays/box	2500PCS/box	6 boxes/carton	15000 PCS/box
CKS32F103R8T6	LQFP64	160 PCS/plate	10 trays/box	1600 PCS/box	6 boxes/carton	9600 PCS/box
CKS32F103RBT6	LQFP64	160 PCS/disk	10 trays/box	1600 PCS/box	6 boxes/carton	9600 PCS/box
CKS32F103VBT6	LQFP100	90 PCS/plate	10 trays/box	900 PCS/box	6 boxes/carton	5400 PCS/box

catalogs

1. present (sb for a job etc)

This document gives the device characteristics of the CKS32F103x8 and CKS32F103xB standard MCU products.

The CKS32F103x8 and CKS32F103xB datasheets must be read in conjunction with their associated reference manuals.

For information about the Cortex™-M3 core, please refer to the Cortex-M3 Technical Reference Manual, available for download from ARM's website:

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2. Specification

The CKS32F103x8 and CKS32F103xB standard MCU series utilize a high-performance ARM® Cortex™-M3 32-bit RISC core operating at 72MHz, with built-in high-speed memories (up to 128K bytes of Flash and 20K bytes of SRAM), a rich set of enhanced I/O ports, and peripherals connected to two APB buses. Two 12-bit ADCs, three general-purpose 16-bit timers, and a PWM timer are included, along with standard and advanced communication interfaces: up to two I2C and SPI interfaces, three USART interfaces, a USB interface, and a CAN interface.

The CKS32F103x8 and CKS32F103xB standard MCUs are available with supply voltages from 2.0V to 3.6V, an operating temperature range of -40°C to +85°C, and an extended temperature range of -40°C to +105°C, with a range of power-saving modes to ensure that low-power applications are required.

The CKS32F103x8 and CKS32F103xB standard series are available in four different packages ranging from 36 pins to 100 pins; the peripheral configurations in the devices vary depending on the package. A basic description of all the peripherals in this family is given below.

These extensive peripheral configurations enable the CKS32F103x8 and CKS32F103xB standard series microcontrollers to be used in a wide variety of applications:

- Motor drives and application control
- Medical and handheld devices
- PC gaming peripherals and GPS platforms
- Industrial applications: programmable logic controllers (PLCs), inverters, printers and scanners
- Alarm systems, video intercom and HVAC systems, etc.

2.1 summarize

2.1.1 ARM® 's Cortex™-M3 core with embedded Flash and SRAM

ARM's Cortex™-M3 processor is the latest generation of embedded ARM processors, providing the low-cost platform, reduced pin count and reduced system power consumption needed to implement MCUs, while delivering superior computational performance and advanced interrupt system response.

ARM's Cortex™-M3 is a 32-bit RISC processor that provides additional code efficiency, utilizing the high performance of the ARM core in the storage space typically found in 8- and 16-bit systems.

The CKS32F103x8 and CKS32F103xB standard series have a built-in ARM core, so it is compatible with all ARM tools and software. **Error! Unrecognized switch parameters.** This is the functional block diagram of this series.

2.1.2 internal flash memory

64K or 128K bytes of internal flash memory for programs and data.

2.1.3 CRC (Cyclic Redundancy Check) calculation unit

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to produce a CRC code from a 32-bit data word. In numerous applications, CRC-based techniques are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting errors in flash memory, the CRC calculation unit can be used to compute the signature of software in real time and compare it with the signature generated at the time of linking and generating that software.

2.1.4 Internal SRAM

20K bytes of internal SRAM that can be accessed (read/write) by the CPU with 0 wait cycles.

2.1.5 Nested Vectorized Interrupt Controller (NVIC)

The CKS32F103x8 and CKS32F103xB standard models have a built-in nested vectorized interrupt controller capable of handling up to 43 maskable interrupt channels (excluding 16 Cortex™-M3 interrupt lines) and 16 priority levels.

- Tightly coupled NVICs enable low-latency interrupt response processing
- Interrupt vector entry address directly into the kernel
- Tightly Coupled NVIC Interface
- Allow early processing of interrupts
- Handling late arriving higher priority interrupts
- Support for interrupting the tail link function
- Automatic saving of processor state
- Auto-resume on return from interrupt, no additional instruction overhead required

The module provides flexible interrupt management capabilities with minimal interrupt latency.

2.1.6 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains 19 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising or falling edge or double edge) and can be individually masked; a pending register maintains the status of all interrupt requests. EXTI can detect pulses with a width less than the clock period of the internal APB2. Up to 80 general-purpose I/O ports are connected to 16 external interrupt lines.

2.1.7 Clock and startup

The selection of the system clock is done at startup, the internal 8MHz RC oscillator is selected as the default CPU clock at reset, then an external 4-16MHz clock with failure monitoring can be selected; when an external clock failure is detected, it is isolated and the system automatically switches to the internal RC oscillator, and if interrupts are enabled, the software receives the corresponding interrupts. Similarly, the PLL clock can be fully isolated when needed.

of interrupt management (e.g., when an external oscillator used during a period fails).

Multiple prescalers are used to configure the frequency of the AHB, the high speed APB (APB2), and the low speed APB (APB1) regions. the maximum frequency of the AHB and high speed APB is 72MHz, and the maximum frequency of the low speed APB is 36MHz. refer to the Clock Driver Block Diagram as shown in Figure 2.

2.1.8 bootstrap model

At startup, one of three bootstrap modes can be selected via the bootstrap pin:

- Bootstrap from program flash memory
- Bootstrap from system memory
- Bootstrap from internal SRAM

The bootloader is stored in system memory and can be reprogrammed to flash memory via USART1.

2.1.9 Power supply program

- V_{DD} = 2.0 to 3.6V: The V_{DD} pin powers the I/O pins and the internal regulator.
- V_{SSA}, V_{DDA} = 2.0 to 3.6V: Provides power to the analog portion of the ADC, reset module, RC oscillator, and PLL. Using the ADC
  V_{DDA} must not be less than 2.4 V. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
- V_{BAT} = 1.8 to 3.6V: When V_{DD} is turned off, power is supplied (via the internal power switcher) to the RTC, external 32kHz oscillator, and back-up registers.

For more information on how to connect the power supply pins, see Figure 10 Power Supply Scheme.

2.1.10 Power supply monitor

A power-on reset (POR)/power-down reset (PDR) circuit is integrated into the device, which is always active to ensure that the system operates when the power supply exceeds 2V; when V_{DD} falls below the set threshold ($V_{POR/PDR}$), the device is placed in reset without the need for an external reset circuit. The device also includes a programmable voltage monitor (PVD) that monitors the V_{DD}/V_{DDA} supply and compares it to the threshold V_{PVD}, generating an interrupt when V_{DD} falls below or rises above the threshold V_{PVD}, which can be used by the interrupt handler to issue a warning message or to transfer the microcontroller to a safe mode The PVD function needs to be programmed to enable it. Refer to Table 8 for $V_{POR/PDR}$ and V_{PVD} values.

2.1.11 regulator

The regulator has three modes of operation: main mode (MR), low power mode (LPR) and shutdown

mode

- Main mode (MR) for normal runtime operation
- Low power mode (LPR) for CPU shutdown mode
- Shutdown mode is used in standby mode of the CPU: the output of the regulator is high-resistance, the power supply to the core circuitry is cut off, and the regulator is in a zero-consumption state (but the contents of the registers and SRAM will be lost).

The regulator is always active after reset and shuts down in standby mode at the high resistance output.

2.1.12 Low Power Mode

The CKS32F103x8 and CKS32F103xB standard products support three low-power modes that provide an optimal balance between the requirement for low power consumption, short start-up times and multiple wake-up events.

- **sleep mode**

In sleep mode, only the MCU is stopped and all peripherals are active and can wake up the MCU in case of an interrupt/event.

- **shutdown mode**

The shutdown mode achieves the lowest power consumption while maintaining no loss of SRAM and register contents. In shutdown mode, all internal 1.5V sections are de-energized, the PLL, the HSI's RC oscillator, and the HSE crystal oscillator are turned off, and the regulator can be placed in either normal mode or low-power mode.

The microcontroller can be woken up from shutdown mode by any signal configured as EXTI, which can be one of the 16 external I/O ports, the output of the PVD, an RTC alarm, or a USB wake-up signal.

- **standby mode**

Minimal power consumption can be achieved in standby mode. The internal voltage regulator is switched off, so that all internal 1.5V sections are disconnected; the PLL, the RC oscillator of the HSI and the HSE crystal oscillator are also switched off; by entering the standby mode, the contents of the SRAM and the registers are lost, but the contents of the backup registers remain, and the standby circuits are still working.

Exiting from standby mode is conditional on an external reset signal on NRST, an IWDG reset, a rising edge on the WKUP pin or a
RTC when the alarm occurs.

NOTE: *The RTC*, *IWDG* and their corresponding clocks are not stopped when entering shutdown or standby mode.

2.1.13 DMA

Flexible 7-way general-purpose DMA manages memory-to-memory, device-to-memory, and memory-to-device data transfers; the DMA controller supports ring buffer management, avoiding interrupts when controller transfers reach the end of the buffer.

Each channel has dedicated hardware DMA request logic, while each channel can be triggered by software; the length of the transmission and the source and destination addresses of the transmission can be set individually by software.

DMA can be used for the main peripherals: SPI, I2C, USART, as well as the general purpose, basic and advanced control timers TIMx and ADC.

2.1.14 RTC (Real Time Clock) and Backup Registers

The RTC and Backup Registers are powered by a switch that selects V_{DD} when V_{DD} is active, otherwise they are powered by the V_{BAT} pin. The back-up registers (10 16-bit registers) can be used to hold 20 bytes of user application data when V_{DD} is turned off.The RTC and back-up registers are not reset by the system or power reset source; nor are they reset when woken up from standby mode.

The real time clock has a set of continuously running counters, a calendar clock function that can be provided by appropriate software, and an alarm interrupt and phase interrupt function.The RTC's drive clock can be a 32.768kHz oscillator using an external crystal, an internal low-power RC oscillator, or a high-speed external clock divided by 128.The internal low-power RC oscillator has a typical frequency of 40kHz.To compensate for deviations from the natural crystal, the RTC can be calibrated by outputting a 512Hz signal. The internal low-power RC oscillator has a typical frequency of 40kHz, and the RTC's clock can be calibrated by outputting a 512Hz signal to compensate for deviations in the natural crystal.

for long time measurements. There is a 20-bit prescaler for the time base clock, which by default generates a 1-second long time reference when the clock is 32.768kHz.

2.1.15 Timers and Watchdogs

The CKS32F103x8 and CKS32F103xB standard series include 1 advanced control timer, 3 general timers, and 2

The watchdog timer and 1 system timer.

The following table compares the functions of the Advanced Control Timer, Normal Timer, and Basic Timer:

Table 1 Comparison of Timer Functions

timers	Counter Resolution	Counter Type	presharing factor	Generate DMA please look for	Capture/Compare Channel	complementary output
TIM1	16-bit	Incremental count/ count down	Between 1 and 65536 any integer of	possible	4	there are
TIM2 TIM3 TIM4	16-bit	Incremental counting /decremental counting	Any integer between 1 and 65536	can	4	hasn't

Advanced Control Timer (TIM1)

The advanced control timer (TIM1) can be thought of as a three-phase PWM generator assigned to six channels with complementary deadband insertion.

The PWM output can also be used as a complete general-purpose timer. 4 independent channels are available:

- Input Capture
- Output Comparison
- Generate PWM (edge or center alignment mode)
- Single pulse output

When configured as a 16-bit standard timer, it has the same function as TIMx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%).

In debug mode, the counter can be frozen while the PWM outputs are disabled, thus cutting off the switches controlled by these outputs.

Many of the functions are the same as the standard TIM timer and the internal structure is the same, so the Advanced Control Timer can operate in concert with the TIM timer through the Timer Link function to provide synchronization or event linking functions.

Universal Timer (TIMx)

Up to three standard timers (TIM2, TIM3, and TIM4) that can run synchronously are built into the CKS32F103x8 and CKS32F103xB standard models. Each timer has a 16-bit auto-loading increment/decrement counter, a 16-bit prescaler, and four independent channels, each of which can be used for input capture, output compare, PWM, and single-pulse mode outputs,

providing up to twelve input capture, output compare, or PWM channels in the largest package configuration.

They can also work with advanced control timers through the timer linking feature, providing synchronization or event linking. The counters can be frozen in debug mode. Any of the standard timers can be used to generate PWM outputs. Each timer has an independent DMA request mechanism.

These timers are also capable of handling signals from incremental encoders, as well as digital outputs from 1 to 3 Hall sensors.

Independent Watchdog

The Standalone Watchdog is based on a 12-bit decrement counter and an 8-bit prescaler, which is clocked by an internal independent 40kHz RC oscillator; since this RC oscillator is independent of the main clock, it can operate in shutdown and standby modes. It can be used as a watchdog to reset the entire system in the event of a problem, or as a free timer to provide timeout management for applications. The option byte can be configured to be a software or hardware initiated watchdog. In debug mode the counter can be frozen.

Windows Watchdog

The window watchdog contains a 7-bit decrement counter that can be configured to run freely. When used as a watchdog, it can reset the entire system in the event of a problem. It is driven by the master clock and has an early warning interrupt; the counter can be frozen in debug mode.

system time base timer

This timer can be used exclusively for real-time operating systems or as a standard decrementing counter. It has the following characteristics:

- 24-bit Decrement Counter
- Auto Reload Function
- Generates a maskable system interrupt when the counter is 0.
- Programmable Clock Source

2.1.16 I2C bus

Up to 2 I² C bus interfaces, capable of operating in multi-master or slave mode, supporting standard and fast modes.
The I2C interface supports 7-bit or 10-bit addressing, and the 7-bit slave mode supports dual slave address addressing. A hardware CRC generator/checker is built-in. The interface can be operated using DMA and supports SMBus bus version 2.0/PMBus bus.

2.1.17 Universal Synchronous/Asynchronous Transceiver (USART)

The USART1 interface communicates at rates up to 4.5 Mb/s, while the other interfaces communicate at rates up to Mb/s. The USART interface has hardware CTS and
RTS signal management, support for IrDA SIR ENDEC transmission codecs, ISO7816-compatible smart cards and LIN master/slave functionality. All USART interfaces can be operated using DMA.

2.1.18 Serial Peripheral Interface (SPI)

Up to 2 SPI interfaces, configurable in slave or master mode, with full- and half-duplex communication rates up to 18 Mb/s. 3-bit prescaler generates 8 master mode frequencies, configurable in 8- or 16-bit data frame format. Hardware CRC generation/checksum support for basic SD card and MMC modes.

DMA operation is available for all SPI interfaces.

2.1.19 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active) at bit rates up to 1 Mb/s. It can receive and send standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has 3 transmit mailboxes and 2 receive FIFOs with 3 stages and 14 adjustable filters.

2.1.20 Universal Serial Bus (USB)

The CKS32F103x8 and CKS32F103xB standard series embed a full-speed USB-compatible device controller that follows the full-speed USB device (12 Mb/s) standard, with software-configurable endpoints and standby/wakeup functionality.The USB-specific 48 MHz clock is generated directly from the internal master PLL (clock source must be an HSE crystal oscillator). The 48MHz clock dedicated to USB is generated directly from the internal master PLL (clock source must be an HSE crystal oscillator).

2.1.21 General Purpose Input Output Interface (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), an input (pull-up or pull-down or float), or a multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. In addition to having analog input capabilities, all GPIO pins allow high currents to pass.

Where required, the peripheral functions of the I/O pins can be locked by a specific operation to avoid accidental write operations to the I/O registers. The I/O pins on the APB2 can be flipped at speeds up to 18MHz.

2.1.22 ADC (analog/digital converter)

The CKS32F103x8 and CKS32F103xB standard models incorporate two 12-bit analog/digital converters (ADCs), each of which shares up to 16 external channels, and can perform either single conversion or scan mode conversion. In scan mode, conversion can be performed automatically on a selected set of analog input pins.

Other logic functions on the ADC interface include:

- Synchronized sample and hold
- Cross sampling and hold
- Single Sampling

The ADC can be operated using DMA.

The analog watchdog is able to monitor one, multiple or all selected channels with great precision, and generates an interrupt when the monitored signal exceeds a preset threshold.

Events generated by the standard timer (TIMx) and the advanced control timer (TIM1) can

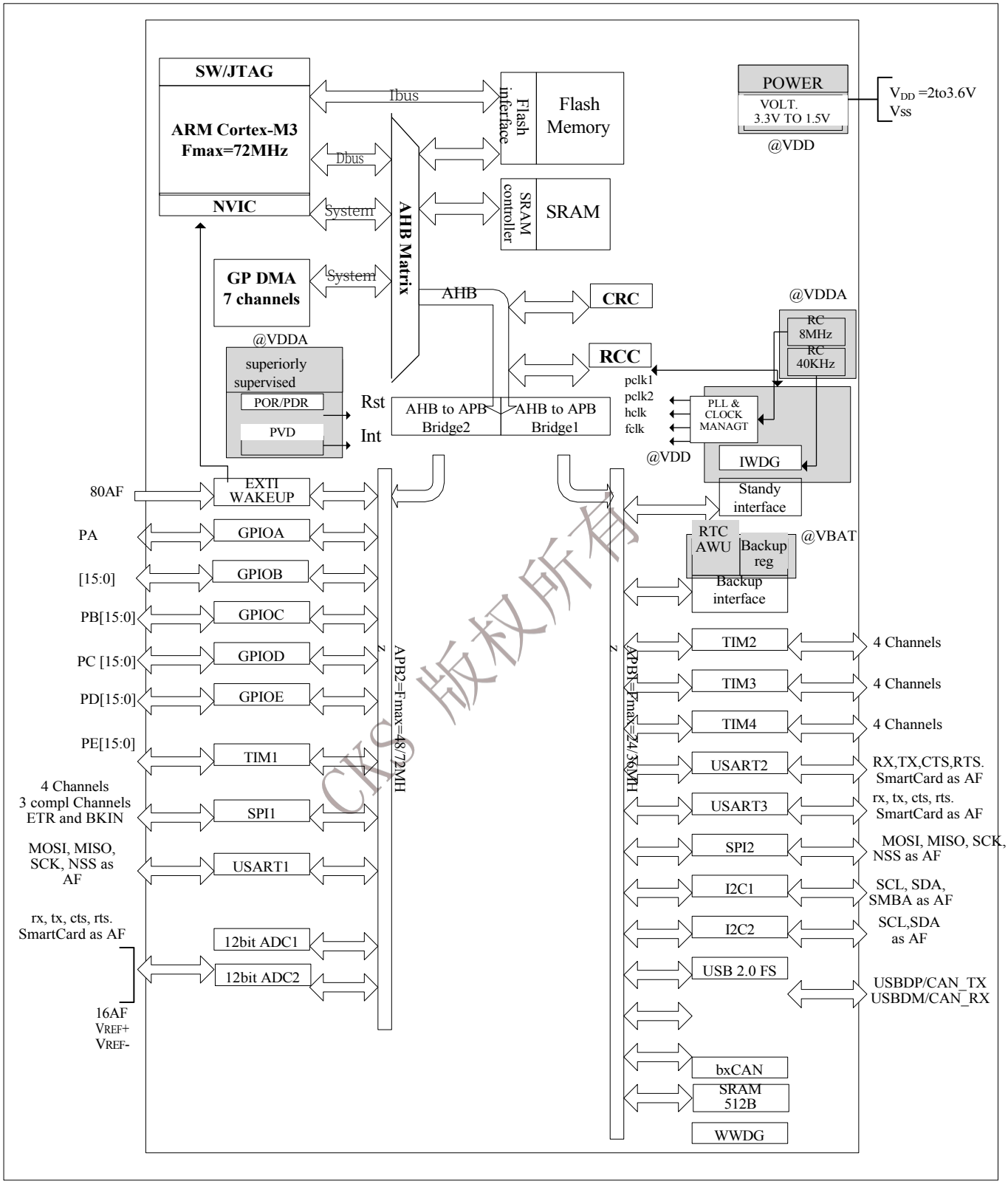
be internally cascaded to the ADC's Start Trigger and Injection Trigger, respectively, and the application program can synchronize the AD conversion with the clock.

2.1.23 temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature over a conversion range of 2V < VDDA< 3.6V. The temperature sensor is internally connected to the input channel of ADC12_IN16, which is used to convert the sensor output to a digital value.

2.1.24 Serial Single Wire JTAG Debug Port (SWJ-DP)

Embedded ARM's SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging interface that enables the connection of either the serial single-wire debugging interface or the JTAG interface. the TMS and TCK signals of the JTAG share the same pins as the SWDIO and SWCLK, respectively, and a special sequence of signals on the TMS pin is used to toggle between the JTAG-DP and the SW-DP.



peripheral function pin

1. Operating temperature: -40℃ to +105℃, junction temperature up to 125℃ .
2. AF: I/O port that can be used as a

Fig. 1 Block diagram of system modules

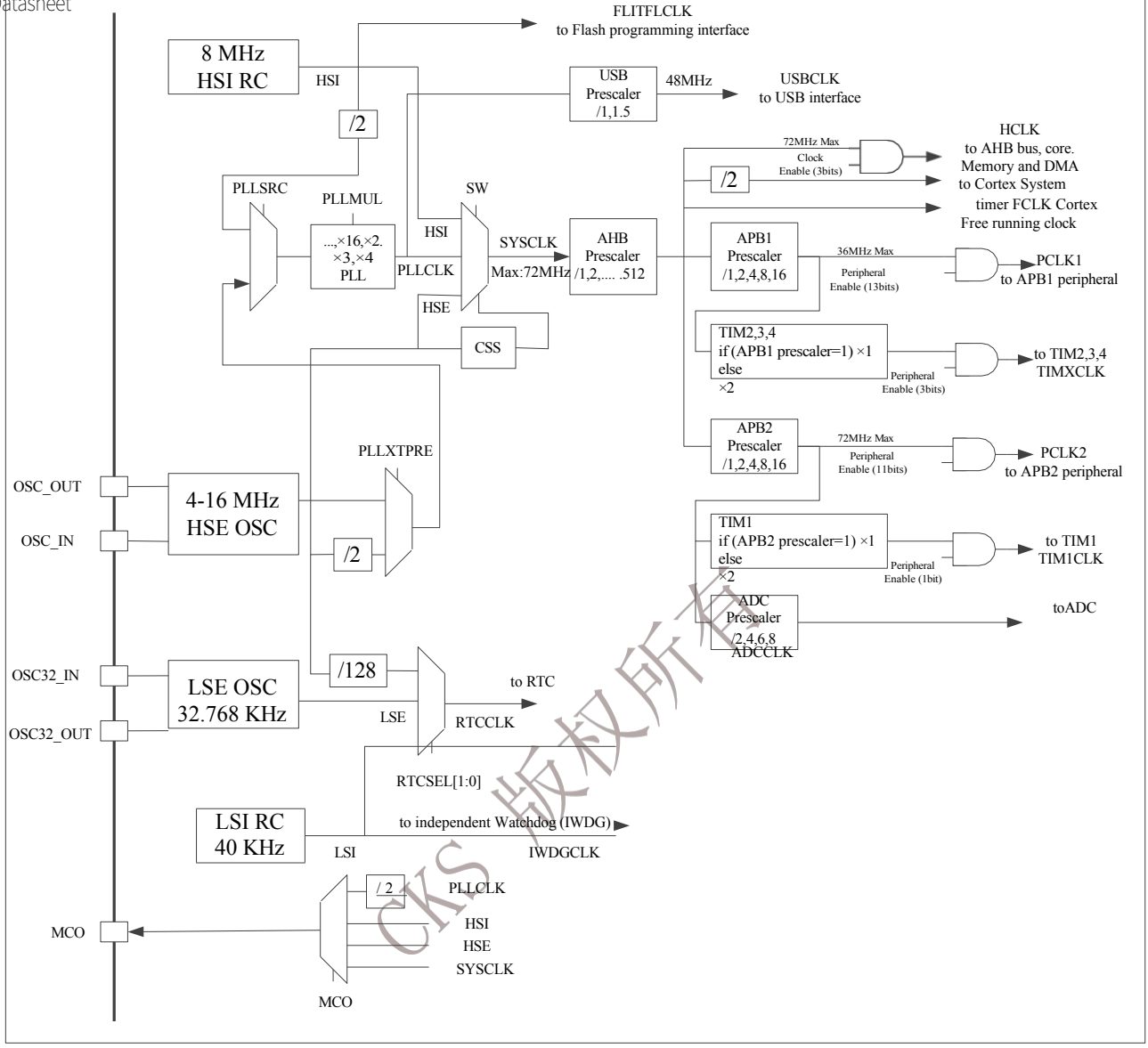


Figure 2 Clock tree

1. When the HSI is used as an input to the PLL clock, the maximum system clock frequency can only be 64MHz.
2. When using the USB function, both HSE and PLL must be used and the CPU frequency must be 48MHz or 72MHz.
3. When an ADC sampling time of 1μs is required, APB2 must be set at 14MHz, 28MHz, or 56MHz.

3. Pin Definitions

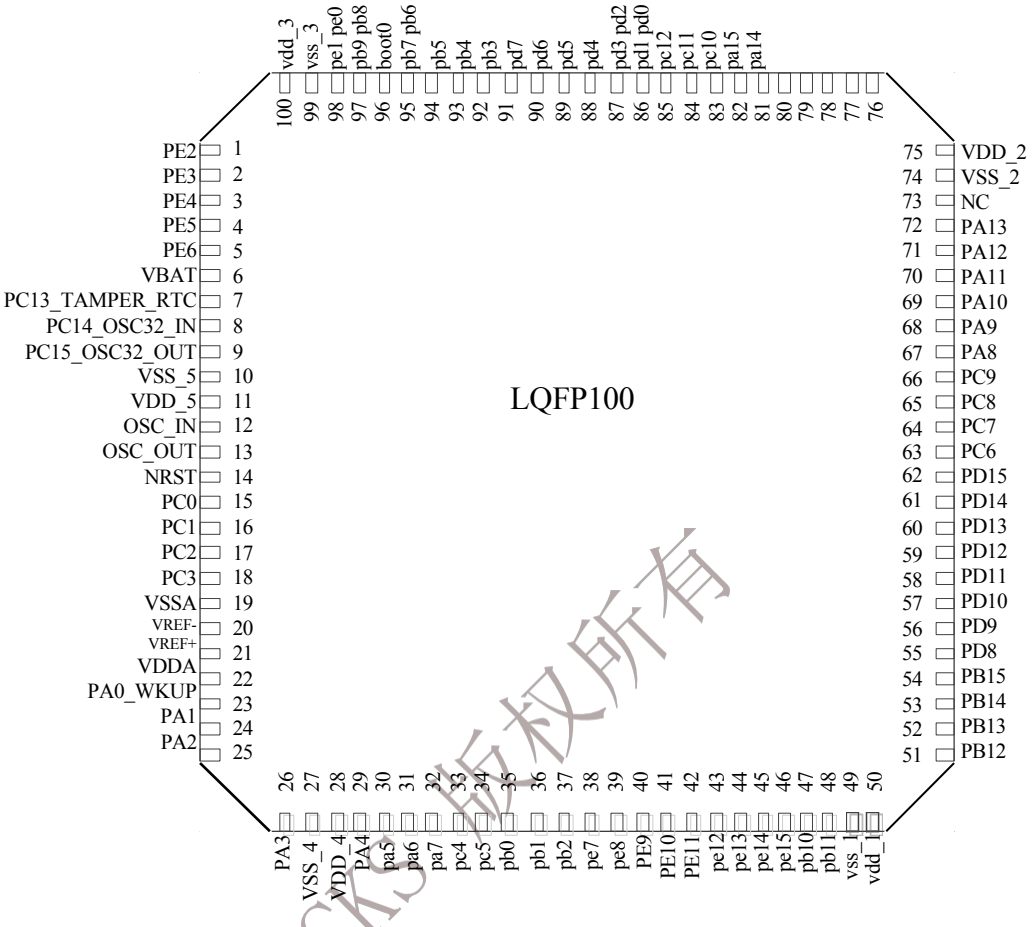


Figure 3CKS32F103xx Standard LQFP100 Pinouts

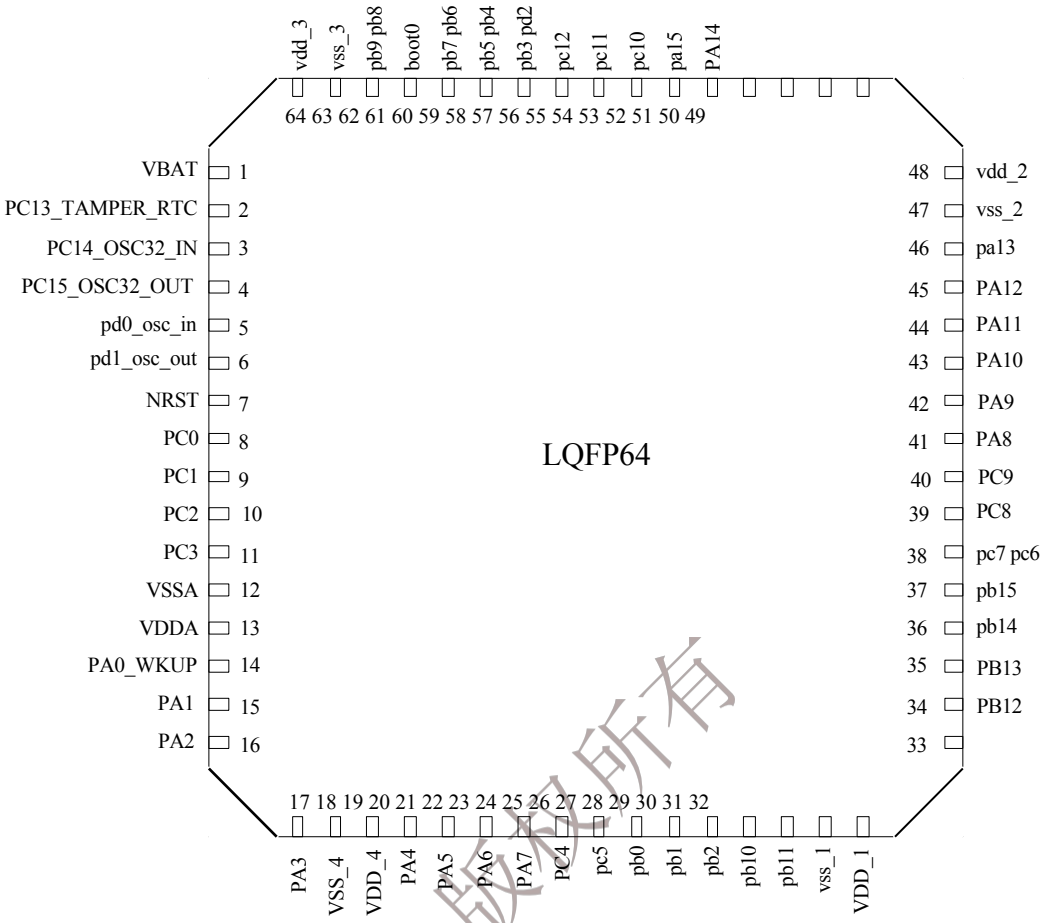


Figure 4CKS32F103xx Standard LQFP64 Pinout

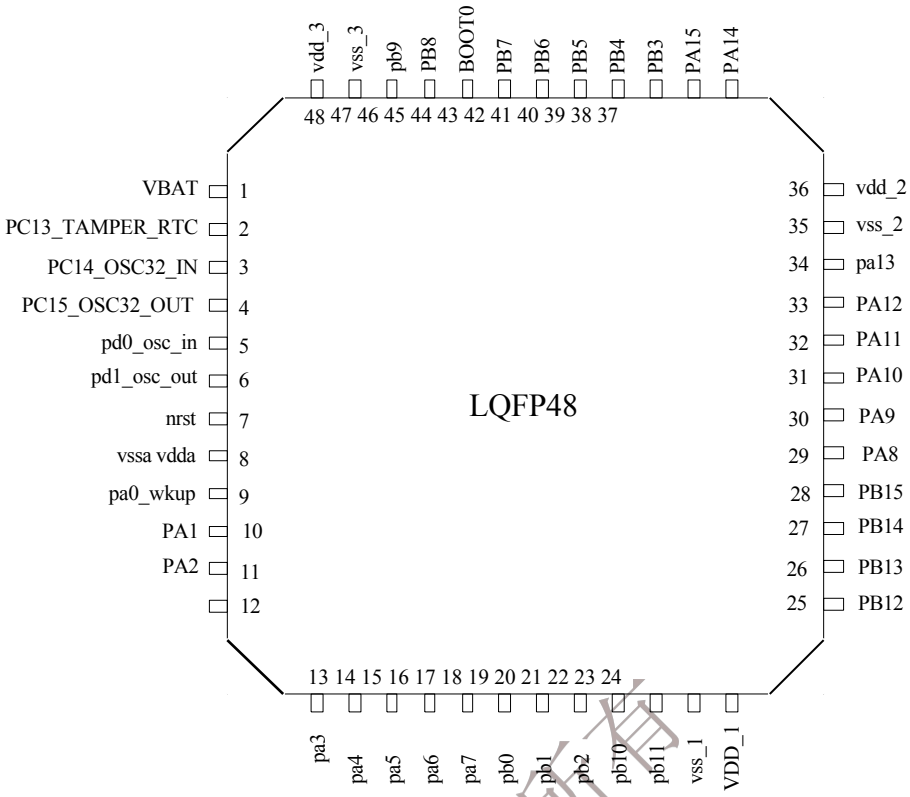


Figure 5CKS32F103xx Standard LQFP48 Pinouts

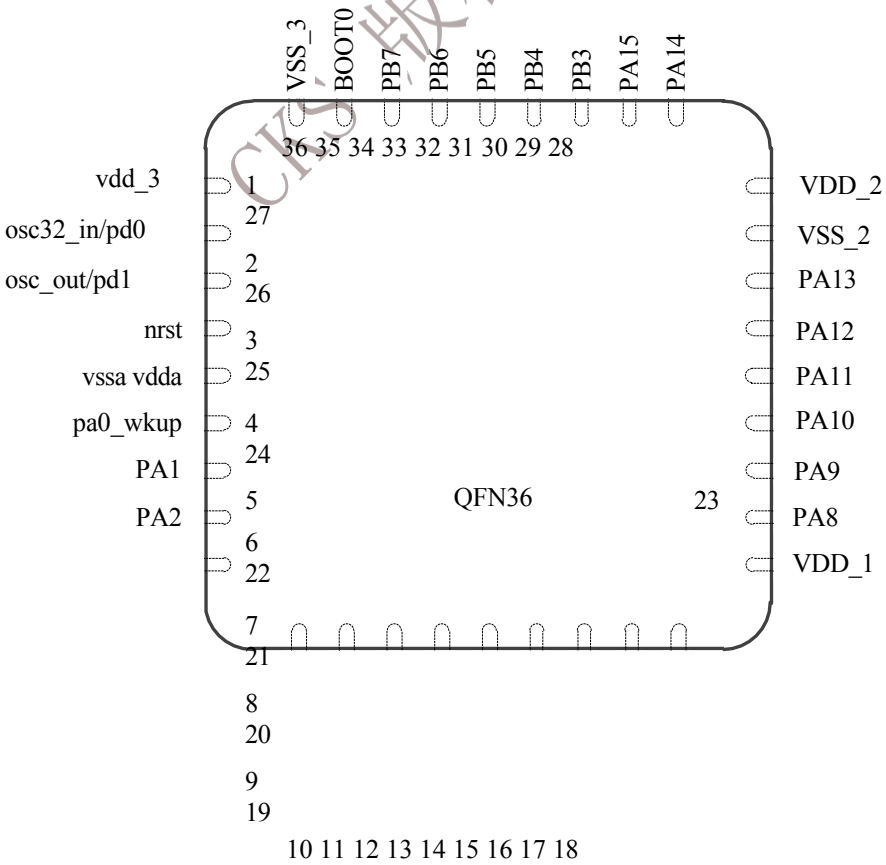


Figure 6CKS32F103xx Standard QFN36 Pinouts

Table 2CKS32F103xx Pin Definitions

Pin Number				Pin Name	type(1)	I/O power level (elec.)	Main Functions(3) (after reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
-	-	1	-	PE2	I/O	FT	PE2	TRACECK	
-	-	2	-	PE3	I/O	FT	PE3	TRACED0	
-	-	3	-	PE4	I/O	FT	PE4	TRACED1	
-	-	4	-	PE5	I/O	FT	PE5	TRACED2	
-	-	5	-	PE6	I/O	FT	PE6	TRACED3	
1	1	6	-	VBAT	S		VBAT		
2	2	7	-	PC13-TAMPER-RTC(4)	I/O		PC13	TAMPER-RTC	
3	3	8	-	PC14-OSC32_IN(4)	I/O		PC14	OSC32_IN	
4	4	9	-	PC15-OSC32_OUT(4)	I/O		PC15	OSC32_OUT	
-	-	10	-	VSS_5	S		VSS_5		
-	-	11	-	VDD_5	S		VDD_5		
5	5	12	2	OSC_IN	I		OCS_IN		PD0(7)
6	6	13	3	OSC_OUT	o		OSC_OUT		PD1(7)
7	7	14	4	NRST	I/O		NRST		
-	8	15	-	PC0	I/O		PC0	ADC12_IN10	
-	9	16	-	PC1	I/O		PC1	ADC12_IN11	
-	10	17	-	PC2	I/O		PC2	ADC12_IN12	
-	11	18	-	PC3	I/O		PC3	ADC12_IN13	
8	12	19	5	VSSA	S		VSSA		
-	-	20	-	VREF-	S		VREF-		
-	-	21	-	VREF+	S		VREF+		
9	13	22	6	VDDA	S		VDDA		
10	14	23	7	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS(6) /ADC12_IN0/ TIM2_CH1_ETR(6)	
11	15	24	8	PA1	I/O		PA1	USART2_RTS(6) / ADC12_IN1/ TIM2_CH2(6)	
12	16	25	9	PA2	I/O		PA2	USART2_TX(6) /ADc12_in2/tim2_ch 3(6)	
13	17	26	10	PA3	I/O		PA3	USART2_RX(6) /ADC12_IN3/TIM2_CH	

Pin Number				Pin Name	type(1)	I/O power level (elec.)	Main Functions(3) (after reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
								4(6)	
-	18	27	-	VSS_4	S		VSS_4		
-	19	28	-	VDD_4	S		VDD_4		
14	20	29	11	PA4	I/O		PA4	spi1_nss(6) / usart2_ck /(6) ADC12_IN4	
15	21	30	12	PA5	I/O		PA5	SPI1_SCK /(6) ADC12_IN5	
16	22	31	13	PA6	I/O		PA6	SPI1_MISO(6) / ADC12_IN6/ TIM3_CH1(6)	TIM1_BKIN
17	23	32	14	PA7	I/O		PA7	SPI1_MOSI(6) / ADC12_IN7/ TIM3_CH2(6)	TIMI_CHIN
-	24	33	-	PC4	I/O		PC4	ADC12_IN14	
-	25	34	-	PC5	I/O		PC5	ADC12_IN15	
18	26	35	15	PB0	I/O		PB0	ADC12_IN8/ TIM3_CH3(6)	TIM1_CH2N
19	27	36	16	PB1	I/O		PB1	ADC12_IN9/ TIM3_CH4(6)	TIM1_CH3N
20	28	37	17	PB2	I/O	FT	PB2/ BOOT1		
-	-	38	-	PE7	I/O	FT	PE7		TIM1_ETR
-	-	39	-	PE8	I/O	FT	PE8		TIM1_CH1N
-	-	40	-	PE9	I/O	FT	PE9		TIM1_CH1
-	-	41	-	PE10	I/O	FT	PE10		TIM1_CH2N
-	-	42	-	PE11	I/O	FT	PE11		TIM1_CH2
-	-	43	-	PE12	I/O	FT	PE12		TIM1_CH3N
-	-	44	-	PE13	I/O	FT	PE13		TIM1_CH3
-	-	45	-	PE14	I/O	FT	PE14		TIM1_CH4
-	-	46	-	PE15	I/O	FT	PE15		TIM1_BKIN
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(6)	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(6)	TIM2_CH4

23	31	49	18	VSS_1	S		VSS_1		
24	32	50	19	VDD_1	S		VDD_1		

Pin Number				Pin Name	type(1)	I/O power level (elec.)	Main Functions(3) (after reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
25	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK /(6) TIM1_BKIN(6)	
26	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(6) / TIM1_CH1N(6)	
27	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_CTS(6) / TIM1_CH2N(6)	
28	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(6)	
-	-	55	-	PD8	I/O	FT	PD8		USART3_TX
-	-	56	-	PD9	I/O	FT	PD9		USART3_RX
-	-	57	-	PD10	I/O	FT	PD10		USART3_CK
-	-	58	-	PD11	I/O	FT	PD11		USART3_CTS
-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1/ USART3_RTS
-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2
-	-	61	-	PD14	I/O	FT	PD14		TIM4_CH3
-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4
-	37	63	-	PC6	I/O	FT	PC6		TIM3_CH1
-	38	64	-	PC7	I/O	FT	PC7		TIM3_CH2
-	39	65	-	PC8	I/O	FT	PC8		TIM3_CH3
-	40	66	-	PC9	I/O	FT	PC9		TIM3_CH4
29	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(6) /MCO	
30	42	68	21	PA9	I/O	FT	PA9	USART1_TX /(6) TIM1_CH2(6)	
31	43	69	22	PA10	I/O	FT	PA10	USART1_RX /(6) TIM1_CH3(6)	
32	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ USBDM/CANRX(6) /TIM1_CH4(6)	

33	45	71	24	PA12	I/O	FT	PA12	usart1_rts/ usbdp/cantx /(6) TIM1_ETR(6)	

Pin Number				Pin Name	type(1)	I/O power level (elec.)	Main Functions(3) (after reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
34	46	72	25	PA13	I/O	FT	JTMS/SWDIO		PA13
-	-	73	-	unconnected					
35	47	74	26	VSS_2	S		VSS_2		
36	48	75	27	VDD_2	S		VDD_2		
37	49	76	28	PA14	I/O	FT	JTCK/SWCLK		PA14
38	50	77	29	PA15	I/O	FT	JTDI		TIM2_CH1_ETR PA15/SPI1_NSS
-	51	78	-	PC10	I/O	FT	PC10		USART3_TX
-	52	79	-	PC11	I/O	FT	PC11		USART3_RX
-	53	80	-	PC12	I/O	FT	PC12		USART3_CK
		81	2	PD0	I/O	FT	OSC_IN(8)		CANRX
		82	3	PD1	I/O	FT	OSC_OUT(8)		CANTX
-	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	
-	-	84	-	PD3	I/O	FT	PD3		USART2_CTS
-	-	85	-	PD4	I/O	FT	PD4		USART2_RTS
-	-	86	-	PD5	I/O	FT	PD5		USART2_TX
-	-	87	-	PD6	I/O	FT	PD6		USART2_RX
-	-	88	-	PD7	I/O	FT	PD7		USART2_CK
39	55	89	30	PB3	I/O	FT	JTDO		pb3/traceswo/ tim2_ch2/ SPI1_SCK
40	56	90	31	PB4	I/O	FT	JNTRST		PB4/TIM3_CH1/ SPI1_MISO
41	57	91	32	PB5	I/O		PB5	I2C1_SMBAI	TIM3_CH2/ SPI1_MOSI
42	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL /(6) TIM4_CH1(6)	USART1_TX
43	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA /(6) TIM4_CH2(6)	USART1_RX
44	60	94	35	BOOT0	I		BOOT0		
45	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3(6)	I2C1_SCL/ CANRX

46	62	96	-	P89	I/O	FT	P89	TIM4_CH4(6)	I2C1_SDA/ CANTX

Pin Number				Pin Name	typology (1)	I/O power level (2)	Main Functions(3) (after reset)	Optional multiplexing function	
LQFP48	LQFP64	LQFP100	QFN36						
-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR	
-	-	98	-	PE1	I/O	FT	PE1		
47	63	99	36	VSS_3	S		VSS_3		
48	64	100	1	VDD_3	S		VDD_3		

1. I = Input, O = Output, S = Supply
2. FT: 5V Voltage Tolerance
3. The PC13, PC14 and PC15 pins are powered by a power switch that can only absorb a limited amount of current (3mA). Therefore, these three pins have the following limitations when used as output pins: when used as output pins, they can only be operated in 2MHz mode, the maximum drive load is 30pF, and they cannot be used as a current source (e.g., to drive LEDs).
4. These pins are in the primary functional state when the backup area is first powered up, after that, even if reset, the state of these pins is controlled by the backup area registers (these registers are not reset by the primary reset system) For specific information on how to control these IO ports, refer to the relevant sections of the CKS32F103x8 and CKS32F103xB Reference Manuals for the Battery Backup Area and BKP registers.
5. This type of multiplexing can be configured by software to other pins (if available for the corresponding package model), for details please refer to CKS32F103x8 and
   The Multiplexing Functions I/O chapter and the Debug Setup chapter of the CKS32F103xB Reference Manual.
6. Pins 2 and 3 for the QFN36 package, and pins 5 and 6 for the LQFP48 and LQFP64 packages are configured as OSC_IN and OSC_OUT function pins by default after a chip reset. Software can reset these pins to function as PD0 and PD1. However, for LQFP100 package, since PD0 and PD1 are intrinsic functional pins, there is no need to reimage them by software. For more details, please refer to the Multiplexed Function I/O section and Debug Setup section of the CKS32F103x8 and CKS32F103xB Reference Manuals. In output mode, PD0 and PD1 can only be configured for 50MHz output mode.
7. ADC12_INx (x represents an integer between 0 and 15), which appears in the pin name labeling in the table, indicates that this pin can be ADC1_INx or ADC2_INx. e.g. ADC12_IN9 indicates that this pin can be configured as ADC1_IN9 or ADC2_IN9.
8. TIM2_CH1_ETR in the multiplexing function corresponding to pin PA0 in the table indicates that the function can be configured as TIM2_TI1 or TIM2_ETR. Similarly, PA15
   The name of the corresponding remapping multiplexing function, TIM2_CH1_ETR, has the same meaning.

4. memory image

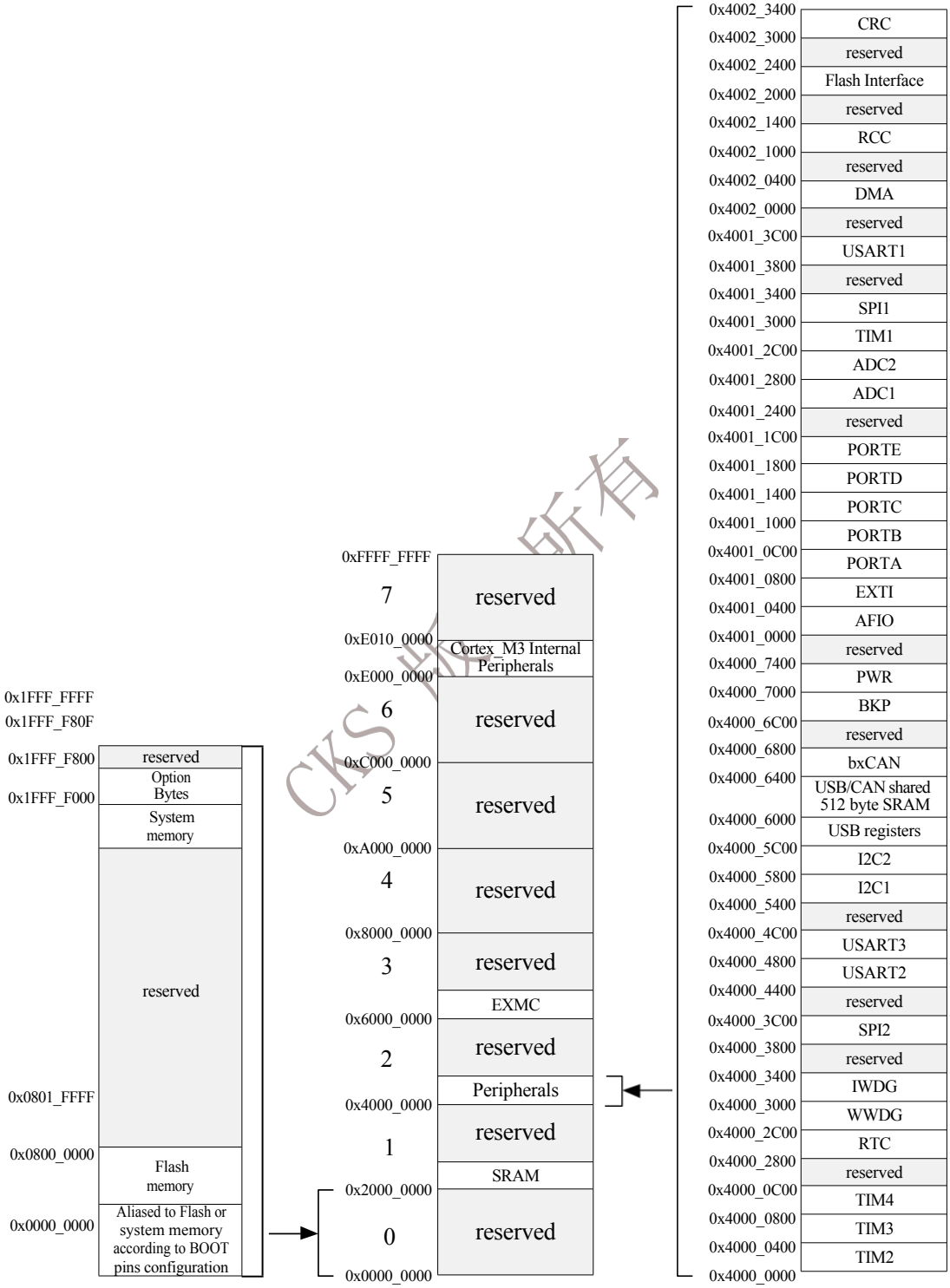


Figure 7 Memory MAP Diagram

5. Electrical Characteristics

5.1 test condition

All voltage's are referenced to V_{SS} unless otherwise noted.

5.1.1 Minimum and maximum values

Unless otherwise stated, all minimum and maximum values are guaranteed at the worst case ambient temperature, supply voltage and clock frequency conditions by testing 100% of the product on the production line at an ambient temperature of TA=25°C and T_A =TAmax (TAmax matches the selected temperature range).

In the notes below each table, it is stated that the data obtained through comprehensive evaluation, design simulation and/or process characterization will not be tested on the production line; on the basis of the comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested plus or minus three times the standard distribution (mean ± 3∑).

5.1.2 Typical values

Typical data is based on TA=25°C and V_{DD} =3.3V (2V ≤ V_{DD} ≤ 3.3V voltage range) unless otherwise noted. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are obtained by sampling a standardized batch, tested over all temperature ranges, with 95% of the products having an error less than or equal to the value given (±2∑ on average).

5.1.3 typical curve

Typical curves are for design guidance only and are untested unless otherwise noted.

5.1.4 load capacitance

The load conditions for measuring the pin parameters are shown in Figure 8.

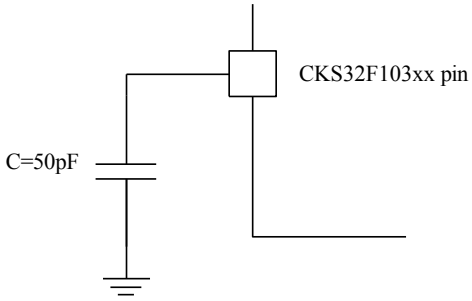


Figure 8 Load Conditions for Pins

5.1.5 Pin Input Voltage

The measurement of the input voltage on the pins is shown in Figure 9.

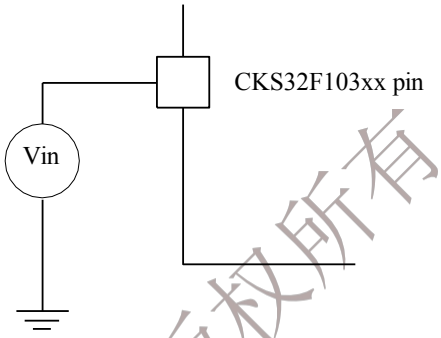


Figure 9 Pin Input Voltage

5.1.6 Power supply program

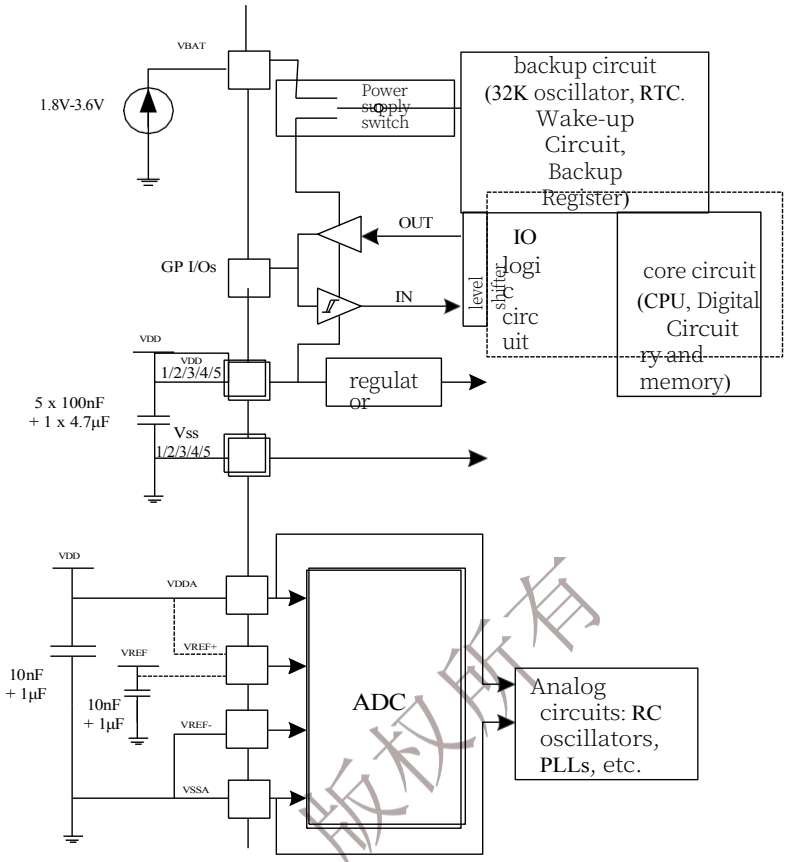


Figure 10 Power supply scheme

Note: The *4.7µF* capacitor in the above diagram must be connected to *VDD3*.

5.1.7 Current consumption measurement

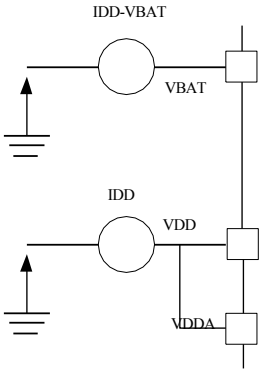


Figure 11 Current consumption measurement scheme

5.2 Absolute maximum rating

Loads applied to the device in excess of the values given in the Absolute Maximum Ratings lists (Tables 3, 4, 5) may cause permanent damage to the device. The fact that only the maximum loads that can be withstood are given does not imply that the device operates functionally without error under these conditions. Prolonged operation of the device at the maximum value will affect the reliability of the device.

Table 3 Voltage Characteristics

notation	descriptive	minimum value	maximum values	unit (of measure)
V_{DD} - V_{SS}	External mains supply voltage (including V_{DDA} and V_{DD}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on pins with 5V tolerance(2)	V_{SS} -0.3	V_{DD} +4.0	
	Input voltage on other pins(2)	V_{SS} -0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Voltage difference between different supply pins		50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Voltage difference between different ground pins		50	
VESD (HBM)	ESD Electrostatic discharge voltage (human body model)	See Section 5.3.11.		

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external permissible range power supply system.
2. $I_{INJ(PIN)}$ must never exceed its maximum value. If it is not possible to ensure that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. When $V_{IN}>V_{INmax}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.

Table 4 Current Characteristics

notation	descriptive	maximum values	unit (of measure)
IVDD	Total current (supply current) through the $V_{DD/VDDA}$ power supply line (1)	150	mA
IVSS	Total current (outgoing current) through the V_{SS} ground (1)	150	
I_{IO}	Output sink current on any I/O and control pins	25	
	Output current on arbitrary I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)(3)	5V Tolerance Pin Injection Current	-5/+0	
	Injection current on other pins(4)	±5	
$\sum I_{INJ(PIN)}$ (2)	Total injected current on all I/O and control pins(4)	±25	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external permissible range power supply system.
2. $I_{INJ(PIN)}$ must never exceed its maximum value. If it is not possible to ensure that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the $I_{INJ(PIN)}$ is externally limited to not exceed its maximum value. When $V_{IN}>V_{DD}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.
3. Reverse current injection can interfere with the analog performance of the device. See Section 5.3.17.
4. When several I/O ports have injected currents at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. This result is based on the characterization of the maximum value of $\sum I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 5 Temperature Characteristics

notation	descriptive	numerical value	unit (of measure)
TSTG	Storage temperature range	-65~+150	℃
TJ	Maximum Junction Temperature	150	℃

5.3 working conditions

5.3.1 General working conditions

Table 6 General working conditions

notation	parameters	prerequisite		minimum value	maximum values	unit (of measure)
fHCLK	Internal AHB clock frequency			0	72	MHz
fPCLK1	Internal APB1 clock frequency			0	36	
fPCLK2	Internal APB2 clock frequency			0	72	
VDD	Standard Operating Voltage			2	3.6	V
V_{DDA} (1)	Analog section operating voltage (without ADC)	must be the same as V_{DD} (2) is the same as		2	3.6	
	Analog section operating voltage (using ADC)			2.4	3.6	
VBAT	Backup section operating voltage			1.8	3.6	
VIN	I/O Input Voltage	Standard I/O		-0.3	VDD+0.3	
		FT I/O	2V<VDD<3.6V	-0.3	5.5	
			VDD=2V	-0.3	5.2	
		BOOT0		0	5.5	
PD	power dissipation Temperature scale 6: T = 85°C Temperature scale 7: T = 105°C	LQFP100			434	mW
		LQFP64			444	
		LQFP48			363	
		QFN36			1000	
TA	Ambient temperature (temperature scale 6)	Maximum power dissipation		-40	85	°C
		Low power dissipation(4)		-40	105	
	Ambient temperature (temperature scale 7)	Maximum power dissipation		-40	105	
		Low power dissipation(4)		-40	125	
TJ	Junction temperature range	Temperature scale 6		-40	105	
		Temperature scale 7		-40	125	

1. When using an ADC, see Table 43.
2. It is recommended that the same power supply be used to power both VDD and VDDA, allowing up to 300mV difference between VDD and VDDA during power-up and normal operation.
3. If the TA is lower, higher PD values are allowed as long as the TJ does not exceed TJmax (see section 1).
4. In states with lower power dissipation, TA can be extended to this range as long as TJ does not exceed TJmax (see Section 1).

5.3.2 Operating conditions at power-up and power-down

The parameters given in the following table were tested under general operating conditions.

Table 7 Operating conditions at power-up and power-down

notation	parameters	conditional	minimum value	maximum values	unit (of measure)
tVDD	V_{DD} Rise Rate		0	∞	μs/V
	V_{DD} Rate of Descent		20	∞	

5.3.3 Embedded reset and power control module features

The parameters given in the following table are based on tests at ambient temperature and V_{DD} supply voltage as listed in Table 6.

Table 8 Embedded Reset and Power Control Module Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
VPVD	Programmable Voltage Detector level selection	PLS[2:0]=000 (rising edge)	2.10	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2.00	2.07	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.17	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.27	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.47	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.37	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.57	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.46	2.59	V
		PLS[2:0]= 101 (rising edge)	2.57	2.67	2.79	V
		PLS[2:0]= 101 (falling edge)	2.47	2.56	2.69	V
		PLS[2:0]= 110 (rising edge)	2.66	2.77	2.90	V
		PLS[2:0]=110 (falling edge)	2.56	2.66	2.80	V
		PLS[2:0]=111 (rising edge)	2.76	2.86	3.00	V
		PLS[2:0]=111 (falling edge)	2.66	2.76	2.90	V
$V_{PVDhyst}$ (2)	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power up/down reset threshold	Falling edge (of a mountain range)	1.80	1.87	1.96	V
		Rising edge (of a mountain range)	1.84	1.92	2.0	V
$V_{PVDhyst}$ (2)	PDR hysteresis			40		mV
$T_{RSTTEMPO}$ (2)	Reset Duration		1	2.5	4.5	ms

1. The characteristics of the product are guaranteed by design to a minimum value of $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

5.3.4 Built-in reference voltage

The parameters given in the following table are based on tests at ambient temperature and V_{DD} supply voltage as listed in Table 6.

Table 9 Built-in reference voltage

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
VREFINT	Built-in reference voltage	-40°C < TA< +105°C	1.16	1.20	1.26	V
		-40°C < TA< +85°C	1.16	1.20	1.24	V
$T_{S\_vref_{int}}$ (1)	When the internal reference voltage is read ADC Sampling Time			5.1	17.1(2)	μs

1. The characteristics of the product are guaranteed by design to a minimum value of $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

5.3.5 Supply Current Characteristics

Current consumption is a combination of a number of parameters and factors including operating voltage, ambient temperature, load on I/O pins, software configuration of the product, operating frequency, flip-flop rate of I/O pins, location of the program in memory, and code executed.

See Figure 11 for a description of how current consumption is measured.

All of the current consumption measurements given in this section for the operating modes are obtained by executing a streamlined set of codes that are able to Dhrystone2.1 code equivalent results.

Maximum current consumption

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are off unless otherwise noted.
- The flash memory access time is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz, and 2 wait cycles for more than 48MHz).
- Command prefetch is turned on (hint: this parameter must be set before setting the clock and bus divider).
- When the peripheral is turned on: $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$.

The parameters given in Tables 10, 11, and 12 are based on tests at the ambient temperatures and V_{DD} supply voltages listed in Table 5.

Table 10 Maximum Current Consumption in Run Mode with Data Processing Code Running from Internal Flash Memory

notation	parameters	prerequisite	f_{HCLK}	Maximum value (1)		unit (of measure)
				TA= 85°C	TA= 105°C	
			72MHz	50	50.3	

			36MHz	19.8	19.9	
			24MHz	13.9	14.2	
			16MHz	10.7	11	
			8MHz	6.8	7.1	

1. Derived from a comprehensive assessment and not tested in production.
2. External clock is 8MHz, PLL is enabled when fHCLK>8MHz.

Table 11 Maximum Current Consumption in Run Mode with Data Processing Code Running from Internal

notation	parameters	prerequisite	RAM fHCLK	Maximum value (1)		unit (of measure)
				TA= 85°C	TA= 105°C	
IDD	Supply current in operating mode	External clock(2) to enable all peripherals	72MHz	48	50	mA
			48MHz	31.5	32	
			36MHz	24	25.5	
			24MHz	17.5	18	
			16MHz	12.5	13	
			8MHz	7.5	8	
		External clock(2) to turn off all peripherals	72MHz	29	29.5	
			48MHz	20.5	21	
			36MHz	16	16.5	
			24MHz	11.5	12	
			16MHz	8.5	9	
			8MHz	5.5	6	

1. Derived from a comprehensive evaluation and tested in production with VDDmax and fHCLKmax as conditions.
2. External clock is 8MHz, PLL is enabled when fHCLK>8MHz.

Table 12 Maximum current consumption in sleep mode with code running in Flash or RAM

notation	parameters	conditional	fHCLK	Maximum value (1)		unit (of measure)
				TA= 85°C	TA= 105°C	
IDD	Supply current in sleep mode	External clock(2) to enable all peripherals	72MHz	30	32	mA
			48MHz	20	20.5	
			36MHz	15.5	16	
			24MHz	11.5	12	
			16MHz	8.5	9	
			8MHz	5.5	6	
		External clock(2) to turn off all peripherals	72MHz	7.5	8	
			48MHz	6	6.5	
			36MHz	5	5.5	

			24MHz	4.5	5	
			16MHz	4	4.5	
			8MHz	3	4	

1. Derived from a comprehensive evaluation, tested in production with VDDmax and with fHCLKmax enabling the peripheral as a condition.
2. External clock is 8MHz, PLL is enabled when fHCLK>8MHz.

Table 13 Typical and Maximum Current Consumption in Stop and Standby Modes

notation	parameters	prerequisite	typical value		maximum values		unit (of measure)
			VDD/VBAT = 2.4V	VDD/VBAT = 3.3V	TA= 85°C	TA= 105°C	
IDD	Supply current in shutdown mode	Regulator is in run mode, low and high speeds Internal RC oscillator and high-speed oscillator off (no independent watchdog)	22.7	23.4	200	370	μA
		The regulator is in low-power mode with low and high The internal RC oscillator and high-speed oscillator are off (no independent watchdog).	9.1	10.3	180	340	
	Supply current in standby mode	Low-speed internal RC oscillator and independent watchdog in the on state	2.4	2.06	-	-	
		Low-speed internal RC oscillator on state, independent watchdog is in off state	2.3	2.81	-	-	
		Low-speed internal RC oscillator and independent watchdog is off, the low-speed oscillator and RTC stalled	1.5	3.17	4	5	

I_{DD_VBAT}	The backup area of the Supply current	Low-speed oscillator and RTC on	1.1	1.4	1.9(2)	2.2	

1. Typical values are tested at TA=25°C.
2. Derived from a comprehensive assessment and not tested in production.

Typical Current Consumption

The MCU is under the following conditions:

- All I/O pins are in input mode and connected to a static level - V_{DD} or V_{SS} (no load).
- All peripherals are off unless otherwise noted.
- The flash memory access time is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz, and 2 wait cycles for more than 48MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 6.
- Command prefetch is turned on (hint: this parameter must be set before setting the clock and bus divider). When the peripheral is turned on:
  fPCLK1= fHCLK/4, f_{PCLK2} = fHCLK/2, and f_{ADCCLK} = fPCLK2/4.

Table 14 Typical Current Consumption in Run Mode with Data Processing Code Running from Internal Flash

notation	parameters	prerequisite	fHCLK	Typical value(1)		unit (of measure)
				Enable all peripherals(2)	Turn off all peripherals	
IDD	Supply Current in Operating Mode	External clocks (3)	72MHz	32.46	21.7	mA
			48MHz	21.96	14.73	
			24MHz	12.13	8.57	
			8MHz	5.5	4.31	

1. Typical values are tested at TA=25°C, VDD=3.3V.
2. An additional 0.8mA of current consumption is added to the ADC for each analog section. In the application environment, this current is only increased when the ADC is turned on (setting the ADON bit of the ADC_CR2 register).
3. External clock is 8MHz, PLL is enabled when fHCLK>8MHz.

Table 15 Typical Current Consumption in Run Mode with Data Processing Code Running from Internal RAM

notation	parameters	prerequisite	fHCLK	Typical value(1)		unit (of measure)
				Enable all peripherals(2)	Turn off all peripherals	
IDD	Supply Current in Operating Mode	External clocks (3)	72MHz	24.84	14.21	mA
			48MHz	17.17	10.05	
			24MHz	9.38	5.86	
			8MHz	4.07	2.92	

1. Typical values are tested at TA=25°C, VDD=3.3V.
2. An additional 0.8mA of current consumption is added to the ADC for each analog section. In the application environment, this current is only increased when the ADC is turned on (setting the ADON bit of the ADC_CR2 register).
3. External clock is 8MHz, PLL is enabled when fHCLK>8MHz.

Table 16 Typical Current Consumption in Sleep Mode with Data Processing Code Running from Internal Flash or RAM

notation	parameters	prerequisite	fHCLK	Typical value(1)		unit (of measure)
				Enable all peripherals(2)	Turn off all peripherals	
IDD	Supply current in sleep mode	External clocks (3)	72MHz	17.57	17.61	mA

1. Typical values are tested at TA=25°C, VDD=3.3V.
2. An additional 0.8mA of current consumption is added to the ADC for each analog section. In the application environment, this current is only increased when the ADC is turned on (setting the ADON bit of the ADC_CR2

register).

3. External clock is 8MHz, PLL is enabled when fHCLK>8MHz.

Built-in peripheral current consumption

The current consumption of the built-in peripherals is listed in Table 17, and the operating conditions of the MCU are as follows:

- All I/O pins are in input mode and connected to a static level - V_{DD} or V_{SS} (no load).

- All peripherals are off unless otherwise noted.
- The values given are calculated by measuring current consumption
  - Turn off the clock for all peripherals
  - Turn on the clock for only one peripheral
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4.

Table 17 Current consumption of built-in peripherals(1)

built-in peripherals		Typical power consumption at 25℃	unit (of measure)	built-in peripherals		Typical work at 25℃ dilly-dally	unit (of measure)
APB1	TIM2	1.2	mA	APB2	GPIOA	0.47	mA
	TIM3	1.2			GPIOB	0.47	
	TIM4	0.9			GPIOC	0.47	
	SPI2	0.2			GPIOD	0.47	
	USART2	0.35			GPIOE	0.47	
	USART3	0.35			ADC1(2)	1.81	
	I2C1	0.39			ADC2	1.78	
	I2C2	0.39			TIM1	1.6	
	USB	0.65			SPI1	0.43	
	CAN	0.72			USART1	0.85	

1. f_{HCLK} = 72MHz, f_{APB1} = fHCLK/2, f_{APB2} = f_{HCLK}, and the prescaler coefficients for each peripheral are default values.
2. Special conditions for ADC: f_{HCLK} = 56MHz, f_{APB1} = fHCLK/2, f_{APB2} = f_{HCLK}, f_{ADCCLK} = fAPB2/4, and ADON=1 in ADC_CR2 register.

5.3.6 External Clock Source Characteristics

High-speed external user clock generated from an external oscillator source

The characterization parameters given in the following table were measured using a high-speed external clock source with ambient temperature and supply voltage in accordance with the conditions in Table 6.

Table 18 High-Speed External User Clock Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
fHSE_ext	User External Clock Frequency(1)		1	8	25	MHz
VHSEH	OSC_IN Input pin high voltage		2.2		3.3	V
VHSEL	OSC_IN Input pin low level voltage		0		2.2	
tw (HSE) tw (HSE)	OSC_IN High or low time(1)		5			ns
tr(HSE)	OSC_IN Time of rise or fall(1)				20	

DuCy (HSE)	duty cycle		45	50	55	%
IL	OSC_IN Input leakage current	VSS≤VIN≤VDD		0.3	±1	μA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external oscillator source

The characterization parameters given in the following table were measured using a low-speed external clock source with ambient temperature and supply voltage in accordance with the conditions in Table 6.

Table 19 Low-speed external user clock characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
fLSE_ext	User External Clock Frequency(1)		0	32.768	4000	KHz
VLSEH	OSC32_IN Input pin high voltage		1.8		3.3	V
VLSEL	OSC32_IN Input Pin Low Voltage		0		1.7	
tw (LSE) tw (LSE)	OSC32_IN High or low time(1)		450			ns
tr(LSE) tf(LSE)	OSC32_IN Rise or fall time(1)				50	
Cin (LSE)	OSC32_IN Input Tolerance(1)			5		pF
DuCy (LSE)	duty cycle		30	50	70	%
IL	OSC32_IN Input leakage current	VSS≤VIN≤VDD		-0.4	±1	μA

1. Guaranteed by design, not tested in production.

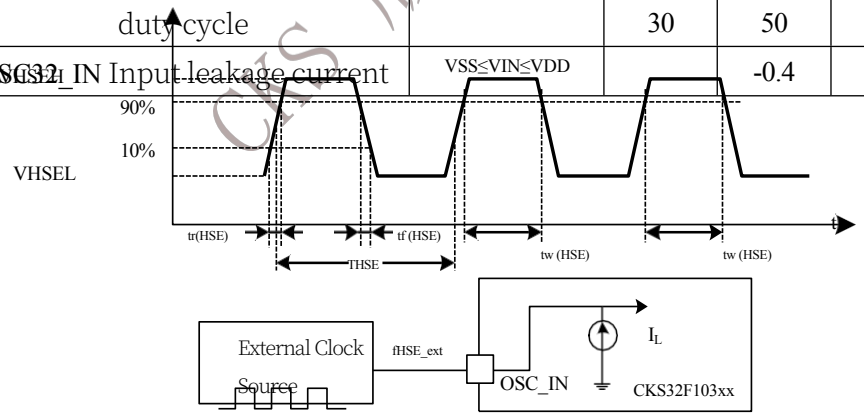


Fig. 12 AC Timing Diagram of External High-Speed Clock Source

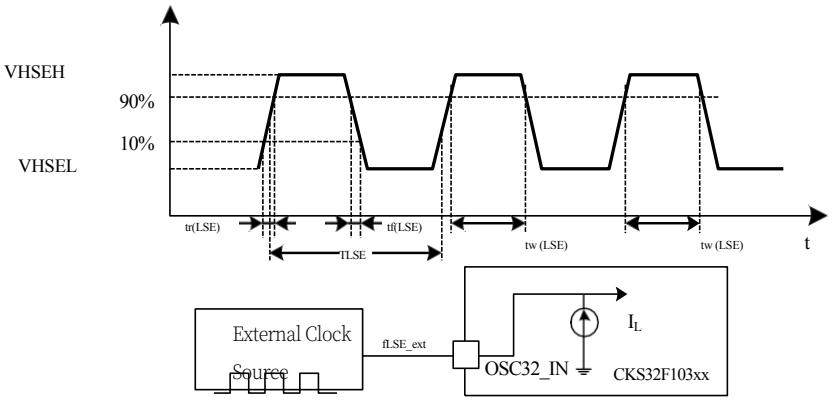


Figure 13 AC Timing Diagram for External Low Speed Clock Source

High-speed external clock generated using a crystal/ceramic resonator

The High Speed External Clock (HSE) can be generated using an oscillator consisting of a 4 to 16 MHz crystal/ceramic resonator. The information given in this section is based on a comprehensive characterization using typical external components listed in the table below. In the application, the resonator and load capacitance must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup.

Table 20 HSE 4~16MHz Oscillator Characteristics(1)(2)

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
fOSC_IN	oscillator frequency		4	8	16	MHz
RF	Feedback resistance			200		kΩ
CL1 CL2(3)	Recommended load capacitance with corresponding The crystal serial impedance (RS) of the	Rs= 30Ω		30		pF
IHSE	HSE Drive Current	VDD=3.3V, VIN=VSS 30pF load			1	mA
gm	Transconductance of the oscillator	activate (a plan)	25			mA/V
tSU(HSE)(5)	activation time	vout stabilization		2		ms

1. Resonator characterization parameters are given by the crystal/ceramic resonator manufacturer.
2. Derived from a comprehensive assessment and not tested in production.
3. For CL2 and CL2, it is recommended to use high quality ceramic dielectric capacitors between 5pF and 25pF (typical) designed for high frequency applications, and to select a crystal or resonator that meets the requirements. Typically, CL1 and CL2 have the same parameters. Crystal manufacturers often give load capacitance parameters as a serial combination of CL1 and CL2. When selecting CL1 and CL2, the capacitance of the PCB and MCU pins should be taken into account (you can roughly estimate the capacitance of the pins to the PCB board at 10pF).
4. Relatively low RF resistance values can provide protection against problems associated with use in humid environments where leakage and bias conditions change. However, this parameter needs to be taken into account when designing MCUs for use in harsh, humid conditions.

5. $t_{SU(HSE)}$ is the startup time, which is the period of time from when the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary greatly depending on the crystal manufacturer.

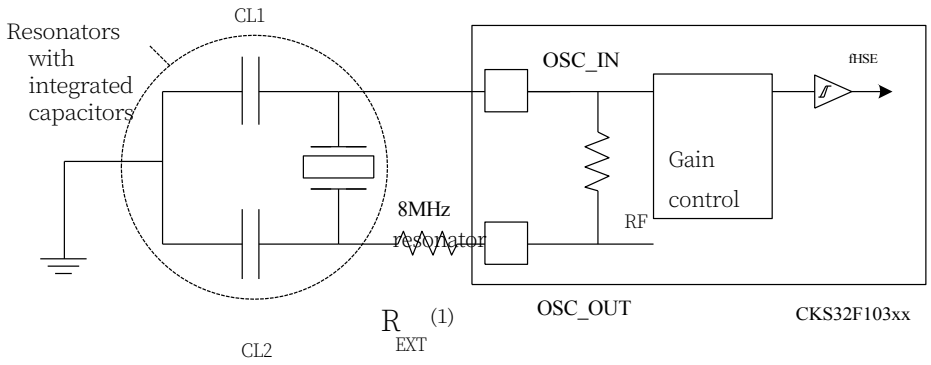


Figure 14 Typical Application Using 8MHz Crystals

1. The R_{EXT} value is determined by the characteristics of the crystal. Typical values are 5 to 6 times R_S.

Low-speed external clock generated using a crystal/ceramic resonator

The Low Speed External (LSE) clock can be generated using an oscillator consisting of a 32.768kHz crystal/ceramic resonator. The information given in this section is based on a comprehensive characterization using typical external components listed in Table 21. In the application, the resonator and load capacitance must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup.

Note: For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric capacitors between *5pF and 15pF*, and select a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give the load capacitance parameters as a serial combination of C_{L1} and C_{L2}.

The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pins and the capacitance associated with the *PCB* board or *PCB*, and its typical value is *between 2pF* and *7pF*.

WARNING: To avoid exceeding the maximum values of C_{L1} and C_{L2} (15pF), it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$pF, and not one with a load capacitance of 12.5pF.

For example, if a resonator with load capacitance CL=6pF and Cstray=2pF is selected, then CL1=CL2=8pF.

Table 21 LSE oscillator characteristics (fLSE=32.768kHz) (1)

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
RF	Feedback resistance			5		MΩ
CL1 CL2(2)	Recommended load capacitance with corresponding	RS= 30kΩ			15	pF

	The crystal serial impedance (R_S) of the (3)					
I_2	LSE Drive Current	VDD=3.3V, V_{IN}=VSS			1.4	μA
gm	Transconductance of the oscillator		5			μA/V
$t_{SU(LSE)}$(4)	activation time	V_{DD} stabilization		3		s

1. Derived from a comprehensive assessment and not tested in production.
2. See the Notes and Warnings paragraph at the top of this form.
3. Current consumption can be optimized by choosing a high quality oscillator with a small R_S value (e.g. MSIV-TIN32.768kHz).
4. $t_{SU(HSE)}$ is the startup time, measured from the time the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary greatly depending on the crystal manufacturer.

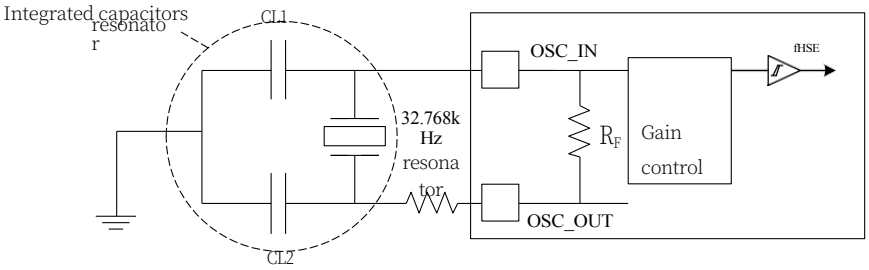


Figure 15 Typical Application Using 32.768kH Crystals

5.3.7 Internal Clock Source Characteristics

The characteristics given in the following table were measured using ambient temperatures and supply voltages in accordance with Table 6.

High Speed Internal (HSI) RC Oscillator

Table 22 HSI Oscillator Characteristics(1)(2)

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
fHSI	frequency			8		MHz
ACCHSI	HSI Oscillator Accuracy	TA= -40~105°C	-2		2.5	%
		TA= -10~85°C	-1.5		2.2	%
		TA= 0~70°C	-1.3		2	%
		TA= 25°C	-1.1		1.8	%
tSU (HSI)	HSI Oscillator Startup Time		1		2	μs
IDD (HSI)	HSI Oscillator Power Consumption			80	100	μA

1. VDD = 3.3V, TA= -40 to 105°C, unless otherwise noted.
2. Guaranteed by design, not tested in production.

Low Speed Internal (LSI) RC Oscillator

Table 23LSI Oscillator Characteristics(1)

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
fLSI (2)	frequency	30	40	60	kHz
tSU(LSI) (3)	LSI Oscillator Startup Time			85	μs
IDD(LSI) (3)	LSI Oscillator Power Consumption		0.65	1.2	μA

1. VDD = 3.3V, TA= -40 to 105°C, unless otherwise noted.
2. Derived from a comprehensive assessment and not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up time from low-power mode

The wake-up times listed in Table 24 were measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used for wake-up depends on the current operating mode:

- Stop or standby mode: clock source is an RC oscillator
- Sleep mode: the clock source is the clock used when entering sleep mode

All times were measured using ambient temperatures and supply voltages in accordance with Table 6.

Table 24 Wake-up times for low-power modes

notation	parameters	prerequisite	typical value	unit (of measure)
$t_{WUSLEEP}$(1)	Wake from sleep mode	Wake-up with HSI RC Clock	1.7	μs
t_{WUSTOP}(1)	Wake-up from shutdown mode (voltage regulation) The device is in run mode)	HSI RC clock wakeup = 2μs	2.6	μs
	Wake-up from shutdown mode (voltage regulation) The device is in low power mode)	HSI RC clock wakeup = 2μs Regulator wake-up time from low-power mode = 5μs	5.1	μs
$t_{WUSTDBY}$(3)	Wake up from standby mode	HSI RC clock wakeup = 2μs Regulator wake-up time from off mode = 38μs	52	μs

1. Wake-up time is measured from the start of the wake-up event until the user program reads the first instruction.

5.3.8 PLL Characterization

The parameters listed in Table 25 were measured using ambient temperatures and supply voltages in accordance with Table 6.

Table 25 PLL Characteristics

notation	parameters	numerical value			unit (of measure)
		minimum value	typical value	maximum value	
f_{PLL_IN}	PLL Input Clock(2)	1	8.0	25	MHz
	PLL Input Clock Duty Cycle (particle used for comparison and "-er than")	40	50	60	%
f_{PLL_OUT}	PLL Multiplier Output Clock	16		72	MHz
t_{LOCK}	PLL phase-lock time		43	200	μs

1. Derived from a comprehensive design and not tested in production.
2. Care needs to be taken to use the correct frequency multiplier factor so that f_{PLL_OUT} is within the allowable range based on the PLL input clock frequency.

5.3.9 Storage characteristics

flash memory

Unless otherwise noted, all characteristics are obtained at TA= -40~105°C.

Table 26 Flash memory characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
tprog	16-bit programming time	TA= -40~105°C	-	-	20	μs
tERASE	Page (1K bytes) Erase Time	TA= -40~105°C	-		2	ms
tME	Whole chip erase time	TA= -40~105°C	-		10	
IDD	Supply Current	Read mode, conditional fHCLK=72MHz, 2 wait cycles, VDD=3.3V			21.6	mA
		Write/erase mode. fHCLK=72MHz, VDD=3.3V			3	
		Standby mode, TA = -40 to 105°C (with a 7 suffix) VDD=3.3~3.6V				μA
NEND	longevity	TA = -40~85°C (6 suffix)	100			thousand times
tRET	Data retention period	TA =-40-85°C	10			surname Nian

1. Guaranteed by design, not tested in production.

Table 27 Flash memory life and data retention period

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
NEND	longevity	TA = -40~85°C (6 suffix)	100			thousand times
tRET	Data retention period	TA =-40-85°C	10			surname Nian

1. Derived from a comprehensive assessment and not tested in production.

5.3.10 EMC Characteristics

Sensitivity testing is performed on a sample of products during a comprehensive evaluation of the product.

Functionality EMS (Electromagnetic Sensitivity)

When running a simple application (2 LEDs blinking through the I/O port), the test sample is subjected to 2 types of electromagnetic interference until an error is generated, which is indicated by the blinking of the LEDs.

- **Electrostatic discharge (ESD)** (positive and negative discharge) is applied to all pins of the chip until a functional error is generated. This test complies with the IEC61000-4-2 standard.
- **FTB:** A pulse train of transient voltages (forward and reverse) is applied across V_{DD} and V_{SS} through a 100pF capacitor until a functional error is generated. This test complies with the IEC61000-4-4 standard.

A chip reset restores the system to normal operation. The test results are listed in the table below.

Table 28 EMS Characteristics

notation	parameters	prerequisite	Level/class model
VFESD	applied to any I/O pin, which results in a functionally incorrect Voltage Limits.	V_{DD} = 3.3V, T_A = +25 °C. f_{HCLK} = 72MHz. in accordance with IEC61000-4-2.	2B
VEFTB	Transient pulse group voltage limits on V_{DD} and V_{SS} applied through a 100pF	V_{DD} = 3.3V, T_A = +25 °C. f_{HCLK} = 72MHz. in accordance with	4A

Designing robust software to avoid noise problems

Evaluation and optimization of EMC at the device level is performed in a typical application environment. It should be noted that good EMC performance is closely related to the user application and specific software.

Therefore, it is recommended that the user optimizes the software for EMC and performs EMC-related certification tests.

Software Recommendations

The flow of the software must include controls for the program to run and fly, for example:

- Destroyed program counters
- Unexpected reset
- Critical data destroyed (control registers, etc. .....)

Pre-certification tests

Many common failures (accidental resets and corrupted program counters) can be reproduced by artificially introducing a low level on NRST or a low level on the crystal pins that lasts 1 second.

During ESD testing, voltages in excess of the application requirements can be applied directly to the chip, and where unexpected actions are detected, the software section needs to be enhanced to prevent unrecoverable errors.

Electromagnetic interference (EMI)

The EMF emitted by the chip is monitored while running a simple application (blinking 2 LEDs through the I/O port). This emission test complies with SAE J1752/3, which specifies the loads on the test board and pins.

Table 29 EMI Characteristics

notation	parameters	prerequisite	Frequency bands monitored	Maximum (f_{HSE}/f_{HCLK})		unit (of measure)
				8/48MHz	8/72MHz	
SEMI	peak value	VDD= 3.3 V, TA= 25°C, LQFP100 package according to IEC 61967-2	0.1~30MHz	12	12	dBμV
			30~130MHz	22	19	
			130MHz~1GHz	23	29	
			SAM EMI Class pin	4	4	-

5.3.11 Absolute maximum (electrical sensitivity)

Based on three different tests (ESD, LU), using specific measurements, the chip is strength tested to determine its performance in terms of electrical sensitivity.

Electrostatic Discharge (ESD)

An electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples, the size of which is related to the number of power supply pins on the chip (3 slices x (n+1) power supply pins). This test complies with the JESD22-A114/ C101 standard.

Table 30 ESD Absolute Maximum Values

notation	parameters	prerequisite	typology	Maximum value (1)	unit (of measure)
VESD (HBM)	Electrostatic discharge voltage (human model)	T = +25 °C, symbol Hop JESD22-A114	2	2000	V
VESD (CDM)	Electrostatic discharge voltage (charging equipment mode)	T = +25 °C, symbol Hop JESD22-C101	II	500	

1. Derived from a comprehensive assessment and not tested in production.

static bolt lock

To evaluate bolting performance, 2 complementary static bolting tests on 6 samples are required:

- For each power supply pin, provide a supply voltage that exceeds the limit.
- Current is injected on each input, output, and configurable I/O pin. This test complies with the EIA/JESD 78A integrated circuit latch standard.

Table 31 Electrical sensitivity

notation	parameters	prerequisite	typology
LU	Static bolts (table)	T = +105 °C according to JESD78A	Category II A

5.3.12 I/O Port Characteristics

Generalized Input/Output Characteristics

Unless otherwise noted, the parameters listed in the following table were measured according to the conditions in Table 6. All I/O ports are CMOS-compatible and TTL.

Table 32 I/O Static Characteristics

notation	parameters	prerequisite	minimum value	typical value	maximum values	unit (of measure)
VIL	Low Level Input Voltage	Standard I/O Pin, Input Low Level Voltage	-	-	0.28×(VDD-2V)+0.8V	V
		FT I/O(1) pin, input Low Level Voltage			0.32 x (VDD-2V) +0.75V	
		All I/O ports except BTOOT0			0.35 VDD	
VIH	High Level Input	Standard I/O Pin, Input High Level Voltage	0.41×(VDD-2V)+1.3V			

	Trigger voltage hysteresis(2)					
	5V Tolerant to I/O Pin Schmitt Trigger Voltage Hysteresis (2)		5%VDD(3)			
Ilkg	Input Leakage Current(4)	VSS ≤ VIN ≤ VDD Standard I/O Ports			±1	μA
		VIN = 5V. 5V Tolerance Port			3	
RPU	Weak pull-up equivalent resistance(5)	VIN = VSS	30	44	50	kΩ
RPD	Weak pull-down equivalent resistance(5)	VIN = VDD	30	44	50	
CIO	I/O Pin Capacitance			5		pF

1. FT = 5V Tolerance.
2. Hysteresis voltage of the Schmitt trigger switching level. Derived from a comprehensive evaluation and not tested in production.
3. The voltage is at least 100mV.
4. The leakage current may be higher than the maximum value if there is a reverse current back-up at an adjacent pin.
5. The pull-up and pull-down resistors are designed as a true resistor in series with a switchable PMOS/NMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).

All I/O ports are CMOS- and TTL-compatible (no software configuration required), and their characteristics take into account most of the stringent CMOS process or TTL parameters:

- For VIH:
  - If VDD is between [2.00V~3.08V]; use CMOS characteristics but include TTL.
  - If VDD is between [3.08V~3.60V]; use TTL characteristics but include CMOS.
- For VIL:
  - If VDD is between [2.00V~2.28V]; use TTL characteristics but include CMOS.
  - If VDD is between [2.28V~3.60V]; use CMOS characteristics but include TTL.

Output drive current

The GPIOs (General Purpose Input/Output Ports) can absorb or output up to +/-8mA and

absorb +20mA (not strictly V). In user applications, the number of I/O pins must be such that the drive current does not exceed the absolute maximum ratings given in section 5.2:

- The sum of the currents drawn by all I/O ports from V, plus the maximum operating current drawn by the MCU o n V, must not exceed the absolute maximum rating, IVDD (see Table 4).
- The sum of the currents absorbed by all I/O ports and flowing off of V, plus the maximum operating current flowing off o f V by the MCU, must not exceed the absolute maximum rating of IVSS (see Table 4).

output voltage

Unless otherwise noted, the parameters listed in Table 33 were measured using ambient temperatures and $_{VDD}$ supply voltages in accordance with Table 6. All

The I/O ports are CMOS and TTL compatible.

Table 33 Output Voltage Characteristics

notation	parameters	prerequisite	minimum value	maximum values	unit (of measure)
V_{OL} (1)	Output low, when all 8 pins draw current at the same time	CMOS port, I_{IO} = +8mA 2.7V < VDD< 3.6V		0.4	V
V_{OH} (2)(3)	Output high, when all 8 pins output current at the same time		VDD-0.4		
V_{OL} (1)	Output low, when all 8 pins draw current at the same time	TLL Port, I_{IO} = +8mA 2.7V < VDD< 3.6V		0.4	
V_{OH} (2)(3)	Output high, when all 8 pins output current at the same time		2.4		
V_{OL} (1)(3)	Output low, when all 8 pins draw current at the same time	I_{IO} = +20mA 2.7V < VDD< 3.6V		1.3	
V_{OH} (2)(3)	Output high, when all 8 pins output current at the same time		2.4		
V_{OL} (1)(3)	Output low, when all 8 pins draw current at the same time	I_{IO} = +6mA 2V < VDD< 2.7V		0.4	
V_{OH} (2)(3)	Output high, when all 8 pins output current at the same time		VDD-0.4		

1. The current I_{IO} absorbed by the chip must always follow the absolute maximum ratings given in Table 4, while the sum of the I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.
2. The current I_{IOs} output from the chip must always follow the absolute maximum ratings given in Table 4, while the sum of the I_{IOs} (all I/O pins and control pins) must not exceed I_{VDD}.
3. Derived from a comprehensive assessment and not tested in production.

Input/Output AC Characteristics

The definitions and values of the input and output AC characteristics are given in Figure 16 and Table 34, respectively.

Unless otherwise specified, the listed parameters were measured using ambient temperatures and supply voltages in accordance with Table 6.

Table 34 Input/Output AC Characteristics(1)

MODEx[1:0]	notation	parameters	prerequisite	minimum value	maximum values	unit (of measure)
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency(2)	CL= 50 pF,VDD= 2~3.6V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	CL= 50 pF,VDD= 2~3.6V		125(3)	ns
	$t_{r(IO)out}$	Output low-to-high rise time			125(3)	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency(2)	CL= 50 pF,VDD= 2~3.6V		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	CL= 50 pF,VDD= 2~3.6V		25(3)	ns
	$t_{r(IO)out}$	Output low-to-high rise time			25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	CL= 30 pF,VDD= 2.7~3.6V		50	MHz
			CL= 50 pF,VDD= 2.7~3.6V		30	
			CL=50 pF,VDD= 2~2.7V		20	

		Pulse width of No.				

1. The speed of the I/O port can be configured via MODEx[1:0]. See the CKS32F103x8 and CKS32F103xB reference manuals for a description of the GPIO port configuration registers.
2. The maximum frequency is defined in Figure 16.
3. Guaranteed by design, not tested in production.

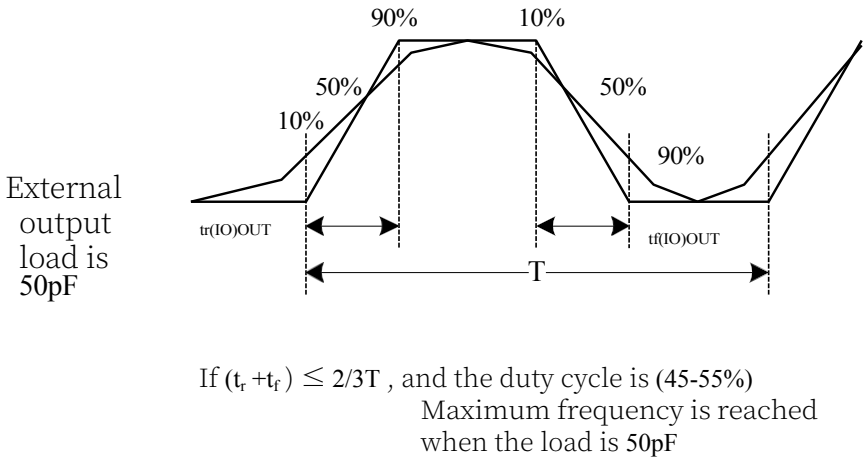


Fig. 16 Definition of Input and Output AC Characteristics

5.3.13 NRST Pin Characteristics

The NRST pin input driver uses a CMOS process which connects a pull-up resistor, R_{PU}, that cannot be disconnected (see Table 32). Unless otherwise noted, the parameters listed in Table 35 were measured using ambient temperature and V_{DD} supply voltage in accordance with Table 6.

Table 35NRST Pin Characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
$V_{IL(NRST)}$(1)	NRST Input Low Level Voltage		-0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input High Voltage		2		VDD+0.5	
$V_{hys(NRST)}$(1)	NRST Schmitt Trigger Voltage Latte sluggish			200		mV
R_{PU}	Weak pull-up equivalent resistance(2)	VIN=VSS	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input Filter Pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input Unfiltered Pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is designed as a true resistor in series with a switchable PMOS implementation. The resistance of this PMON/NMOS switch is approximately 10%.

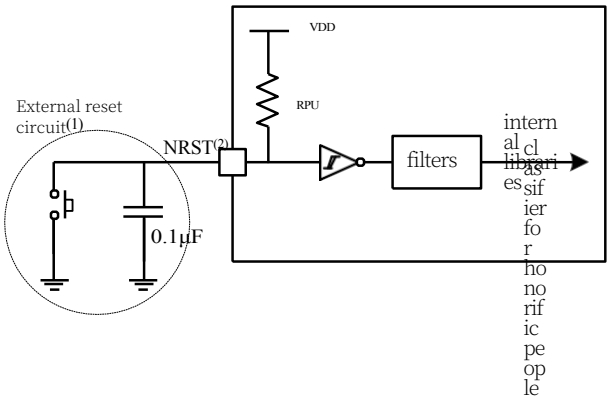


Figure 17 Recommended NRST Pin Protection

1. The reset network is designed to prevent parasitic resets.
2. The user must ensure that the potential of the NRST pin can fall below the maximum $V_{IL(NRST)}$ listed in Table 35, otherwise the MCU cannot be reset.

5.3.14 TIM Timer Features

The parameters listed in Table 36 are guaranteed by design.

For details on the characteristics of the input/output multiplexing function pins (output compare, input capture, external clock, PWM output), refer to Section 5.3.12.

Sections.

Table 36TIMx(1) Characteristics

notation	parameters	prerequisite	minimum value	maximum values	unit (of measure)
tres(TIM)	Timer Resolution Time		1		tTIMxCLK
		fTIMxCLK= 72MHz	13.9		ns
fEXT	Timers for CH1 to CH4 External Clock Frequency		0	fTIMxCLK/2	MHz
		fTIMxCLK = 72MHz	0	36	MHz
ResTIM	Timer Resolution			16	bit
tCOUNTER	When the internal clock is selected, CK_INT 16-bit Counter Clock Cycle		1	65536	tTIMxCLK
		fTIMxCLK= 72MHz	0.0139	910	µs
tMAX_COUNT	Maximum possible count			65536×65536	tTIMxCLK
		fTIMxCLK= 72MHz		59.6	s

1. TIMx is a generic name that stands for TIM1~TIM4.

5.3.15 communications interface

I2C Interface Features

Unless otherwise noted, the parameters listed in Table 50 and Table 37 were measured using ambient temperature, f_{PCLK1} frequency, and V supply voltage in accordance with Table 6.

The I2C interface of the CKS32F103x8 and CKS32F103xB standard models conforms to the standard I2C

communication protocol with the following limitations: SDA and SCL is not a "true" open-drain pin; when configured as an open-drain output, the PMOS tube between the pin and V_{DD} is turned off but still present.

The I^2C interface characteristics are listed in Table 37 and see Section 5.3.12 for details on the characteristics of the input/output multiplexing function pins (SDA and SCL).

Table 37I² C Interface Characteristics

notation	parameters	Standard I2C(1)		Fast I2C(1)(2)		unit (of measure)
		maximum values	minimum value	maximum values	minimum value	
tw(SCLL)	SCL Clock Low Time	4.7		1.3		μs
twSCLH)	SCL Clock High Time	4.0		0.6		
tsu (SDA)	SDA build-up time	250		100		ns
th (SDA)	SDA Data Hold Time	0(3)		0(4)	900(3)	
tr(SDA) tr(SCL)	SDA and SCL Rise Time		1000	20+0.1Cb	300	
tfSDA) tfSCL)	SDA and SCL downtime		300		300	
th (STA)	Start condition hold time	4.0		0.6		μs
tsu (STA)	Repeat start condition establishment time	4.7		0.6		
tsu (STO)	Stop condition establishment time	4.0		0.6		μs
tw(STO:STA)	Time from stop condition to start condition Interval (Bus Idle)	4.7		1.3		μs
Cb	Tolerance load per bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. To achieve the maximum frequency for standard mode I² C, f_{PCLK1} must be greater than 2 MHz. f_{PCLK1} must be greater than 4 MHz to achieve the maximum frequency for fast mode I² C.
3. If an elongated SCL signal low time is not required, only the maximum hold time for the start condition is required.
4. In order to cross the undefined region of the falling edge of SCL, a hold time of at least 300ns on the SDA signal must be guaranteed within the MCU.

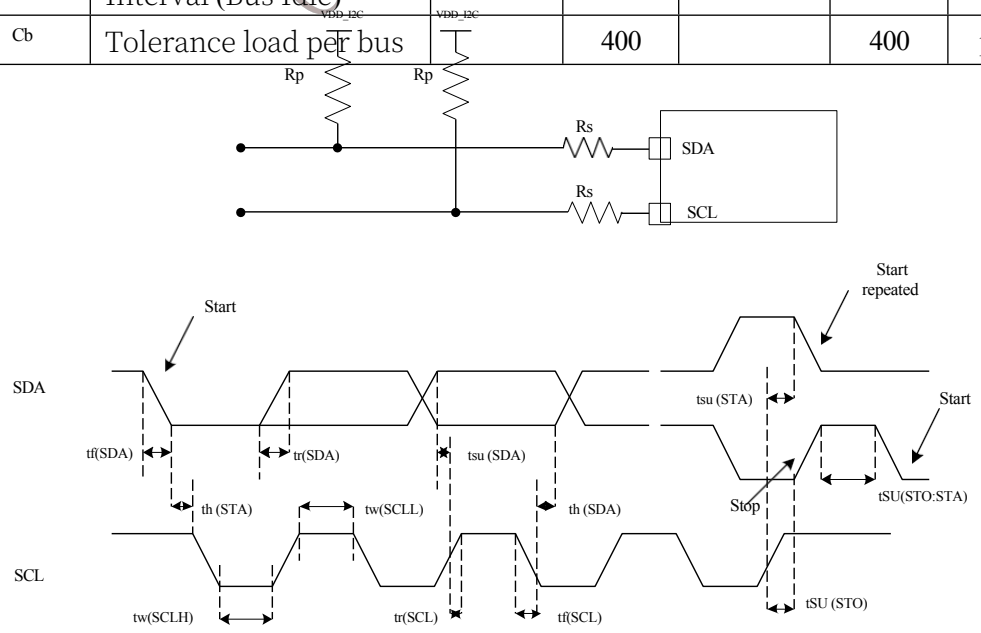


Figure 18 I2C Bus AC Waveform and Measurement Circuitry(1)

1. The measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 38SCL frequency (f_{PCLK1} = 36MHz, V_{DD} = 3.3V) (1)(2)

fSCL(kHz)	I2C_CCR Values
	RP=4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. RP= external pull-up resistor, fSCL=I² C speed.
2. For speeds around 200kHz, the error in speed is ±5%. For other speed ranges, the error in speed is ±2%. These variations depend on the accuracy of the external components in the design.

SPI Interface Features

Unless otherwise noted, the parameters listed in Table 39 were measured using the ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with the conditions in Table 6.

For details on the characteristics of the input/output multiplexing function pins (NSS, SCK, MOSI, MISO), see Section 5.3.12.

Table 39SPI Characteristics(1)

notation	parameters	conditional	minimum value	maximum values	unit (of measure)
fSCK 1/tc(SCK)	SPI Clock Frequency	Master Mode	-	18	MHz
		modal	-	18	
tr(SCK) tf(SCK)	SPI Clock Up and Down timing	Load capacitance: C = 30pF	-	8	ns
Ducy (SCK)	Slave Input Clock Duty Cycle	modal	30	70	%
tsu(NSS)(2)	NSS Establishment Time	modal	4tPCLCK	-	ns
th (NSS)(2)	NSS Hold Time	modal	2tPCLCK	-	
tw(SCKH)(2) tw(SCKL)(2)	SCK high and low time	Master mode, f_{PCLK} = 36MHz, preshunt factor = 4	50	60	
tsu(MI)(2) tsu(SI)(2)	Data Entry Establishment Time, Main paradigm	Master Mode	5		
		modal	5		
th(MI)(2) th(SI)(2)	Data Entry Hold Time, Main paradigm	Master Mode	5		
		modal	4		
ta(SO)(2)(3)	Data output access	Slave mode, f_{PCLK} = 20MHz	0	3tPCLCK	

1. The SPI1 characterization of the remapping needs to be further determined.
2. Derived from a comprehensive assessment and not tested in production.
3. The minimum value indicates the minimum time to drive the output, and the maximum value indicates the maximum time to get the data correctly.
4. The minimum value indicates the minimum time to turn off the output, and the maximum value indicates the maximum time to place the data line in a high resistance state.

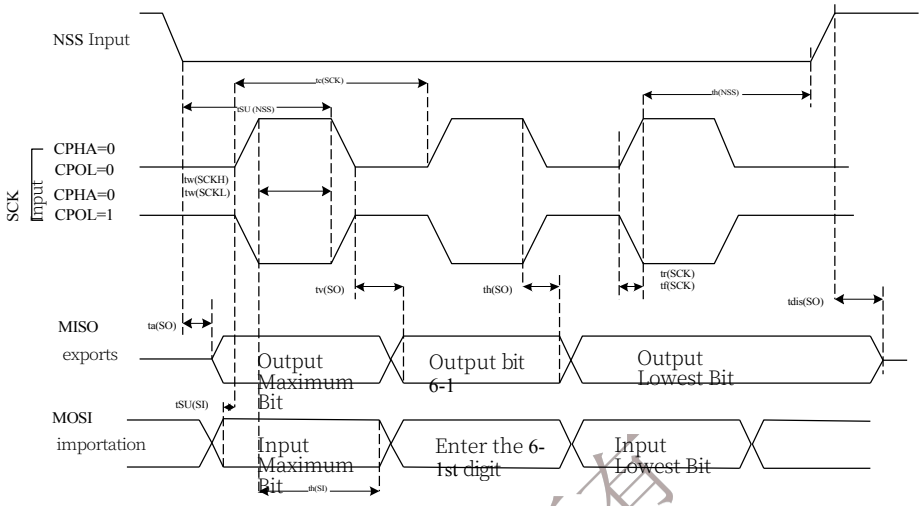


Figure 19SPI Timing Diagram-Slave Mode and CPHA=0

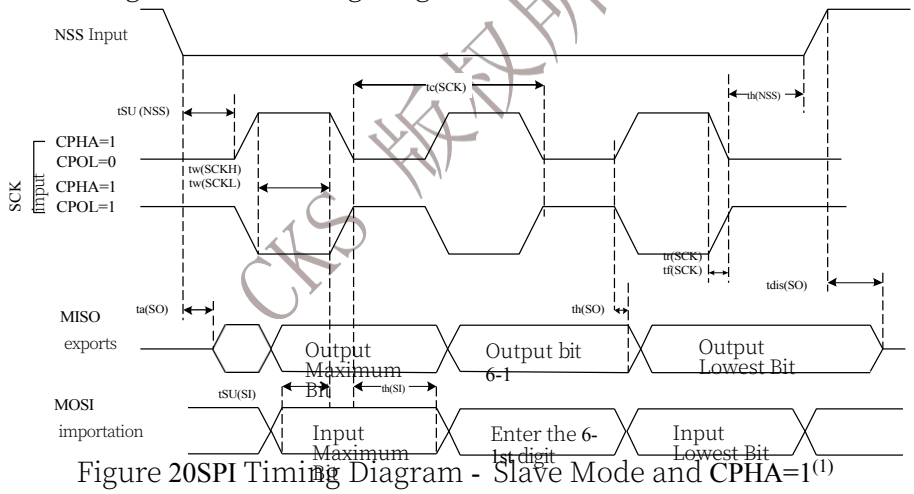


Figure 20SPI Timing Diagram - Slave Mode and CPHA=1(1)

1. The measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

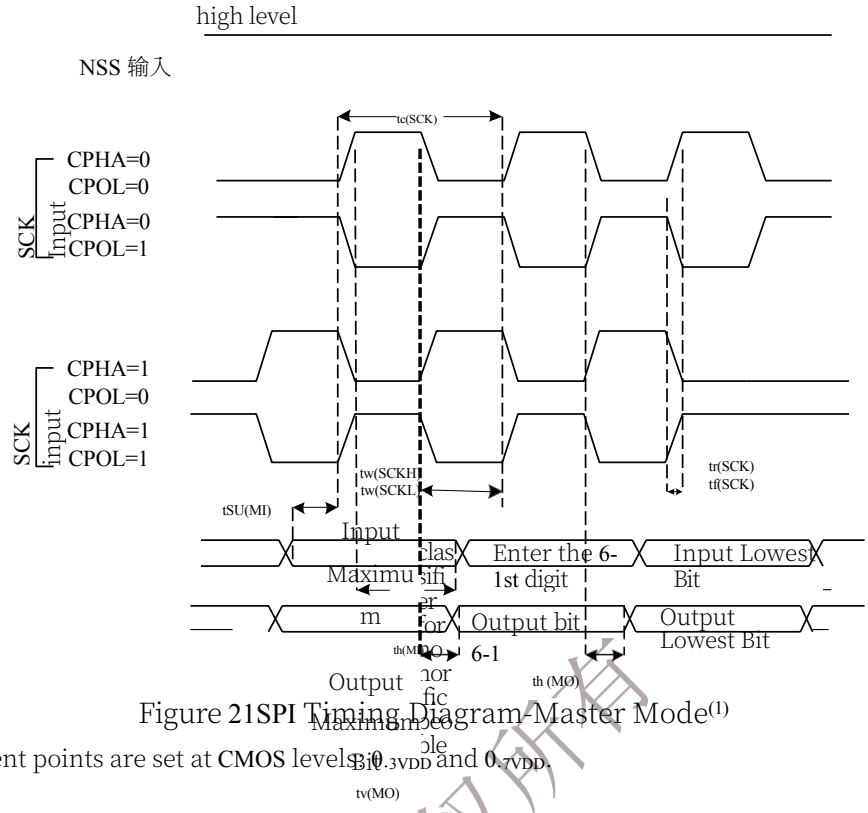


Figure 21SPI Timing Diagram-Master Mode(1)

1. The measurement points are set at CMOS levels: 0.3VDD and 0.7VDD.

USB Characteristics

The USB (Full Speed) interface is USB-IF certified.

Table 40USB Startup Time

notation	parameters	maximum values	unit (of measure)
$t_{STARTUP}$(1)	USB Transceiver Startup Time	1	µs

1. Guaranteed by design, not tested in production.

Table 41USB DC Characteristics

notation	parameters	prerequisite	Minimum(1)	Maximum value (1)	unit (of measure)
Input level					
V_{DD}	USB Operating Voltage(2)		3.0(3)	3.6	V
V_{DI} (4)	Differential Input Sensitivity	I(USBDP,USBDM)	0.2		V
V_{CM}(4)	Differential common mode range	Includes V_{DI} scopes	0.8	2.5	
V_{SE}	Single-Ended Receiver Threshold		1.3	2.0	
output level					
V_{OL}	Static output low level	1.5kΩ RL to 3.6V(5)		0.3	V
V_{OH}	Static Output High	15kΩ RL to V_{SS} (5)	2.8	3.6	

1. All voltage measurements are based on the ground at the equipment end.
2. For compatibility with the USB 2.0 full-speed electrical specification, the USBDP(D+) pin must be connected to a voltage of 3.0~3.6V through a 1.5kΩ resistor.
3. The correct USB functionality of the CKS32F0103xx is guaranteed at 2.7V instead of the degraded electrical characteristics in the 2.7~3.0V voltage range.

4. Assured by comprehensive evaluation, not tested in production.
5. R_L is the load connected to the USB drive.

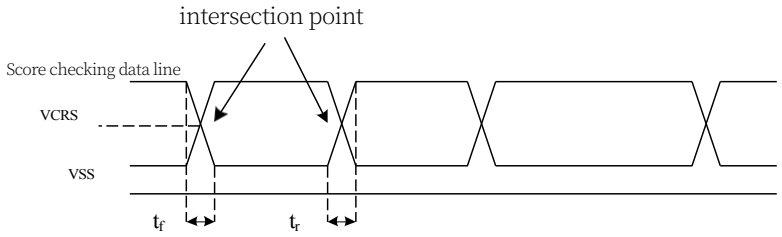


Figure 22USB Timing: Data Signal Rise and

Fall Time Definitions Table

notation	parameters	conditional	minimum value	maximum values	unit (of measure)
tr	rising time(2)	CL ≤ 50pF	4	20	ns
tf	descent time(2)	CL ≤ 50pF	4	20	ns
trfm	Rise and fall time matching	tr / tf	90	110	%
VCRS	Output Signal Cross Voltage		1.3	2.0	V

42USB Full Speed Electrical Characteristics(1)

1. Guaranteed by design, not tested in production.
2. Measurement data signal from 10% to 90%.

5.3.16 CAN (Controller Area Network) interface

See Section 5.3.12 for details on the characteristics of the input/output multiplexing function pins (CAN_TX and CAN_RX).

5.3.17 12-Bit ADC Characterization

Unless otherwise noted, the parameters in Table 43 are measured using ambient temperature, f_{PCLK2} frequency, and V_{DDA} supply voltage that meet the conditions in Table 6.

NOTE: It is recommended that a calibration be performed at each power-up.

Table 43ADC Characteristics

notation	parameters	conditional	minimum value	typical value	maximum values	unit (of measure)
VDDA	Supply Voltage	-	2.4	-	3.6	V
VREF+	Positive reference voltage	-	2.4	-	VDDA	V
IVREF	Voltage at V input pin	-	-	160(1)	220(1)	μA
fADC	ADC Clock Frequency	-	0.6	-	14	MHz
fS(2)	sampling rate	-	0.05	-	1	MHz
fTRIG(2)	External Trigger	fADC=14MHz	-	-	823	kHz
						1/fADC

V_{AIN}(3)	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} Connect to ground)	-	V_{REF+}	V
R_{AIN} (2)	External Input Impedance		-	-	50	kΩ
R_{ADC}(2)	Sampling Switch Resistor		-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitance				8	pF
t_{CAL}(2)	calibration time	fADC=14MHz	5.9			μs
			83			1/fADC
t_{lat}(2)	Injection Trigger Conversion Delay	fADC=14MHz			0.214	μs
					3(4)	1/fADC
t_{latr}(2)	Regular Trigger Transition Delay	fADC=14MHz			0.143	μs
					2(4)	1/fADC
t_S(2)	sampling time	fADC=14MHz	0.107		17.1	μs
			1.5		239.5	1/fADC
t_{STAB}(2)	power-on time		0	0	1	μs
t_{CONV}(2)	Total conversion time (including sampling time)	fADC=14MHz	1		18	μs
			14~252 (sampling tS+ progressively approaching 12.5)			1/fADC

1. Assured by a comprehensive assessment, not tested in production.
2. Guaranteed by design, not tested in production.
3. In QFN36, LQFP48, and LQFP64 packages, V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}. see Table 2 for details.
4. For external triggering, a delay $1/f_{PCLK2}$ must be added to the delays listed in Table 43.

Formula 1:

Maximum R_{AIN} Formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above equation (Equation 1) is used to determine the maximum external impedance that will allow an error of less than 1/4 LSB, where N=12 (for 12-bit resolution).

Table 44 fADC = Maximum R_{AIN} at 14MHz (1)

T_S (cycle)	t_S (μs)	Maximum R_{AIN} (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50

1. Guaranteed by design, not tested in production.

Table 45ADC Accuracy - Restricted Test Conditions(1)(2)

notation	parameters	test condition	typical value	Maximum value (3)	unit (of measure)
ET	Aggregate error	f_{PCLK2} = 56 MHz f_{ADC} = 14 MHz, RAIN< 10 kΩ, V_{DDA} = 3 - 3.6V, T_A= 25 °C Measurements are performed after ADC calibration	±1.3	±2	LSB
EO	offset error		±1	±1.5	
EG	gain error		±0.5	±1.5	
ED	differential linear error (DLE)		±0.7	±1	
EL	Integral Linearity Error		±0.8	±1.5	

1. The DC accuracy value of the ADC is measured after an internal calibration.
2. ADC Accuracy vs. Reverse Current Injection: It is important to avoid injecting reverse current on any standard analog input pin, as this can significantly degrade the accuracy of a conversion being performed on another analog input pin. It is recommended that a Schottky diode be added to the standard analog pin (between the pin and ground) where reverse injection current may be generated.

   The ADC accuracy will not be affected if the forward injection current, as long as it is within the $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ ranges given in Section 5.3.12.
3. Assured by comprehensive evaluation, not tested in production.

Table 46ADC Accuracy(1)(2)(3)

notation	parameters	test condition	typical value	Maximum value (3)	unit (of measure)
ET	Aggregate error	f_{PCLK2} = 56 MHz f_{ADC} = 14 MHz, RAIN< 10 kΩ, V_{DDA} = 2.4 - 3.6V Measurements are performed after ADC calibration	±2	±5	LSB
EO	offset error		±1.5	±2.5	
EG	gain error		±1.5	±3	
ED	differential linear error (DLE)		±1	±2	
EL	Integral Linearity Error		±1.5	±3	

1. The DC accuracy value of the ADC is measured after an internal calibration.
2. Optimal performance can be achieved over restricted V_{DDA} frequency, V_{REF}, and temperature ranges.
3. ADC Accuracy vs. Reverse Current Injection: It is important to avoid injecting reverse current on any standard analog input pin, as this can significantly degrade the accuracy of a conversion being performed on another analog input pin. It is recommended that a Schottky diode be added to the standard analog pin (between the pin and ground) where reverse injection current may be generated.

   The ADC accuracy will not be affected if the forward injection current, as long as it is within the $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ ranges given in Section 5.3.12.
4. Assured by comprehensive evaluation, not tested in production.

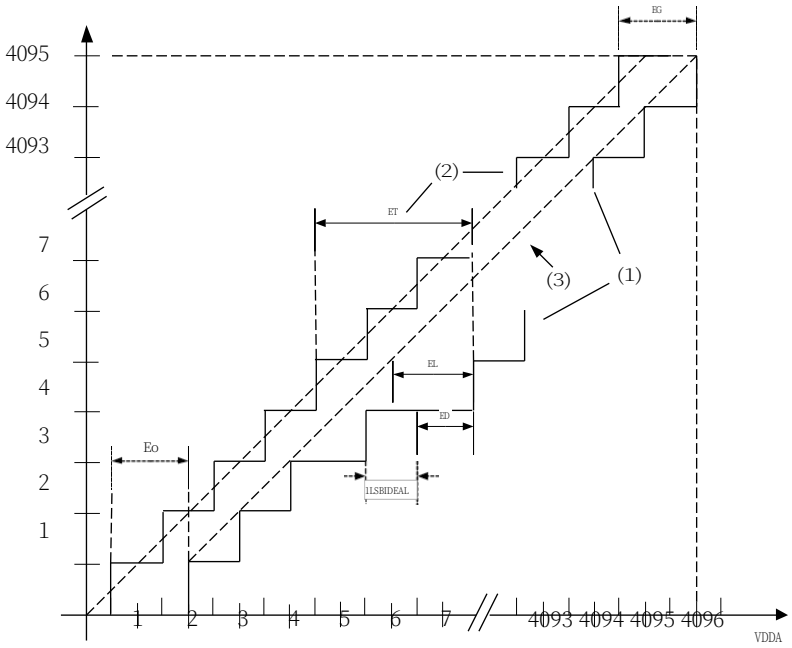


Figure 23ADC Accuracy Characteristics

(1) Example of an actual ADC conversion curve

(2) Ideal Conversion Curve

(3) Actual conversion point connection

E_T Combined error: the maximum deviation between the actual conversion curve and the ideal conversion curve.

Eo offset error: the difference between the first leap on the actual conversion curve and the first leap on the ideal conversion curve.

E_G Gain error: the difference between the last leap on the actual conversion curve and the last leap on the ideal conversion curve.

E_D Differential Linearity Error: The difference between the actual step on the conversion curve and the ideal step (1LSB). Where 1LSBIDEAL=VREF+/4096 (or VDDA/4096, depending on the package)

E_L Integral linearity error: Maximum deviation of the actual conversion curve from the endpoint line.

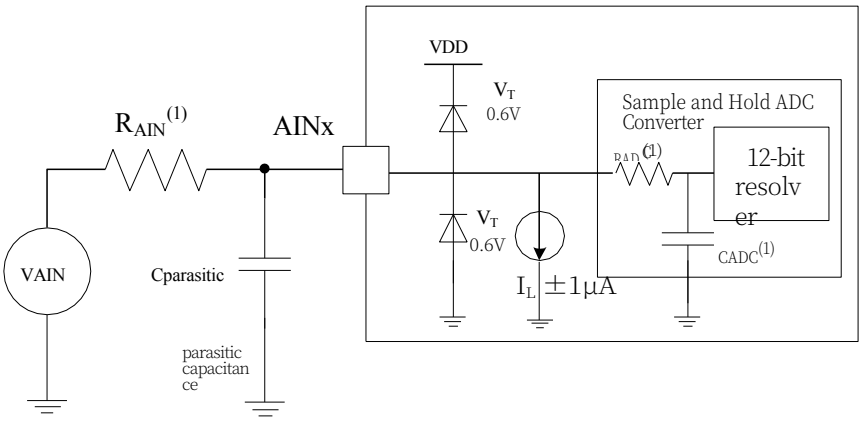


Figure 24 Typical Connection Diagram Using ADCs

1. See Table 46 for R_{AIN}, R_{ADC}, and C_{ADC} values.

2. Cparasitic represents the parasitic capacitance (about 7pF) of the PCB (related to the quality of soldering and PCB layout) with respect to the pads. Larger Cparasitic values will reduce the accuracy of the conversion and the solution is to reduce the f_{ADC}.

PCB Design Recommendations

Depending on whether V_{REF+} is connected to V_{DDA} or not, the decoupling of the power supply must be connected according to Figure 25 or Figure 26. The 10nF capacitors shown must be dielectric capacitors and should be placed as close as possible to the MCU chip.

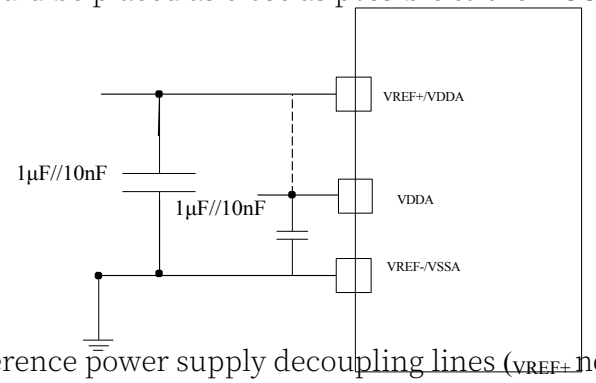


Figure 25 Supply and reference power supply decoupling lines (V_{REF+} not connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are only found on products with 100 feet or more.

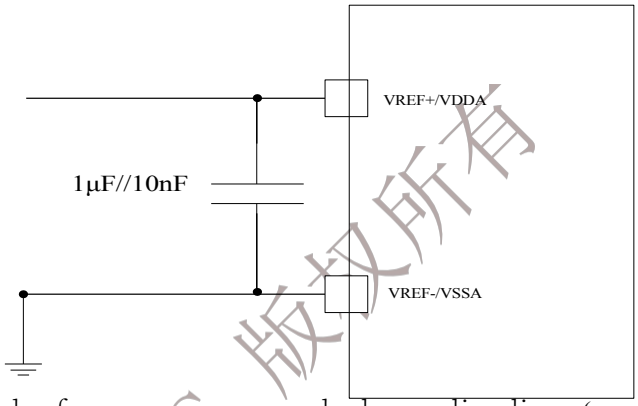


Figure 26 Supply and reference power supply decoupling lines (V_{REF+} connected to V_{DDA})

1. The V_{REF+} and V_{REF-} inputs are only found on products with more than 100 pins.

5.3.18 Temperature Sensor Characteristics

Table 47 Temperature Sensor Characteristics

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
T_L (1)	V_{SENSE} Linearity with respect to temperature		±1	±2	°C
Avg_Slope(1)	average slope	4.0	4.3	4.6	mV/°C
V_{25} (1)	Voltage at 25°C	1.61	1.62	1.63	V
t_{START} (2)	Establishment time	4		10	μs
T_{S_temp} (2)(3)	ADC sampling time when reading temperature	17.1			μs

1. Assured by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The minimum sampling time can be determined by the application program through multiple cycles.

6. Package Characteristics

6.1 Encapsulated mechanical data

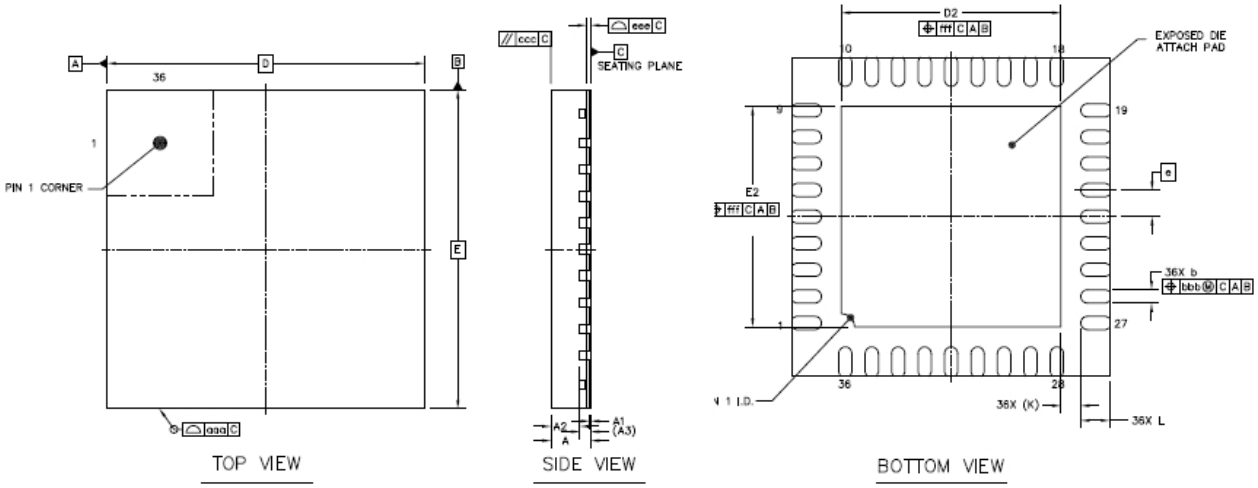
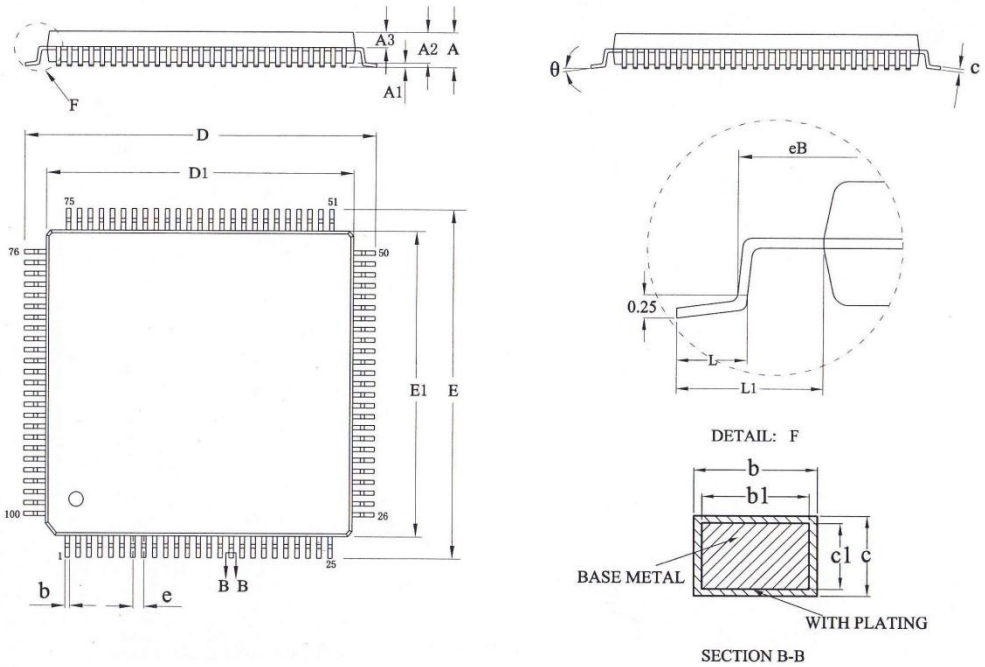


Figure 27QFN36 Package Diagram

Table 48QFN36 Package Mechanical Data

grade	millimetre		
	minimum value	typical value	maximum values
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	6 BSC		
E	6 BSC		
e	0.5 BSC		
D2	4.05	4.15	4.25
E2	4.05	4.15	4.25
K	0.375 REF		
L	0.45	0.55	0.65
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		



\windshield

Figure 28LQFP100, 100-pin low-profile

square flat package diagram Table

gradLQFP100, 100-pin low-profile square flat package data	millimetre		
	minimum value	typical value	maximum values
A			1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.20
eB	15.05	-	15.35
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

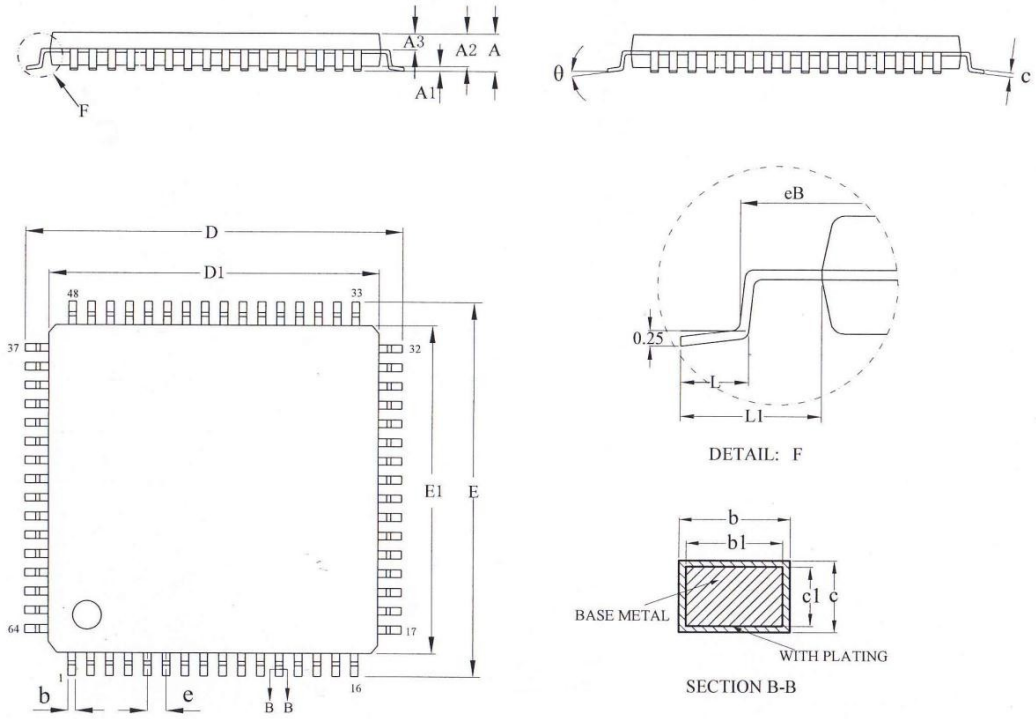


Figure29 LQFP64, 64-pin low-profile

square flat package diagram Table 50

grade LQFP64, 64-pin low-profile square flat package data	millimetre		
	minimum value	typical value	maximum values
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.25	-	11.45
E1	9.90	10.00	10.10
e	0.50BSC		
θ	O°	-	7°
L	0.45	-	0.75
L1	1.00REF		

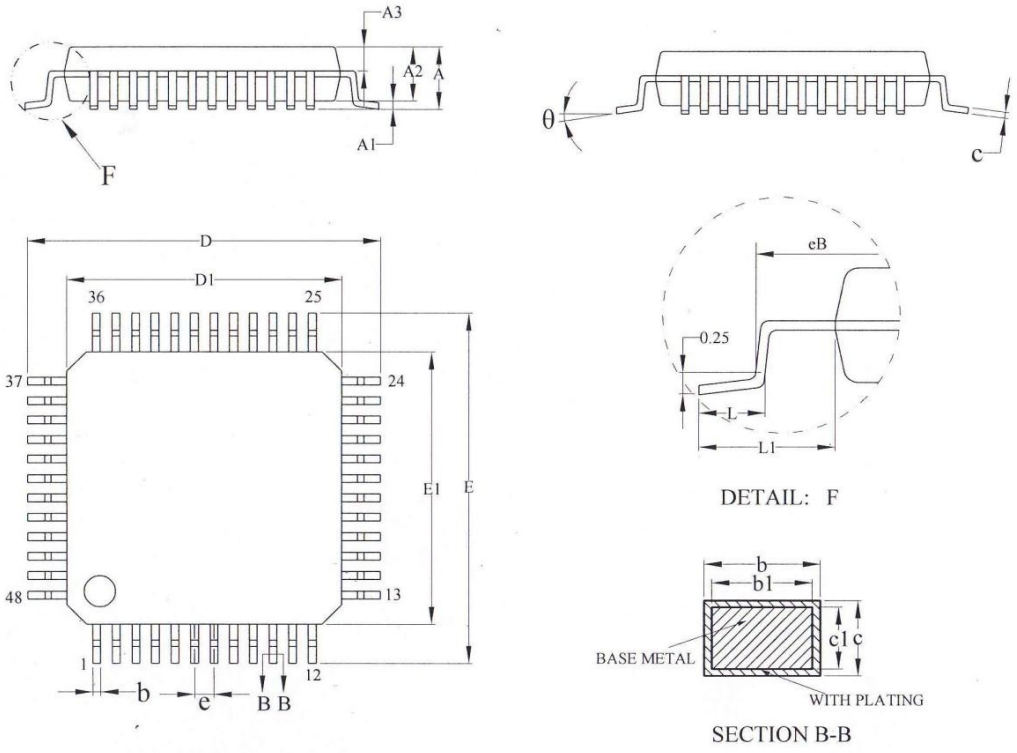


Figure 30LQFP48, 48-pin low-profile

square flat package Diagram 51LQFP48,

grade 48-pin low-profile square flat package data	millimetre		
	minimum value	typical value	maximum values
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.20
eB	8.10	-	8.25
e	0.50BSC		
L	0.40	-	0.65

L1	1.00REF		
k	0	-	7°

6.2 thermal property

The maximum junction temperature (TJmax) of the chip must not exceed the range of values given in Table 6.

The maximum junction temperature (TJmax) of the chip is expressed in Celsius and can be calculated by the following formula:

$$TJmax = TAmax + (PDmax \times \Theta JA)$$

Among them:

- TAmax is the maximum ambient temperature, expressed in °C.
- ΘJA is the thermal impedance of the junction to ambient in the package, labeled in °C/W.
- PDmax is the sum of PINTmax and PI/Omax (PDmax = PINTmax + PI/Omax).
- PINTmax is the product of I_{DD} and V_{DD}, expressed in watts, and is the maximum internal power consumption of the chip.

PI/Omax is the maximum power consumption of all output pins:

$$PI/Omax = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}).$$

Consider the actual $V_{OL/IOL}$ and $V_{OH/IOH}$ that are low and high on the I/O in the application.

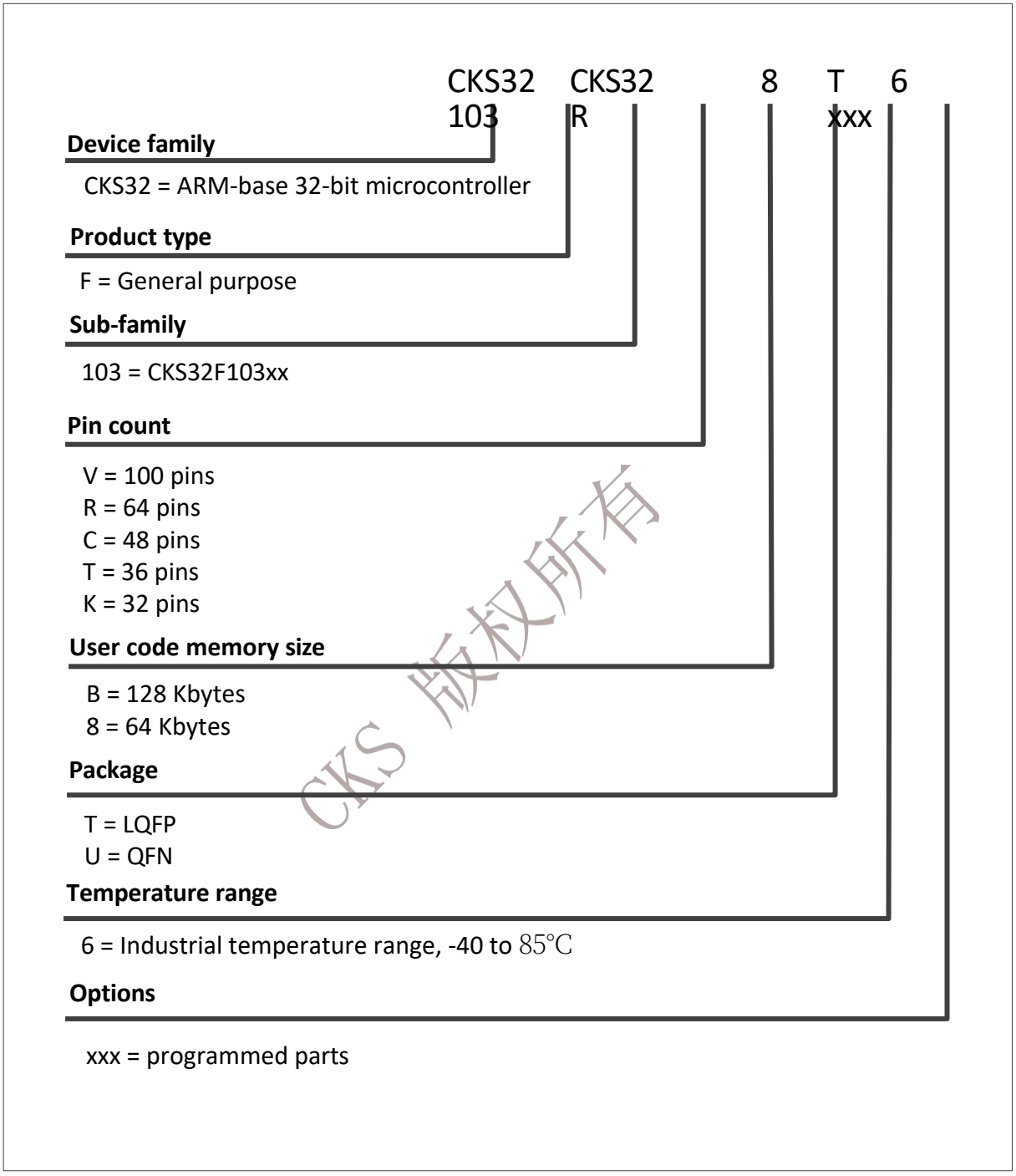
Table 52 Thermal Characteristics of Packages

notation	parameters	numerical value	unit (of measure)
ΘJA	Thermal Impedance to Environment - LQFP100 - 14×14mm/0.5mm Pitch	46	℃/W
	Thermal Impedance of Junction to Environment - LQFP64 - 10×10mm/0.5mm Pitch	45	
	Thermal Impedance of Junction to Environment - LQFP48 - 7×7mm/0.5mm Pitch	55	
	Thermal impedance of junction to environment - QFN36-6×6mm/0.5mm pitch	18	

6.2.1 reference document

JESD51-2 Environmental Conditions for Thermal Measurements of Integrated Circuits-Natural Convection (Air at Rest). See www.jedec.org.

7. Model Naming



8. Version History

dates	releases	revised part
2018.01.18	Initial draft	
2018.04.20	1.0	Modify the pin definitions for pin 80 and pin 81 in Figure 3; Typical values with 48MHz clock are added in Table 14;
2018.08.11	1.1	Add Table 15 Typical Current Consumption in Run Mode, Data Processing Code from Internal Running in RAM; Modify the clock in Table 16 to the typical value at 72MHz;
2018.10.10	1.2	Revise the maximum value of f_{LSE_ext} in Table 18; revise the I_{DD} unit μA to mA in Table 26; Modify the minimum, typical, and maximum values for V_{25} in Table 47.
2018.10.15	1.3	Add sections on device comparison/ordering information/model designation, etc.
2020.03.17	1.4	Added package QFN36 related content