

The diagram illustrates the PC architecture for the RISC-V SoC, showing the interconnection of various components:

- 1 CPU:** The RISC-V CPU core, connected to the DDR memory and the AXI DMA.
- 2 MATLAB:** The MATLAB environment, connected to the JTAG AXI manager and the GUI interface.
- 3 JTAG AXI manager:** The JTAG AXI manager, connected to the MATLAB and the GUI interface.
- 4 Vecim:** The Vecim Vector coprocessor, connected to the Boundaryscan and the Mock DRAM interconnect.
- Boundaryscan:** The Boundaryscan interface, connected to the Mock DRAM interconnect and the Test chip.
- Mock DRAM interconnect:** The Mock DRAM interconnect, connected to the Boundaryscan and the Test chip.
- Test chip:** The Test chip, connected to the Mock DRAM interconnect and the PowerSupply.
- PowerSupply:** The PowerSupply, connected to the Test chip and the VSS.
- VSS:** The VSS (Ground) connection, connected to the PowerSupply and the Test chip.
- DDR:** The DDR memory, connected to the CPU and the AXI DMA.
- AXI DMA:** The AXI DMA controller, connected to the CPU and the MATLAB.
- JTAG UART:** The JTAG UART interface, connected to the MATLAB and the GUI interface.
- GUI interface:** The GUI interface, connected to the MATLAB and the JTAG AXI manager.