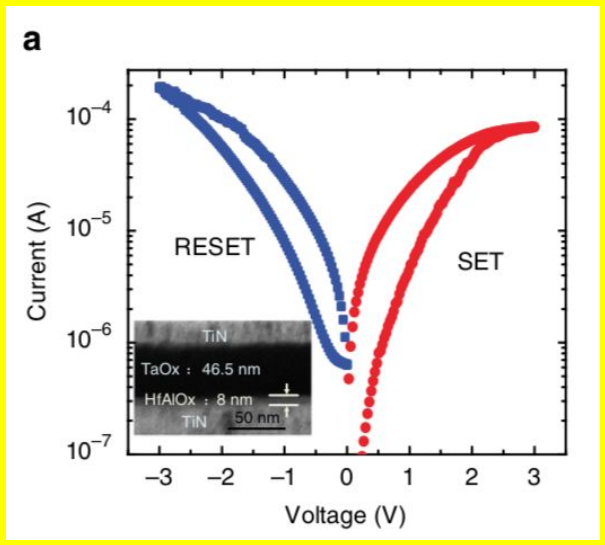
1. General Questions
    a. What is the typical I-V characteristic of a RRAM device? Try to sketch its I-V curve to show your idea.
        i. (Hint: Refer to the research of Leon Chua, regarded as the father of memristor.)
        ii. The I-V characteristic of a RRAM device is smooth and symmetrical between the SET and RESET processes
        iii. 

    b. What are the advantages of RRAM as electronic synapses? And what are the drawbacks?
        i. (Hint: An electronic synapse is used as the connector between pre-neuron and post-neuron in artificial neural networks. You can compare RRAM synapses with classical electronic synapses, biological synapses on operation speed, energy consumption, area, reliability, scaling down, etc.)
        ii. Advantages: Energy consumption is lower, saves area
        iii. Disadvantages: RRAM face a challenge of CMOS compatibility and cross-talk issues.
    c. What's the difference between unipolar RRAM and bipolar RRAM? Describe how they work respectively. Is the RRAM device mentioned in [Yao et al., 2017] unipolar or bipolar?
        i. Bipolar allows electricity to flow both ways through the RRAM device.
            1. Saving area & energy
        ii. Unipolar allows electricity to flow only one way through the RRAM device.
        iii. The device mention is bipolar.
    d. What is the physical mechanism of the resistive switching process in general?
        i. (Hint: Refer to the "Introduction to RRAM" material I sent to you before, if necessary.)

ii. The polarization of the metal rods around the material in the middle of them either takes away from the bridge or gives more material to the bridge. (migration of oxygen under an electric field)

e. What is the SET and RESET process of a RRAM device?
   i. SET generation of oxygen vacancies and formation of a filament to increase resistivity
   ii. RESET oxidation of filament to allow decrease resistivity

f. What does ”1T1R” mean? And why we use ”1T1R” architecture?
   i. 1 Transistor and 1 Resistor
   ii. For high performance (speed)

2. Questions on the Article
   a. Why there is always an abrupt transition during the SET process? How does [Yao et al., 2017] overcome this difficulty?
      i. There’s an abrupt transition during the SET process because the generation or migration of a small number of oxygen vacancies in this region may induce a notable change of the conductance.
      ii. To overcome this difficulty, oxygen vacancy generation and electrical field/temperature should be effectively suppressed to avoid abrupt switching.
   b. What method does [Yao et al., 2017] use to reduce the variations of RRAM cells in a software way?
      i. The write-verify process is used.
   c. What is the RRAM array size in [Yao et al., 2017]? What is the original input image size? How to fix the mismatch?
      i. 1024 cells with 128 rows and 8 columns
      ii. 640 by 480 pixels (320 or a 20x16 size)
      iii. Which is cropped and down sampled
   d. What materials does [Yao et al., 2017] use for each layer of the RRAM stack? Point out the function of each layer.
      i. TiN/TaOx /HfAlyOx /TiN
      ii. HfAlyOx is the switching layer that laminate structure is leveraged to control the generation of oxygen vacancies and shows a better analogue performance than HfOx
      iii. TaOx capping layer that acts as an in-built current compliance layer and oxygen reservoir is deposited by physical vapour deposition method
      iv. TiN is fab-friendly
         1. TiN top electrode TiN/Al are deposited by reactive sputtering and electron beam evaporation
         2. TiN bottom electrode with atomic layer deposition

3. Fabrication Questions
   a. What is the fabrication workflow of the RRAM stack in [Yao et al., 2017]? Detailed fabricating parameters (temperature, thickness, etc.) are prefered.

i. The RRAM devices are formed on the drain of the transistors by using the following processes (Supplementary Fig. 2). The HfO2/Al2O3 multilayer structure is deposited on the TiN bottom electrode with atomic layer deposition method by repeating HfO2 and Al2O3 cycles at 200 °C periodically. For each period, three cycles of HfO2 and one cycles of Al2O3 are deposited. The thickness of one atomic layer deposition cycle of both HfO2 and Al2O3 is around 1 Å. The final thickness of the HfAlyOx layerisabout8nm.Then a 60nm TaOx capping layer that acts as an in-built current compliance layer and oxygen reservoir is deposited by physical vapour deposition method. The top electrode TiN/Al are deposited by reactive sputtering and electron beam evaporation, respectively. Finally, the top Al pad is patterned by dry etching with Cl2/BCl3 plasma.

b. How to control the ratio of different materials during deposition process?
   i. There are 3 cycles of adding HfO2 and Al2O3 adding up to 8nm
   ii. Then they use a TaOx capping layer of 60nm that acts as a built-in current compliance layer and oxygen reservoir which is deposited by a physical vapour deposition method