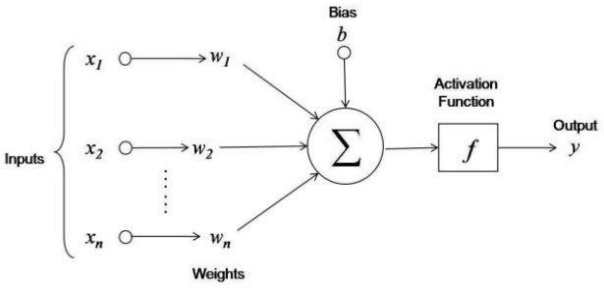
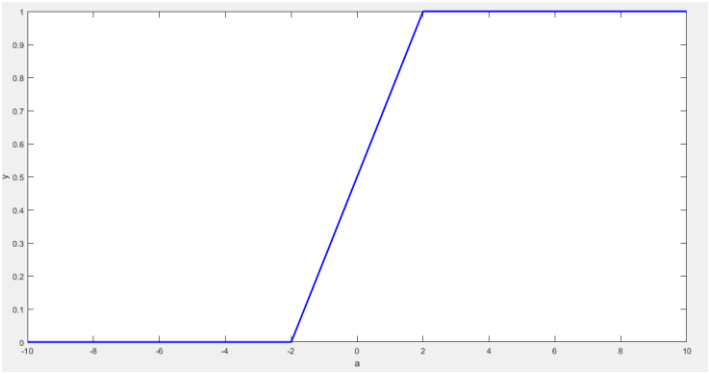
Perceptron

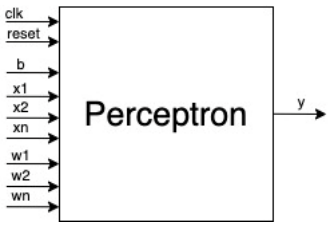
Design a digital circuit that realises a perceptron which takes $N_{IN} = 10$ inputs $x_n$represented with $b_x = 8$ bits. The network carries out the products between x_n and generic coefficients w_n and adds the result with a bias b. w_n and b are represented with $b_w = 9$ bits. x_n, w_n and b shall be considered in the range [-1,1] using fixed-point arithmetic. The output of the system shall be represented with $b_{out} = 16$ bits, truncating the least significant bits.



The activation function of the perceptron shall be the one represented in the next figure:



The interface of the circuit to be designed is as follows:



The interface may be modified depending on the architectural solution adopted to perform the operation within the perceptron. If this is the case, the reason must be stated in the final report.

Final report must presents:

- Introduction (algorithm description, possible applications, possible architectures, …)
- Architecture description (block diagram, I/O interface, etc.)
- VHDL code (with detailed comments)
- Test-plan and relevant Testbenches for the functional verification of the system

- Report the power consumption, the maximum clock frequency and the resource utilization on a Zync Xilinx FPGA. Explain possible logic synthesis warning messages
- Conclusion

Hint: The activation function can be realized without using a look-up table through a custom network which tests the amplitude of x and assigns the correct output y.