Jacques Benzly Te

(619) 648-7766 | jacquezte@gmail.com | San Diego, California, 92110
LinkedIn: https://www.linkedin.com/in/jacques-te | Website: https://jacquesbte.github.io/myportfolio

EDUCATION

University of San Diego Shiley-Marcos School of Engineering — **San Diego, CA**
BS/BA Electrical Engineering — Expected Graduation, Dec 2026
Minor in Math — Major GPA: 4.0 Overall GPA: 3.99

SKILLS

Programming & Firmware: Python, C/C++, Verilog, MATLAB.
Hardware & Digital Design: FPGA (AMD Vivado, Basys 3), STM32 (Nucleo-L476RG), ESP32, UART/SPI/I2C, PCB Design (NI Ultiboard, Multisim)
EDA & Tools: AutoCAD, SolidWorks, Lab Instrumentation (Oscilloscopes, function generators), soldering
Machine Learning & Edge AI: TensorFlow Lite, Edge Impulse, TinyML, IoT (Make.com, API/ Webhooks)

ENGINEERING PROJECTS AND EXPERIENCE

Wake Word Detection on STM32 Nucleo-L476RG | TinyML Project

- Built a **real-time wake word detection system** on STM32 Nucleo-L476RG, achieving **>92% detection accuracy** under varied noise conditions.
- Trained and optimized a TensorFlow Lite model with MFCC features and data augmentation, **cutting false activations by 35%** through hyperparameter tuning.
- Deployed model on embedded hardware with **<80KB memory footprint** and **sub-150ms latency**, ensuring responsiveness within MCU constraints.
- Delivered a complete pipeline from audio data collection to embedded deployment, demonstrating scalable **TinyML inference on low-power microcontrollers**.

Torero Space Program CubeSat Project | Communications & Data Subsystem Lead

- Led a team of 5 engineers to design the 1U CubeSat communications subsystem, enabling reliable two-way data transfer with the ground station.
- Integrated and programmed LoRa (RYLR896) modules with ESP32/Raspberry Pi firmware, achieving long-range telemetry within satellite power and timing constraints.
- Conducted lab signal range tests and implemented error-checked packet validation, boosting communication reliability by >95%.
- Configured ground and satellite modules with synchronized frequency and addressing, ensuring robust, interference-free operation for mission readiness.

Configurable Hardware Accelerator for Matrix Multiplication | FPGA Design Project

- Designed a **scalable NxN matrix multiplier** with pipelined MAC units, 6-state FSM, and triple-port memory for high-throughput computation.
- Implemented an **8×8 hardware accelerator** on Basys 3 (Artix-7 FPGA) with UART data loading, LED/7-segment display monitoring, and Python-driven real-time verification.
- Achieved **100 MHz operation performing 512 MACs per cycle**, enabling efficient parallelized matrix multiplication with dynamic data input.
- Optimized FPGA resource usage by leveraging **dual-port BRAM and registered MAC outputs**, extending design scalability up to block RAM limits while maintaining timing closure.

Fiber Optical Receiver Preamplifier Design | Analog Electronics Project

- Designed and implemented a **two-stage BJT preamplifier** (common-emitter + common-collector) for photodiode-based fiber-optic signal detection.
- Achieved a **–12.5 kΩ transresistance gain** (25% above requirement) while maintaining linear response and polarity control.
- Delivered a **clean output to 50 Ω load with <1% distortion** across 30–60 Ω range, verified through simulation and lab testing.

Jacques Benzly Te

(619) 648-7766 | jacquezte@gmail.com | San Diego, California, 92110
LinkedIn: https://www.linkedin.com/in/jacques-te | Website: https://jacquesbte.github.io/myportfolio

- Extended –3 dB bandwidth to **11.2 MHz (12% above spec)** and reduced output impedance from ~1 kΩ to ~100 Ω, improving power transfer efficiency by **600%**.

ML-Powered Finger Timer | Embedded Computer Vision Project
- Developed a **gesture-controlled timer** using ESP32 + 5MP camera, detecting 1–5 fingers with an Edge Impulse ML model.
- Implemented an **OLED display with countdown logic**, providing hands-free timing for cooking, workouts, or task management.
- Trained and tested custom datasets across lighting/angles, reaching **95%+ recognition accuracy** and reliable **real-time countdown execution**.

TradingView ESP32 Alert Notifier | IoT Project
- Built an **ESP32-based real-time notifier** to display and sound alerts from TradingView via Make.com webhooks.
- Integrated **0.96″ OLED, buzzer, and button interface**, supporting multiple alert types (BUY/SELL/LONG/SHORT) with local history storage.
- Achieved **<1s latency** from cloud-to-device alerts, enabling traders to act quickly with **20+ alerts stored for review**.

Environmental Monitoring and Fan Control System | Embedded Systems Project
- Built a **temperature-controlled system** on STM32 Nucleo-L476RG with ADC-based sensing (TMP36) and PWM-driven fan control.
- Programmed low-level C drivers for I²C OLED display, delivering **real-time feedback** on temperature and fan speed with minimal firmware overhead.
- Validated system in live tests, achieving **responsive PWM adjustments** to thermal changes and added a **watchdog timer** for fault recovery, improving overall reliability.

VHDL Event Counter | Digital Design Project
- Designed and implemented an **event counter in VHDL** on the Basys 3 FPGA to track falling edges of an input signal.
- Integrated **button-controlled inputs** and displayed counts on a **7-segment display**, ensuring clear real-time visualization.
- Validated accurate edge detection over **1-second measurement intervals**, making the design suitable for broader signal-processing applications.

AFFILIATIONS

IEEE, ASME, SASE, Tau Beta Pi (Engineering Honor Society), USD Torero Space Program, Filipino Ugnayan Student Org.