

Jacques Benzly Te

(619) 648-7766 | jacquezte@gmail.com | San Diego, California, 92110

Linked In: <https://www.linkedin.com/in/jacques-te/>.

EDUCATION

University of San Diego Shiley-Marcos School of Engineering

BS/BA Electrical Engineering

Minor in Math

San Diego, CA

Expected Graduation, Dec 2026

Major GPA: 4.0 Overall GPA: 3.99

SKILLS

Software: NI Multisim, NI Ultiboard (PCB design software), AutoCAD, SolidWorks, Programming language (Python, C), Arduino IDE, MATLAB, Vivado, Excel, TensorFlow, IoT, Verilog and VHDL.

Technical: Oscilloscope, Function generators, Soldering, Circuit Design and Analysis, Power Systems Analysis, FPGA, Embedded systems and VLSI.

ENGINEERING PROJECTS AND EXPERIENCE

AI-Enabled Edge Device Development

Wake Word Detection on STM32 Nucleo-L476RG | personal project

- Designed and implemented a **real-time wake word detection system** on an **STM32 Nucleo-L476RG**.
- Developed and trained a **deep learning model** for wake word detection using **TensorFlow** leveraging **MFCC feature extraction** and data augmentation techniques for improved accuracy.
- Optimized machine learning models for deployment on **low-power embedded hardware**.
- Resolved overfitting issues through **architectural tuning, hyperparameter optimization**, and enhanced **data augmentation**.
- Utilized **TensorFlow Lite for Microcontrollers** to train and test wake word models.
- Integrated **signal processing techniques** to preprocess audio inputs effectively.
- Successfully implemented **edge inference** with **efficient power consumption** and **memory usage**.
- Developed a **robust pipeline** from data acquisition to model deployment and validation.

Torerro Space Program CubeSat Project | Ongoing Cube Satellite Project

- Lead a **team of five engineers** in designing and implementing the **Communications and Data Subsystem** for a 1U CubeSat Mission.
- Designed the CubeSat's **communication architecture** to enable two-way data transmission between the satellite and the ground station.
- Integrated **LoRa modules (RYLR896)** for low-power, long range telemetry and command data transmission, leveraging UART AT-command protocol.
- Developed and tested **Raspberry PI and ESP32 based transmitter and receiver firmware** to interface with the LoRa modules, ensuring compatibility with satellite power and timing constraints.
- Conducted **Lab-based signal range testing** and implemented data packet validation strategies to increase communication reliability.
- Configured satellite-side and ground-side modules for synchronized frequency, network ID, and device addressing to prevent signal interference.

Fiber Optical Receiver Preamplifier Design | Analog Electronics Design Project

- Designed and implemented a two-stage BJT-based preamplifier (Common-Emitter + Common-Collector) using BC107BP transistors for fiber-optic signal detection from a photodiode source.
- Achieved a **transresistance gain of $-12.5\text{ k}\Omega$** , exceeding the required minimum by **25%**, while maintaining polarity inversion and linear response.
- Successfully delivered clean signal output to a **50Ω load**, validated over the specified 30–60 Ω range with <1% distortion.
- Simulated and verified amplifier performance with a **-3 dB bandwidth of 11.2 MHz**, exceeding the 10 MHz baseband requirement by **12%** to ensure full signal fidelity.
- Reduced output impedance from $\sim 1\text{ k}\Omega$ to $\sim 100\text{ }\Omega$ via a Common-Collector buffer stage, resulting in a **600% improvement in power transfer and load matching efficiency** compared to a single stage design.

Jacques Benzly Te

(619) 648-7766 | jacquezte@gmail.com | San Diego, California, 92110

Linked In: <https://www.linkedin.com/in/jacques-te/>.

Configurable Hardware Accelerator for Matrix Multiplication | FPGA Design Project

- Designed scalable NxN matrix multiplier with parametrized RTL architecture: pipelined MAC units, 6-state FSM, triple-port memory, configurable matrix size.
- Implemented on 8x8 matrix on the Basys 3 development board utilizing **Artix-7 FPGA resources**: USB-UART interface for real-time data loading, 16 LEDs for status monitoring, 4-digit 7-segment display for results, 5 pushbuttons for control.
- Achieved 100MHz operation performing **512 MAC operations/cycle (8x8)**, **UART dynamic data loading** (115200 baud), **Python test automation** with real-time monitoring and verification.
- Optimized resource utilization through **dual-port BRAM** for parallel operand fetching, registered MAC outputs for **timing closure**, and efficient address generation logic supporting matrix operations up to available block RAM capacity.

Environmental Monitoring and Fan Control System | Embedded Systems Project

- Developed a **temperature-controlled embedded system** on **STM32 Nucleo-L476RG** using a **TMP36 analog sensor**, with real-time **ADC-based temperature monitoring** and **PWM-driven fan control**.
- Utilized an **SSD1306 I2C OLED display** for real-time feedback on temperature and fan speed, powered by **custom low-level C modules** and a **lightweight, timing-efficient firmware structure**.
- Validated **system responsiveness** by correlating thermal variations with **dynamic PWM duty cycle** adjustments during live testing.
- Integrated a **hardware watchdog timer** to enhance reliability by detecting and recovering from **software faults or peripheral failures**

VHDL Event Counter Project | Digital Design Project

- Developed an event counter using VHDL on an Artix-3 Basys Board, displaying the count on a seven segment display.
- Implemented a button-controlled system that counts falling edges in a voltage signal over a one-second period.
- Designed for easy integration into broader signal processing applications.

Quantitative research assistant in high school

- Assisted in collecting and analyzing various data from surveys and secondary data.
- Utilized statistical analysis: Correlation, Linear Regression, and Logistic Regression to determine relationships between variables of interest.
- Used Excel to generate visual figures to visualize and describe data.

AFFILIATIONS

USD Institute of Electrical and Electronics Engineers (IEEE)

USD American Society of Mechanical Engineers (ASME)

USD Society of Asian Scientists and Engineers (SASE)

USD Filipino Ugnayan Student Org. (FUSO)

USD Tau Beta Pi (Engineering Honors Society)

USD Torrero Space Program

Fall 2022 - Present

Fall 2022 - Present

Spring 2024 - Present

Fall 2022 - Present

Fall 2024 - Present

Spring 2025 - Present