Jacques Benzly Te

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EDUCATION

University of San Diego Shiley-Marcos School of Engineering — **San Diego, CA**
BS/BA Electrical Engineering — Expected Graduation, Dec 2026
Minor in Math — Major GPA: 4.0 Overall GPA: 3.99

SKILLS

Programming & Firmware: Python, C/C++, Verilog, MATLAB, RoboDK, KUKA Robot Language.
Hardware & Digital Design: FPGA (AMD Vivado, Basys 3), STM32 (Nucleo-L476RG), ESP32, UART/SPI/I2C, PCB Design (NI Ultiboard, Multisim), NVDIA Jetson Orin Nano (Edge AI Inference).
Analog & RF Design: Circuit Design & Analysis, Signal Conditioning, Power Systems, PCB Design (NI Ultiboard, Multisim), Transmission line design, impedance matching, Keysight ADS.
EDA & Tools: AutoCAD, SolidWorks, Lab Instrumentation (Oscilloscopes, function generators), soldering
Machine Learning & Edge AI: TensorFlow Lite, Edge Impulse, TinyML, IoT (Make.com, API/ Webhooks).

ENGINEERING PROJECTS AND EXPERIENCE

Wake Word Detection on STM32 Nucleo-L476RG | TinyML Project

- Built a **real-time wake word detection system** achieving **>92% accuracy** under varied noise conditions.
- Trained and optimized a **TensorFlow Lite model with MFCC features**, reducing false activations by **35%**
- Deployed model on embedded hardware with **<80KB memory footprint** and **sub-150ms latency**, ensuring responsiveness within MCU constraints.
- Deployed the model on STM32 with **<80 KB memory** and **<150 ms latency**, demonstrating efficient **TinyML inference** on low-power MCUs.

Torero Space Program CubeSat Project | Communications & Data Subsystem Lead

- **Led** a 5-member team to design and validate the 1U CubeSat communications subsystem, achieving >95% reliable two-way telemetry between the satellite and ground station.
- Integrated and programmed LoRa (RYLR896) modules with ESP32/Raspberry Pi firmware, **optimizing frequency, addressing,** and **power for long-range**, interference-free operation.

Performant Manufacturing | Automated Robotic Microfluidic Chip Assembly Cell **|** Ongoing Capstone Project

- Lead the **electrical subsystem** and **robot programming** for a **KUKA robotic arm** automating **microfluidic chip** assembly through **precision gluing, pick-and-place, and UV** curing operations.
- Designed and programmed robot motion paths in **RoboDK**; built and tested **24 V to 5 V interface circuits** and **ESP32-based control** for the vacuum-suction pick-and-place end effector and gluing system.

Configurable Hardware Accelerator for Matrix Multiplication | FPGA Design Project

- Designed a **scalable NxN matrix multiplier** with pipelined MAC units, 6-state FSM, and triple-port memory for high-throughput computation.
- Implemented an **8×8 hardware accelerator** on Basys 3 (Artix-7 FPGA) with UART data loading, LED/7-segment display monitoring, and Python-driven real-time verification.
- Achieved **100 MHz operation performing 512 MACs per cycle**, enabling efficient parallelized matrix multiplication with dynamic data input.
- Optimized FPGA resource usage by leveraging **dual-port BRAM and registered MAC outputs**, extending design scalability up to block RAM limits while maintaining timing closure.

Fiber Optical Receiver Preamplifier Design | Analog Electronics Project

- Designed **a two-stage BJT preamplifier** (common-emitter + common-collector) for **photodiode-based fiber-optic detection**.
- A Achieved **–12.5 kΩ transresistance** gain (**25% above target**) with **linear response** and **polarity control**.
- Delivered **<1% distortion** to a 50 Ω load across 30–60 Ω range, extending –3 dB bandwidth to 11.2 MHz and reducing output impedance from **~1 kΩ to ~100 Ω** (**600% power transfer improvement**).

AFFILIATIONS: IEEE, ASME, SASE, Tau Beta Pi (Honor Society), USD Torero Space Program, FUSO