Jacques Benzly Te

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EDUCATION

University of San Diego Shiley-Marcos School of Engineering **San Diego, CA**
BS/BA Electrical Engineering Expected Graduation, Dec 2026
Minor in Math Major GPA: 4.0 Overall GPA: 3.99

SKILLS

Software: NI Multisim, NI Ultiboard (PCB design software), AutoCAD, SolidWorks, Programming language (Python, C), Arduino IDE, MATLAB, Vivado, Excel, TensorFlow, IoT, Verilog and VHDL.
Technical: Oscilloscope, Function generators, Soldering, Circuit Design and Analysis, Power Systems Analysis, FPGA, Embedded systems and VLSI.

ENGINEERING PROJECTS AND EXPERIENCE

AI-Enabled Edge Device Development
Wake Word Detection on STM32 Nucleo-L476RG | personal project

- Designed and implemented a **real-time wake word detection system** on an **STM32 Nucleo-L476RG**.
- Developed and trained a **deep learning model** for wake word detection using **TensorFlow** leveraging **MFCC feature extraction** and data augmentation techniques for improved accuracy.
- Optimized machine learning models for deployment on **low-power embedded hardware**.
- Resolved overfitting issues through **architectural tuning, hyperparameter optimization**, and enhanced **data augmentation**.
- Utilized **TensorFlow Lite for Microcontrollers** to train and test wake word models.
- Integrated **signal processing techniques** to preprocess audio inputs effectively.
- Successfully implemented **edge inference** with **efficient power consumptio**n and **memory usage.**
- Developed a **robust pipeline** from data acquisition to model deployment and validation.

Torerro Space Program CubeSat Project | Ongoing Cube Satellite Project

- Lead a **team of five engineers** in designing and implementing the **Communications and Data Subsystem** for a 1U CubeSat Mission.
- Designed the CubeSat's **communication architecture** to enable two-way data transmission between the satellite and the ground station.
- Integrated **LoRa modules (RYLR896)** for low-power, long range telemetry and command data transmission, leveraging UART AT-command protocol.
- Developed and tested **Raspberry PI and ESP32 based transmitter and receiver firmware** to interface with the LoRa modules, ensuring compatibility with satellite power and timing constraints.
- Conducted **Lab-based signal range testing** and implemented data packet validation strategies to increase communication reliability.
- Configured satellite-side and ground-side modules for synchronized frequency, network ID, and device addressing to prevent signal interference.

Fiber Optical Receiver Preamplifier Design | Analog Electronics Design Project

- Designed and implemented a two-stage BJT-based preamplifier (Common-Emitter + Common-Collector) using BC107BP transistors for fiber-optic signal detection from a photodiode source.
- Achieved a **transresistance gain of –12.5 kΩ**, exceeding the required minimum by **25%**, while maintaining polarity inversion and linear response.
- Successfully delivered clean signal output to a **50Ω load**, validated over the specified 30–60Ω range with <1% distortion.
- Simulated and verified amplifier performance with a **–3 dB bandwidth of 11.2 MHz**, exceeding the 10 MHz baseband requirement by **12%** to ensure full signal fidelity.
- Reduced output impedance from ~1 kΩ to ~100 Ω via a Common-Collector buffer stage, resulting in a **600% improvement in power transfer and load matching efficiency** compared to a single stage design.

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Environmental Monitoring and Fan Control System | Embedded Systems Project

- Developed a **temperature-controlled embedded system** on **STM32 Nucleo-L476RG** using a **TMP36 analog sensor**, with real-time **ADC-based temperature monitoring** and **PWM-driven fan control**.
- Utilized an **SSD1306 I2C OLED display** for real-time feedback on temperature and fan speed, powered by **custom low-level C modules** and a **lightweight, timing-efficient firmware structure**.
- Validated **system responsiveness** by correlating thermal variations with **dynamic PWM duty cycle** adjustments during live testing.
- Integrated a **hardware watchdog timer** to enhance reliability by detecting and recovering from **software faults or peripheral failures**

VHDL Event Counter Project | Digital Design Project

- Developed an event counter using VHDL on an Artix-3 Basys Board, displaying the count on a seven segment display.
- Implemented a button-controlled system that counts falling edges in a voltage signal over a one-second period.
- Designed for easy integration into broader signal processing applications.

Quantitative research assistant in high school

- Assisted in collecting and analyzing various data from surveys and secondary data.
- Utilized statistical analysis: Correlation, Linear Regression, and Logistic Regression to determine relationships between variables of interest.
- Used Excel to generate visual figures to visualize and describe data.

AFFILIATIONS

USD Institute of Electrical and Electronics Engineers (IEEE) **Fall 2022 - Present**
USD American Society of Mechanical Engineers (ASME) **Fall 2022 - Present**
USD Society of Asian Scientists and Engineers (SASE) **Spring 2024 - Present**
USD Filipino Ugnayan Student Org. (FUSO) **Fall 2022 - Present**
USD Tau Beta Pi (Engineering Honors Society) **Fall 2024 - Present**
USD Torrero Space Program **Spring 2025 - Present**