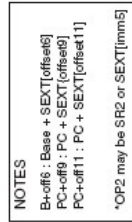


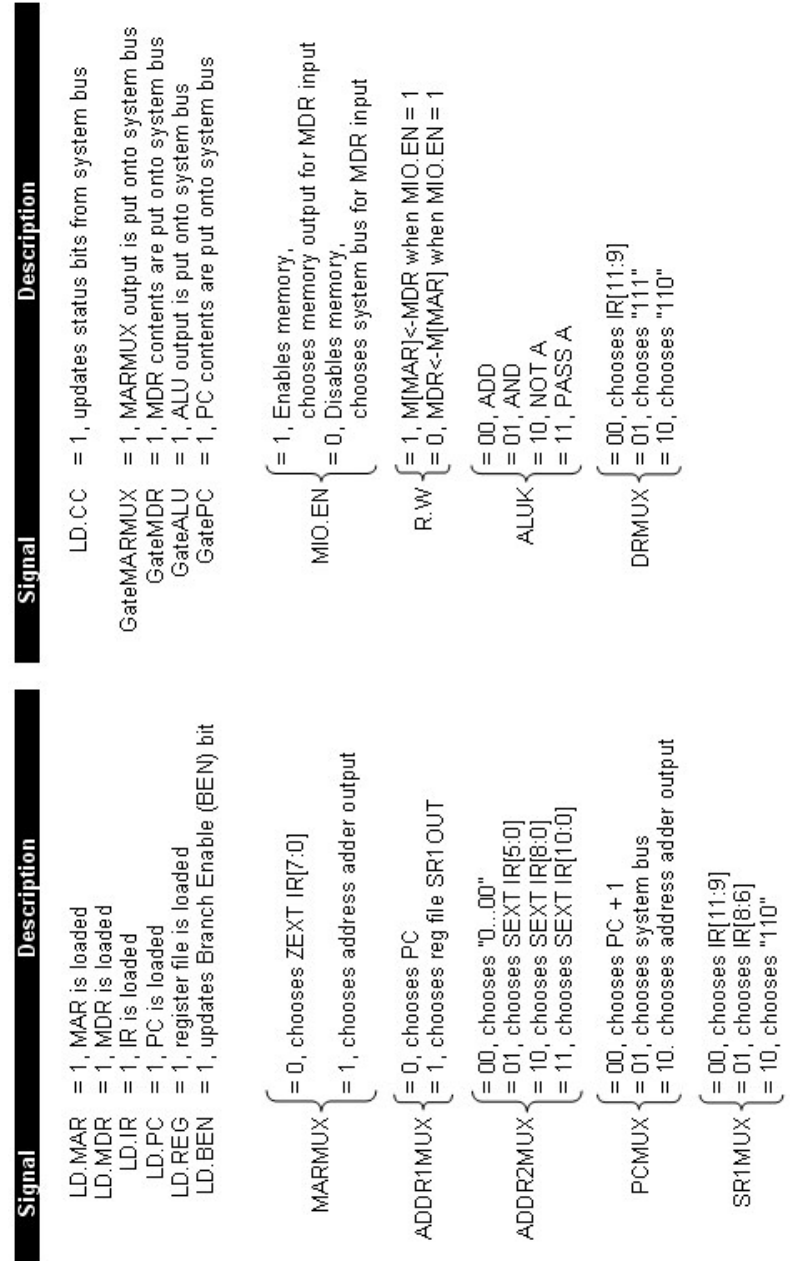
## LC-3 Instructions



NOTES: RTL corresponds to execution (after fetch!); JSRR not shown

ADD	0001	DR	SR1	0	00	SR2	ADD DR, SR1, SR2	LD	0010	DR	PCOffset9					LD DR, PCOffset9
$DR \leftarrow SR1 + SR2, Setcc$								$DR \leftarrow M[PC + SEXT(PCOffset9)], Setcc$								
ADD	0001	DR	SR1	1	imm5		ADD DR, SR1, imm5	LDI	1010	DR	PCOffset9					LDI DR, PCOffset9
$DR \leftarrow SR1 + SEXT(imm5), Setcc$								$DR \leftarrow M[M[PC + SEXT(PCOffset9)]], Setcc$								
AND	0101	DR	SR1	0	00	SR2	AND DR, SR1, SR2	LDR	0110	DR	BaseR	offset6				LDR DR, BaseR, offset6
$DR \leftarrow SR1 \text{ AND } SR2, Setcc$								$DR \leftarrow M[BaseR + SEXT(offset6)], Setcc$								
AND	0101	DR	SR1	1	imm5		AND DR, SR1, imm5	LEA	1110	DR	PCOffset9					LEA DR, PCOffset9
$DR \leftarrow SR1 \text{ AND } SEXT(imm5), Setcc$								$DR \leftarrow PC + SEXT(PCOffset9), Setcc$								
BR	0000	n	z	p	PCOffset9		BR{nzp} PCOffset9	NOT	1001	DR	SR	111111				NOT DR, SR
$((n \text{ AND } N) \text{ OR } (z \text{ AND } Z) \text{ OR } (p \text{ AND } P)):$ $PC \leftarrow PC + SEXT(PCOffset9)$								$DR \leftarrow \text{NOT } SR, Setcc$								
JMP	1100	000	BaseR	000000			JMP BaseR	ST	0011	SR	PCOffset9					ST SR, PCOffset9
$PC \leftarrow BaseR$								$M[PC + SEXT(PCOffset9)] \leftarrow SR$								
JSR	0100	1	PCOffset11				JSR PCOffset11	STI	1011	SR	PCOffset9					STI SR, PCOffset9
$R7 \leftarrow PC, PC \leftarrow PC + SEXT(PCOffset11)$								$M[M[PC + SEXT(PCOffset9)]] \leftarrow SR$								
TRAP	1111	0000	trapvect8				TRAP trapvect8	STR	0111	SR	BaseR	offset6				STR SR, BaseR, offset6
$R7 \leftarrow PC, PC \leftarrow M[ZEXT(trapvect8)]$								$M[BaseR + SEXT(offset6)] \leftarrow SR$								

## LC-3 Datapath Control Signals



Signal	Description	Signal	Description
LD.MAR	= 1, MAR is loaded	LD.CC	= 1, updates status bits from system bus
LD.MDR	= 1, MDR is loaded	GateMARMUX	= 1, MARMUX output is put onto system bus
LD.IR	= 1, IR is loaded	GateMDR	= 1, MDR contents are put onto system bus
LD.PC	= 1, PC is loaded	GateALU	= 1, ALU output is put onto system bus
LD.REG	= 1, register file is loaded	GatePC	= 1, PC contents are put onto system bus
LD.BEN	= 1, updates Branch Enable (BEN) bit		
MARMUX	$\begin{cases} = 0, \text{ chooses ZEXT IR}[7:0] \\ = 1, \text{ chooses address adder output} \end{cases}$	MIO.EN	$\begin{cases} = 1, \text{ Enables memory,} \\ \quad \text{chooses memory output for MDR input} \\ = 0, \text{ Disables memory,} \\ \quad \text{chooses system bus for MDR input} \end{cases}$
ADDR1MUX	$\begin{cases} = 0, \text{ chooses PC} \\ = 1, \text{ chooses reg file SR1 OUT} \end{cases}$	R.W	$\begin{cases} = 1, \text{ MIMAR} \leftarrow \text{MDR when MIO.EN} = 1 \\ = 0, \text{ MDR} \leftarrow \text{MIMAR when MIO.EN} = 1 \end{cases}$
ADDR2MUX	$\begin{cases} = 00, \text{ chooses "0...00"} \\ = 01, \text{ chooses SEXT IR}[5:0] \\ = 10, \text{ chooses SEXT IR}[8:0] \\ = 11, \text{ chooses SEXT IR}[10:0] \end{cases}$	ALUK	$\begin{cases} = 00, \text{ ADD} \\ = 01, \text{ AND} \\ = 10, \text{ NOT A} \\ = 11, \text{ PASS A} \end{cases}$
PCMUX	$\begin{cases} = 00, \text{ chooses PC} + 1 \\ = 01, \text{ chooses system bus} \\ = 10, \text{ chooses address adder output} \end{cases}$	DRMUX	$\begin{cases} = 00, \text{ chooses IR}[11:9] \\ = 01, \text{ chooses "11"} \\ = 10, \text{ chooses "10"} \end{cases}$
SR1MUX	$\begin{cases} = 00, \text{ chooses IR}[11:9] \\ = 01, \text{ chooses IR}[8:6] \\ = 10, \text{ chooses "10"} \end{cases}$		