



SAM R34/R35 64-PIN

SAM R34/R35 LoRa[®] Technology SoC Summary

Introduction

The SAM R34/R35 is a family of ultra-low-power microcontrollers integrated with a RF transceiver communications interface, using the 32-bit ARM[®] Cortex[®] -M0+ processor with up to 256 KB Flash and 40 KB of SRAM, including an area of battery backed-up SRAM. The integrated sub-GHz transceiver supports LoRa[®] Technology spread spectrum modulation, combining ultra-long range communications and high interference immunity with extremely low-current consumption.

Operational Features

- Processor:
 - ARM[®] Cortex[®] -M0+ CPU running at up to 48 MHz (2.46 CoreMark[®]/MHz)
 - Single-Cycle Hardware Multiplier
 - Micro Trace Buffer (MTB)
- Memory:
 - In-System Self-Programmable Flash Memory, with options for sizes - 256 KB, 128 KB or 64 KB
 - Static Random Access Memory (SRAM) with options for sizes - 32 KB, 16 KB or 8 KB
 - 8 KB low-power RAM with battery backup retention (with 4 KB option)
- System:
 - Power-on Reset (POR) and Brown-out Reset
 - Internal and External Clock Options with 48 MHz Digital Frequency Locked Loop (DFLL48M) and 48 MHz to 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)
 - External Interrupt Controller (EIC)
 - Up to 15 External Interrupts
 - One Non-Maskable Interrupt
 - Two-Pin Serial Wire Debug (SWD) Programming, Test and Debugging Interfaces
- Operating Voltage: 1.8V- 3.6V
- Low-Power Consumption
 - Transceiver:
 - RX_ON = 9.9 to 14.2 mA
 - TX_ON = up to 39 mA at 14 dBm
 - TX_ON = up to 124 mA at +20 dBm
 - MCU:
 - Idle and Standby Sleep Modes
 - SleepWalking Peripherals
 - Down to 701 uA/MHz in Active Mode
- Temperature Range: -40°C to +85°C (Industrial)

RF/Analog Features

- Integrated LoRa[®] Technology Transceiver:
 - 137 to 1020 MHz Frequency Band Coverage
 - +20 dBm (100 mW) High-Power PA, Constant RF Output vs. Supply Voltage
 - +14 dBm (25 mW) High-Efficiency Power Amplifier (PA)
- High Sensitivity:
 - Down to -136 dBm (LoRaWAN[™] protocol compliant modes)
 - Down to -148 dBm (proprietary narrowband modes)

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- Up to 168 dB Maximum Link Budget
- Bullet-Proof Front End: IIP3 = -11 dBm
- Excellent Blocking Immunity
- Low RX Current of 9.9 mA
- Fully Integrated Synthesizer with a Resolution of 61 Hz
- LoRa Technology, (G)FSK, (G)MSK and OOK Modulation
- Built-In Bit Synchronizer for Clock Recovery
- Preamble Detection
- 127 dB Dynamic Range RSSI
- Automatic RF Sense and CAD with Ultra-Fast Automatic Frequency Control (AFC) Packet Engine up to 256 bytes with Cyclic Redundancy Check (CRC)

Peripherals

- 12-Channel Direct Memory Access Controller (DMAC)
- 12-Channel Event System
- Three 16-bit Timer/Counters (TC), configurable as either:
 - One 8-bit TC with compare/capture channels
 - One 16-bit TC with compare/capture channels
 - One 32-bit TC with compare/capture channels, by using two TCs
- Three 16-bit Timer/Counters for Control (TCC), with Extended Functions:
 - Up to four compare channels with optional complementary output
 - Generation of synchronized Pulse Width Modulation (PWM) pattern across port pins
 - Deterministic fault protection, fast decay and configurable dead-time between complementary output
 - Dithering that increases resolution with up to five bit and reduces quantization error
- 32-bit Real Time Counter (RTC) with Clock/Calendar Function
- Watchdog Timer (WDT)
- CRC-32 Generator
- One Full-Speed (12 Mbps) Universal Serial Bus (USB) 2.0 Interface:
 - Embedded host and device function
 - Eight endpoints
- Up to Five Serial Communication Interfaces (SERCOM), each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I²C up to 3.4 MHz
 - Serial Peripheral Interface (SPI)
 - Local Interconnect Network (LIN) Slave
- One 12-bit, 350 kps Analog-to-Digital Converter (ADC) with up to Eight External Channels:
 - Differential and single-ended input
 - 1/2x to 16x programmable gain stage
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
- Two Analog Comparators (AC) with Window Compare Function
- Peripheral Touch Controller (PTC):
 - 48-channel capacitive touch and proximity sensing

I/O and Package

- 27 Programmable I/O Pins
- 64-Lead Ball Grid Array (BGA)

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NOTES:

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1.0 CONFIGURATION SUMMARY

TABLE 1-1: CONFIGURATION SUMMARY

	SAM R34J	SAM R35J
Pins	64	
General Purpose I/O pins (GPIOs)	27	
Flash	up to 256 KB (See Table 2-1 and Table 2-2)	
Flash RWW section	8 KB	
System SRAM	up to 32 KB (See Table 2-1 and Table 2-2)	
Low-Power SRAM	up to 8 KB (See Table 2-1 and Table 2-2)	
Timer Counter (TC) instances	3	
Waveform output channels per TC instance	2	
Timer Counter for Control (TCC) instances	3	
Waveform output channels per TCC	4/2/2	
USB interface	1	0
Serial Communication Interface (SERCOM) instances	5+1(1)	
Inter-IC Sound (I ² S) interface	No	
Analog-to-Digital Converter (ADC) channels	8	
Analog Comparators (AC)	2	
Digital-to-Analog Converter (DAC) channels	No	
Real-Time Counter (RTC)	Yes	
RTC alarms	1	
RTC compare values	One 32-bit value or two 16-bit values	
External Interrupt lines	15	
Peripheral Touch Controller (PTC) X and Y lines	8x6	
Maximum CPU frequency	48 MHz	
Packages	BGA	
Oscillators	16 MHz crystal oscillator for TRX (XOSCRF) 0.4-32 MHz crystal oscillator (XOSC) 32.768 kHz internal oscillator (OSC32K) 32.768 kHz crystal oscillator (XOSC32K) 32 kHz ultra-low-power internal oscillator (OSCULP32K) 8 MHz high-accuracy internal oscillator (OSC8M) 48 MHz Digital Frequency Locked Loop (DFLL48M) 96 MHz Fractional Digital Phased Locked Loop (FDPLL96)	
Event System channels	12	
SW Debug Interface	Yes	
Watchdog Timer (WDT)	Yes	

Note 1: SERCOM4 is internally connected to the LoRa[®] technology transceiver.

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2.0 ORDERING INFORMATION

ATSAMR 34 J 18 B T - I / 7JX

Product Family

SAMR = SoC Microcontroller with RF

Product Series

34 = Cortex M0+ CPU + DMA + USB + LoRa Radio
35 = Cortex M0+ CPU + DMA + LoRa Radio

Pin Count

J = 64 Pins

Flash Memory Density

16 = 64 KB
17 = 128 KB
18 = 256 KB

Device Variant

B = Hardware Revision

Package Type

7JX = 64 Ball, 6x6mm TFBGA

Temperature Rating

I = -40 to +85C

Package Carrier

T = Tape and Reel

2.1 SAM R34J

TABLE 2-1: SAM R34J ORDERING CODES

Ordering Code	FLASH (bytes)	SRAM (bytes)	Low-PowerSRAM (bytes)	USB	Package	Carrier Type
ATSAMR34J16AT-I/7JX	64K	8K	4K	1	BGA-64	Tape & Reel
ATSAMR34J17AT-I/7JX	128K	16K	8K	1	BGA-64	Tape & Reel
ATSAMR34J18AT-I/7JX	256K	32K	8K	1	BGA-64	Tape & Reel
ATSAMR34J16A-I/7JX	64K	8K	4K	1	BGA-64	Tray
ATSAMR34J17A-I/7JX	128K	16K	8K	1	BGA-64	Tray
ATSAMR34J18A-I/7JX	256K	32K	8K	1	BGA-64	Tray

2.2 SAM R35J

TABLE 2-2: SAM R35J ORDERING CODES

Ordering Code	FLASH (bytes)	SRAM (bytes)	Low-PowerSRAM (bytes)	USB	Package	Carrier Type
ATSAMR35J16AT-I/7JX	64K	8K	4K	0	BGA-64	Tape & Reel
ATSAMR35J17AT-I/7JX	128K	16K	8K	0	BGA-64	Tape & Reel
ATSAMR35J18AT-I/7JX	256K	32K	8K	0	BGA-64	Tape & Reel
ATSAMR35J16A-I/7JX	64K	8K	4K	0	BGA-64	Tray
ATSAMR35J17A-I/7JX	128K	16K	8K	0	BGA-64	Tray
ATSAMR35J18A-I/7JX	256K	32K	8K	0	BGA-64	Tray

3.0 SYSTEM INTRODUCTION

3.1 Transceiver Circuit Description

Microchip SAM R34/R35 is a family of ultra-low-power microcontrollers integrated with an RF transceiver communications interface. The R34 and R35 are equipped with a LoRa technology compliant RF interface for long range communications with the worldwide sub-GHz frequency bands, in a highly integrated 6x6 mm 64-lead BGA package.

Using the 32-bit ARM Cortex M0+ processor core, this family of devices offer optimized memory configurations scalable up to 256 KB Flash and 40 KB of SRAM, including an area of battery backed-up SRAM. The sophisticated power management technologies, such as power domain gating, SleepWalking, ultra-low-power peripherals and more, allow for extremely low-current consumption in ultra-long battery life applications.

The integrated Sub-GHz transceiver supports LoRa technology spread spectrum modulation, combining ultra-long range communications and high interference immunity with extremely low-current consumption.

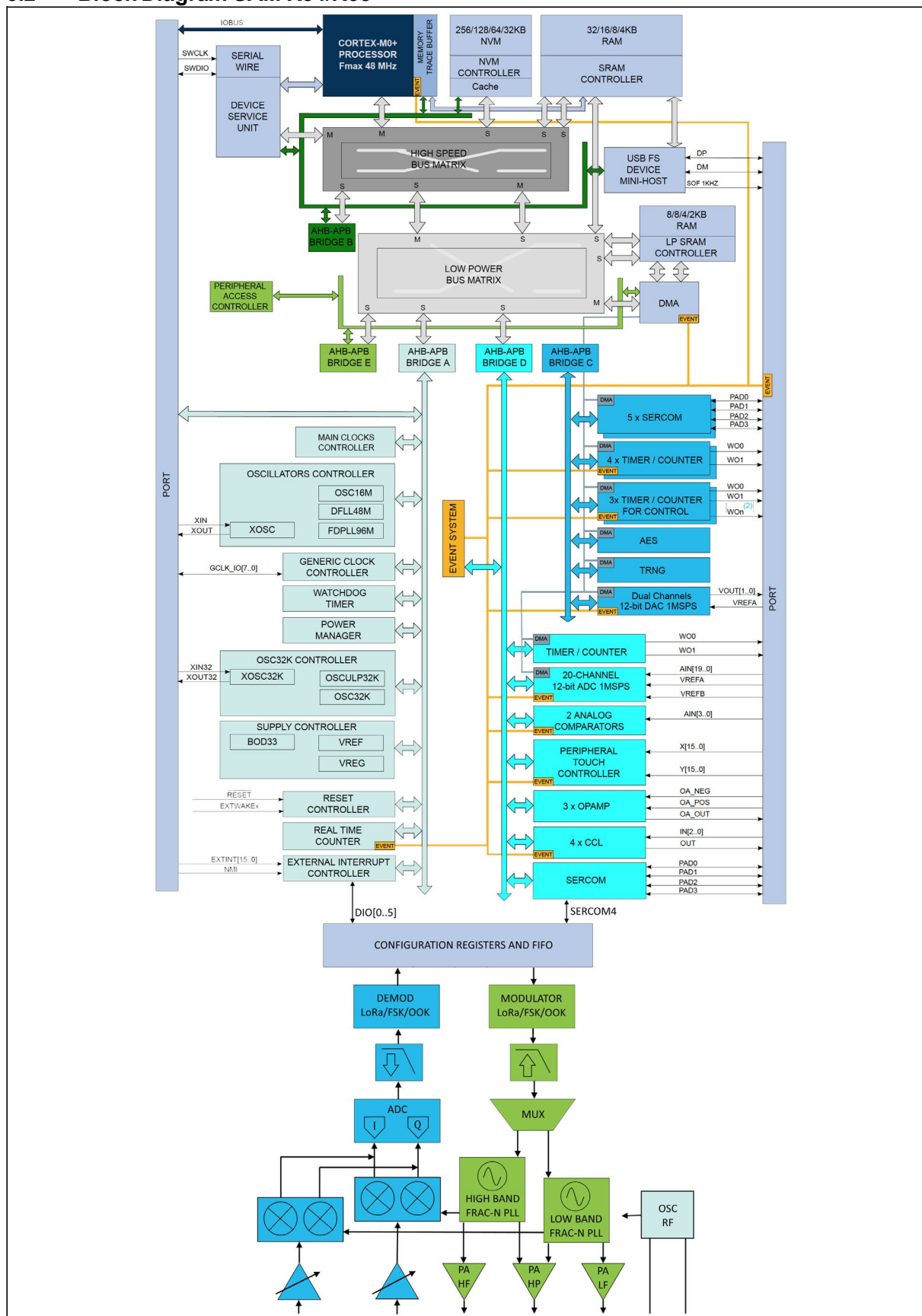
Receive sensitivities of over -148 dBm can be achieved in narrow-band modes, and -136 dBm in LoRaWAN protocol compliant modes, using a low-cost crystal and bill of materials.

The transmit section offers two integrated power amplifiers for both high efficiency with +14 dBm output power, or +20 dBm for highest power; depending on the regional regulations. This combination of high power and high RX sensitivity yields industry leading link budget, making it ideal for any application requiring long range low-data-rate communications. LoRa technology also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference robustness and energy consumption. For maximum flexibility the user may decide on the spread spectrum modulation bandwidth (BW), spreading factor (SF) and forward error correction rate (CR). Another benefit of the spread spectrum modulation is that each spreading factor is orthogonal – thus multiple transmitted signals can occupy the same channel without interfering.

R34 and R35 also support high performance (G)FSK, (G)MSK and OOK modes for systems including WMBus and IEEE802.15.4g.

This transceiver offers bandwidth options ranging from 7.8 kHz to 500 kHz with spreading factors ranging from 6 to 12, and covering all available frequency bands from 137 to 1020 MHz.

3.2 Block Diagram SAM R34/R35



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4.0 PINOUT

Note: Alpha device pinout. Subject to change.

4.1 BGA Diagram for SAM R34/R35

	1	2	3	4	5	6	7	8
A		GND_RF	PA00	PA01	VDDCORE	VSW	VDDIN	VDDIO2
B		GND_RF	GNDANA	PB02	GND	RESET	GND	PA24
C	VDDIN_RF	VDDANA	PB03	PA05	PA30	PA28	PB23	PA25
D	VRPA_RF	RXTX_RF	PA04	GND	PA31	GND	PA23	PA22
E	GND_RF	GNDANA	PA06	PA27	PB22	PA17	PA18	PA19
F		GND_RF	PA07	PA08	PA09	PA13	PA16	PA14
G		GND_RF	GND_RF	VDDI01	GND_RF	GND_RF	GND_RF	PA15
H		VRANA_RF	VDDANA_RF	VRDIG_RF	GND_RF	XTA	XTB	VDDDIG_RF

Legend:

- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- OSCILLATOR INPUT
- GROUND
- INPUT SUPPLY
- REGULATED INPUT/OUTPUT SUPPLY
- RESET PIN
- RF PIN

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5.0 SIGNAL DESCRIPTION

This section provides the naming and functional description of the internal and external signals. [Section 6.0 "I/O Multiplexing and Considerations"](#) describes the routing of these signals between the MCU core and radio subsystem and to the external package pins.

TABLE 5-1: SIGNAL DESCRIPTIONS LIST

Signal Name	Function	Type
Analog Comparators (AC)		
AIN<3:0>	AC Analog Inputs	Analog
CMP<1:0>	AC Comparator Outputs	Digital
Analog Digital Converter (ADC)		
AIN<19:0>	ADC Analog Inputs	Analog
VREFB	ADC Voltage External Reference B	Analog
Operational Amplifier (OPAMP)		
OANEG<2:0>	OPAMP Analog Negative Inputs	Analog
OAPOS<2:0>	OPAMP Analog Positive Inputs	Analog
OAOUT<2:0>	OPAMP Analog Outputs	Analog
External Interrupt Controller (EIC)		
EXTINT<15:0>	External Interrupts Inputs	Digital
NMI	External Non-Maskable Interrupt Input	Digital
Reset Controller (RSTC)		
EXTWAKE<7:0>	External Wake-Up Inputs	Digital
Generic Clock Generator (GCLK)		
GCLK_IO<7:0>	Generic Clock (source clock inputs or generic clock generator output)	Digital
Custom Control Logic (CCL)		
IN<11:0>	Logic Inputs	Digital
OUT<3:0>	Logic Outputs	Digital
Supply Controller (SUPC)		
VBAT	External Battery Supply Inputs	Analog
PSOK	Main Power Supply OK Input	Digital
OUT<1:0>	Logic Outputs	Digital
Power Manager (PM)		
RESETN ⁽¹⁾	Reset Input	Digital
Serial Communication Interface (SERCOMx)		
PAD<3:0>	SERCOM Inputs/Outputs Pads	Digital
Oscillators Control (OSCCTRL)		
XIN	Crystal or External Clock Input	Analog/Digital
XOUT	Crystal Output	Analog
32KHz Oscillators Control (OSC32KCTRL)		
XIN32	32KHz Crystal or External Clock Input	Analog/Digital
XOUT32	32KHz Crystal Output	Analog
Timer Counter (TCx)		
WO<1:0>	Waveform Outputs	Digital
Timer Counter (TCCx)		
WO<7:0>	Waveform Outputs	Digital

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TABLE 5-1: SIGNAL DESCRIPTIONS LIST (CONTINUED)

Signal Name	Function	Type
Peripheral Touch Controller (PTC)		
X<15:0>	PTC Input	Analog
Y<15:0>	PTC Input	Analog
General Purpose I/O (PORT)		
PA01-PA00	Parallel I/O Controller I/O Port A	Digital
PA09-PA04	Parallel I/O Controller I/O Port A	Digital
PA19-PA12	Parallel I/O Controller I/O Port A	Digital
PA25-PA22	Parallel I/O Controller I/O Port A	Digital
PA28-PA27	Parallel I/O Controller I/O Port A	Digital
PA03-PB02	Parallel I/O Controller I/O Port B	Digital
PA23-PB22	Parallel I/O Controller I/O Port B	Digital
Universal Serial Bus (USB)		
DP	DP for USB	Digital
DM	DM for USB	Digital
SOF1 kHz	USB Start of Frame	Digital
External RF Signals		
RF_XTB	XTAL Connection	OSC
RF_XTA	XTAL Connection or TCXO Input	OSC
VRDIG_RF	Regulated Supply Voltage for Digital Blocks	Reg Output
VDDANA_RF	Supply Voltage for Analog Circuitry	Analog Power
VRANA_RF	Regulated Supply Voltage for Analog Circuitry	Reg Output
RFI_LF	RF Input for Bands 2 and 3	RF Input
RFO_LF	RF Output for Bands 2 and 3	RF Output
PA_BOOST	Optional High-Power PA Output, all Frequency Bands	RF Output
VRPA_RF	Regulated Supply Voltage for the PA	Reg Output
VDDIN_RF	Supply Voltage for RF Blocks	RF Power
RFO_HF	RF Output for Band 1	RF Output
VDDDIG_RF	Supply Voltage for Digital Blocks	Digital Power
RXTX_RF	RX/TX Switch Control: High in TX	Digital I/O
RFI_HF	RF Input for Band 1	RF Input
Internal RF Signals		
DIO0	Digital I/O, Software Configured	I/O
DIO1/DCLK	Digital I/O, Software Configured	I/O
DIO2/DATA	Digital I/O, Software Configured	I/O
DIO3	Digital I/O, Software Configured	I/O
DIO4	Digital I/O, Software Configured	I/O
DIO5	Digital I/O, Software Configured	I/O
SCLK	SPI Clock Input	Input
MISO	SPI Data Output	Output
MOSI	SPI Data Input	Input
SEL	SPI Chip Select Input	Input
RF_RST	Reset Trigger Input	I/O

Note 1: Active level: Low.

6.0 I/O MULTIPLEXING AND CONSIDERATIONS

6.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively may be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0..31) in the PORT must be written to '1'. The selection of peripheral functions A to H are done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

TABLE 6-1: PORT FUNCTION MULTIPLEXING

Pin	I/O Pin	Supply	A					B ⁽¹⁾⁽²⁾			C	D	E	F	G	H	I
			EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM ⁽¹⁾⁽²⁾	SERCOM-ALT	TC/TCC	TCC	COM	AC/GCLK/SUPC	CCL
A3	PA00	VSWOUT	EXTINT[0]	EXTWAKE[0]	—	—	—	—	—	—	—	SERCOM1/PAD[0]	TCC2/WO[0]	—	—	—	—
A4	PA01	VSWOUT	EXTINT[1]	EXTWAKE[1]	—	—	—	—	—	—	—	SERCOM1/PAD[1]	TCC2/WO[1]	—	—	—	—
D3	PA04	VDDANA	EXTINT[4]	EXTWAKE[4]	VREFB	AIN[4]	AIN[0]	—	—	OAOUT[2]	—	SERCOM0/PAD[0]	TCC0/WO[0]	—	—	—	CCL0/IN[0]
C4	PA05	VDDANA	EXTINT[5]	EXTWAKE[5]	—	AIN[5]	AIN[1]	—	—	OAPOS[2]	—	SERCOM0/PAD[1]	TCC0/WO[1]	—	—	—	CCL0/IN[1]
E3	PA06	VDDANA	EXTINT[6]	EXTWAKE[6]	—	AIN[6]	AIN[2]	—	Y[4]	OAPOS[0]	—	SERCOM0/PAD[2]	TCC1/WO[0]	—	—	—	CCL0/IN[2]
F3	PA07	VDDANA	EXTINT[7]	EXTWAKE[7]	—	AIN[7]	AIN[3]	—	—	OAOUT[0]	—	SERCOM0/PAD[3]	TCC1/WO[1]	—	—	—	CCL0/OUT[0]
F4	PA08	VDDIO	NMI	—	—	AIN[16]	—	X[0]	Y[6]	—	SERCOM0/PAD[0]	SERCOM2/PAD[0]	TCC0/WO[0]	TCC1/WO[2]	—	—	CCL1/IN[3]
F5	PA09	VDDIO	EXTINT[9]	—	—	AIN[17]	—	X[1]	Y[7]	—	SERCOM0/PAD[1]	SERCOM2/PAD[1]	TCC0/WO[1]	TCC1/WO[3]	—	—	CCL1/IN[1]
F6	PA13	VDDIO	EXTINT[13]	—	—	—	—	—	—	—	SERCOM2/PAD[1]	SERCOM4/PAD[1]	TCC2/WO[1]	TCC0/WO[7]	—	AC/CMP[1]	—
F8	PA14	VDDIO	EXTINT[14]	—	—	—	—	—	—	—	SERCOM2/PAD[2]	SERCOM4/PAD[2]	TC4/WO[0]	TCC0/WO[4]	—	GCLK_IO[0]	—
G8	PA15	VDDIO	EXTINT[15]	—	—	—	—	—	—	—	SERCOM2/PAD[3]	SERCOM4/PAD[3]	TC4/WO[1]	TCC0/WO[5]	—	GCLK_IO[1]	—
F7	PA16	VDDIO	EXTINT[0]	—	—	—	—	X[4]	—	—	SERCOM1/PAD[0]	SERCOM3/PAD[0]	TCC2/WO[0]	TCC0/WO[6]	—	GCLK_IO[2]	CCL0/IN[0]
E6	PA17	VDDIO	EXTINT[1]	—	—	—	—	X[5]	—	—	SERCOM1/PAD[1]	SERCOM3/PAD[1]	TCC2/WO[1]	TCC0/WO[1]	—	GCLK_IO[3]	CCL0/IN[1]
E7	PA18	VDDIO	EXTINT[2]	—	—	—	—	X[6]	—	—	SERCOM1/PAD[2]	SERCOM3/PAD[2]	TC4/WO[0]	TCC0/WO[2]	—	AC/CMP[0]	CCL0/IN[2]
E8	PA19	VDDIO	EXTINT[3]	—	—	—	—	X[7]	—	—	SERCOM1/PAD[3]	SERCOM3/PAD[3]	TC4/WO[1]	TCC0/WO[3]	—	AC/CMP[1]	CCL0/OUT[0]

TABLE 6-1: PORT FUNCTION MULTIPLEXING (CONTINUED)

Pin	I/O Pin	Supply	A					B ⁽¹⁾⁽²⁾			C	D	E	F	G	H	I
			EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM ⁽¹⁾⁽²⁾	SERCOM-ALT	TC/TCC	TCC	COM	AC/GCLK/SUPC	CCL
D8	PA22	VDDIO	EXTINT[6]	—	—	—	—	X[10]	—	—	SERCOM3/PAD[0]	SERCOM5/PAD[0]	TC0/WO[0]	TCC0/WO[4]	—	GCLK_IO[6]	CCL2/IN[0]
D7	PA23	VDDIO	EXTINT[7]	—	—	—	—	X[11]	—	—	SERCOM3/PAD[1]	SERCOM5/PAD[1]	TC0/WO[1]	TCC0/WO[5]	USB/SOF 1 KHz[6]	GCLK_IO[7]	CCL2/IN[1]
B8	PA24	VDDIO	EXTINT[12]	—	—	—	—	—	—	—	SERCOM3/PAD[2]	SERCOM5/PAD[2]	TC1/WO[0]	TCC1/WO[2]	USB/DM[6]	—	CCL2/IN[2]
C8	PA25	VDDIO	EXTINT[13]	—	—	—	—	—	—	—	SERCOM3/PAD[3]	SERCOM5/PAD[3]	TC1/WO[1]	TCC1/WO[3]	USB/DP[6]	—	CCL2/OUT[2]
E5	PB22	VDDIN	EXTINT[6]	—	—	—	—	—	—	—	—	SERCOM5/PAD[2]	TC3/WO[0]	—	—	GCLK_IO[0]	CCL0/IN[0]
C7	PB23	VDDIN	EXTINT[7]	—	—	—	—	—	—	—	—	SERCOM5/PAD[3]	TC3/WO[1]	—	—	GCLK_IO[1]	CCL0/OUT[0]
E4	PA27	VDDIN	EXTINT[15]	—	—	—	—	—	—	—	SERCOM3/PAD[0]	—	—	—	—	GCLK_IO[0]	—
C6	PA28	VDDIN	EXTINT[8]	—	—	—	—	—	—	—	SERCOM3/PAD[1]	—	—	—	—	GCLK_IO[0]	—
C5	PA30	VDDIN	EXTINT[10]	—	—	—	—	—	—	—	—	SERCOM1/PAD[2]	TCC1/WO[0]	—	SWCLK	GCLK_IO[0]	CCL1/IN[0]
D5	PA31	VDDIN	EXTINT[11]	—	—	—	—	—	—	—	—	SERCOM1/PAD[3]	TCC1/WO[1]	—	SWDIO ⁽³⁾	—	CCL1/OUT[1]
B4	PB02	VSWOUT	EXTINT[2]	—	—	AIN[10]	—	—	—	—	—	SERCOM5/PAD[0]	TC2/WO[0]	—	—	SUPC/OUT[1]	CCL0/OUT[0]
C3	PB03	VSWOUT	EXTINT[3]	—	—	AIN[11]	—	—	—	—	—	SERCOM5/PAD[1]	TC2/WO[1]	—	—	SUPC/VBAT	

- Note**
- 1: All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
 - 2: Only some pins can be used in SERCOM I²C mode. See also [Section 6.3.3 "SERCOM I²C Pins"](#).
 - 3: This function is only activated in the presence of a debugger.
 - 4: When an analog peripheral is enabled, the analog output of the peripheral will interfere with the alternative functions of this pin. This is also true even when the peripheral is used for internal purposes.
 - 5: Clusters of multiple GPIO pins are sharing the same supply pin. See [Section 6.3.4 "GPIO Clusters"](#).
 - 6: USB is not available on R35J devices.

6.2 Internal Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively may be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to '1'. The selection of peripheral functions A to H are done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

TABLE 6-2: INTERNAL MULTIPLEXED SIGNALS

Internal Signal	I/O Pin	Supply	Type	A		B						C	D	E	F	G	H	I
				EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM	SERCOM-ALT	TC/TCC	FECTRL/ TCC/ SERCOM	COM	AC/GCLK/ SUPC	CCL
DIO0	PB16	VDDIO	I/O	EXTINT[0]	—	—	—	—	—	—	—	SERCOM5/ PAD[0]	—	TCC2/ WO[0]	TCC0/ WO[4]	—	GCLK_IO[2]	CCL3/ IN[11]
DIO1/ DCLK	PA11	VDDIO	I/O	EXTINT[11]	—	—	AIN[19]	—	X[3]	Y[9]	—	SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TCC1/ WO[1]	TCC0/ WO[3]	—	GCLK_IO[5]	CCL1/ OUT[1]
DIO2/ DATA	PA12	VDDIO	I/O	EXTINT[12]	—	—	—	—	—	—	—	SERCOM2/ PAD[0]	SERCOM4/ PAD[0]	TCC2/ WO[0]	TCC0/ WO[6]	—	AC/CMP[0]	—
DIO3	PB17	VDDIO	I/O	EXTINT[1]	—	—	—	—	—	—	—	SERCOM5/ PAD[1]	—	TCC2/ WO[1]	TCC0/ WO[5]	—	GCLK_IO[3]	CCL3/ OUT[3]
DIO4	PA10	VDDIO	I/O	EXTINT[10]	—	—	AIN[18]	—	X[2]	Y[8]	—	SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TCC1/ WO[0]	TCC0/ WO[2]	—	GCLK_IO[4]	CCL1/ IN[5]
DIO5	PB00	VDDANA	I/O	EXTINT[0]	—	—	AIN[8]	—	—	—	—	—	SERCOM5/ PAD[2]	TCC3/ WO[0]	—	—	SUPC_PSOK	CCL0/IN[1]
RF_RST	PB15	VDDIO	I/O	EXTINT[15]	—	—	—	—	X[15]	—	—	SERCOM4/ PAD[3]	—	TCC0/ WO[1]	—	—	GCLK_IO[1]	CCL3/ IN[10]
MOSI	PB30	VDDIO	I/O	EXTINT[14]	—	—	—	—	—	—	—	—	SERCOM5/ PAD[0]	TCC0/ WO[0]	SERCOM4/ PAD[2]	—	—	—
SEL	PB31	VDDIO	I/O	EXTINT[15]	—	—	—	—	—	—	—	—	SERCOM5/ PAD[1]	TCC0/ WO[1]	SERCOM4/ PAD[1]	—	—	—
SCLK	PC18	VDDIO	I/O	—	—	—	—	—	—	—	—	—	—	—	SERCOM4/ PAD[3]	—	—	—
MISO	PC19	VDDIO	I/O	—	—	—	—	—	—	—	—	—	—	—	SERCOM4/ PAD[0]	—	—	—

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6.3 Other Functions

6.3.1 OSCILLATOR PINOUT

The oscillators are not mapped to the normal PORT functions and their multiplexing are controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32KHz Oscillators Controller (OSC32KCTRL).

TABLE 6-3: OSCILLATOR PINOUT

Oscillator	Supply	Signal	I/O Pin
XOSC	VDDIO	XIN	PA14
		XOUT	PA15
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

To improve the cycle-to-cycle jitter of XOSC32, it is recommended to keep the neighboring pins of XIN32 and XOUT32 following pins as static as possible.

TABLE 6-4: XOSC32 JITTER MINIMIZATION

Package Pin Count	Static Signal Recommended
64	PB02, PB03

6.3.2 SERIAL WIRE DEBUG INTERFACE PINOUT

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

TABLE 6-5: SERIAL WIRE DEBUG INTERFACE PINOUT

Signal	Supply	I/O Pin
SWCLK	VDDIN	PA30
SWDIO	VDDIN	PA31

6.3.3 SERCOM I²C PINS

TABLE 6-6: SERCOM PINS SUPPORTING I²C

Device	Pins Supporting I ² C Hs mode
SAM R34J/R35J	PA08, PA09, PA13, PA16, PA17, PA22, PA23

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6.3.4 GPIO CLUSTERS

TABLE 6-7: GPIO CLUSTERS

Package	Cluster	GPIO													Supplies Pins Connected to the Cluster
64 Pins	1	PA31	PA30	—	—	—	—	—	—	—	—	—	—	—	VDDIN C4/ GND D4
	2	PA28	PA27	PB23	PB22	—	—	—	—	—	—	—	—	—	VDDIN C4/ GND D4 and VDDIO C6/ GND C5
	3	PA25	PA24	PA23	PA22	—	—	PA19	PA18	PA17	PA16	PA15	PA14	PA13	VDDIO C6/ GND C5 and VDDIO F3/ GND F4
	4	—	—	PA09	PA08	—	—	—	—	—	—	—	—	—	VDDIO F3/ GND F4
	5	PA07	PA06	PA05	PA04	—	—	—	—	—	—	—	—	—	VDDANA C1/ GNDANA C3
	6	—	—	PA01	PA00	PB03	PB02	—	—	—	—	—	—	—	VDDANA C1/ GNDANA C3

6.3.5 TCC CONFIGURATIONS

The SAM R34/R35 has three instances of the Timer/Counter for Control applications (TCC) peripheral, TCC<2:0>.

TABLE 6-8: TCC CONFIGURATION SUMMARY

TCC No.	Channels (CC_NUM)	Waveform Output (WO_NUM)	Counter size	Fault	Dithering	Output matrix	Dead Time Insertion (DTI)	SWAP	Pattern generation
0	4	8	24-bit	Yes	Yes	Yes	Yes	Yes	Yes
1	2	4	24-bit	Yes	Yes	—	—	—	Yes
2	2	2	16-bit	Yes	—	—	—	—	—

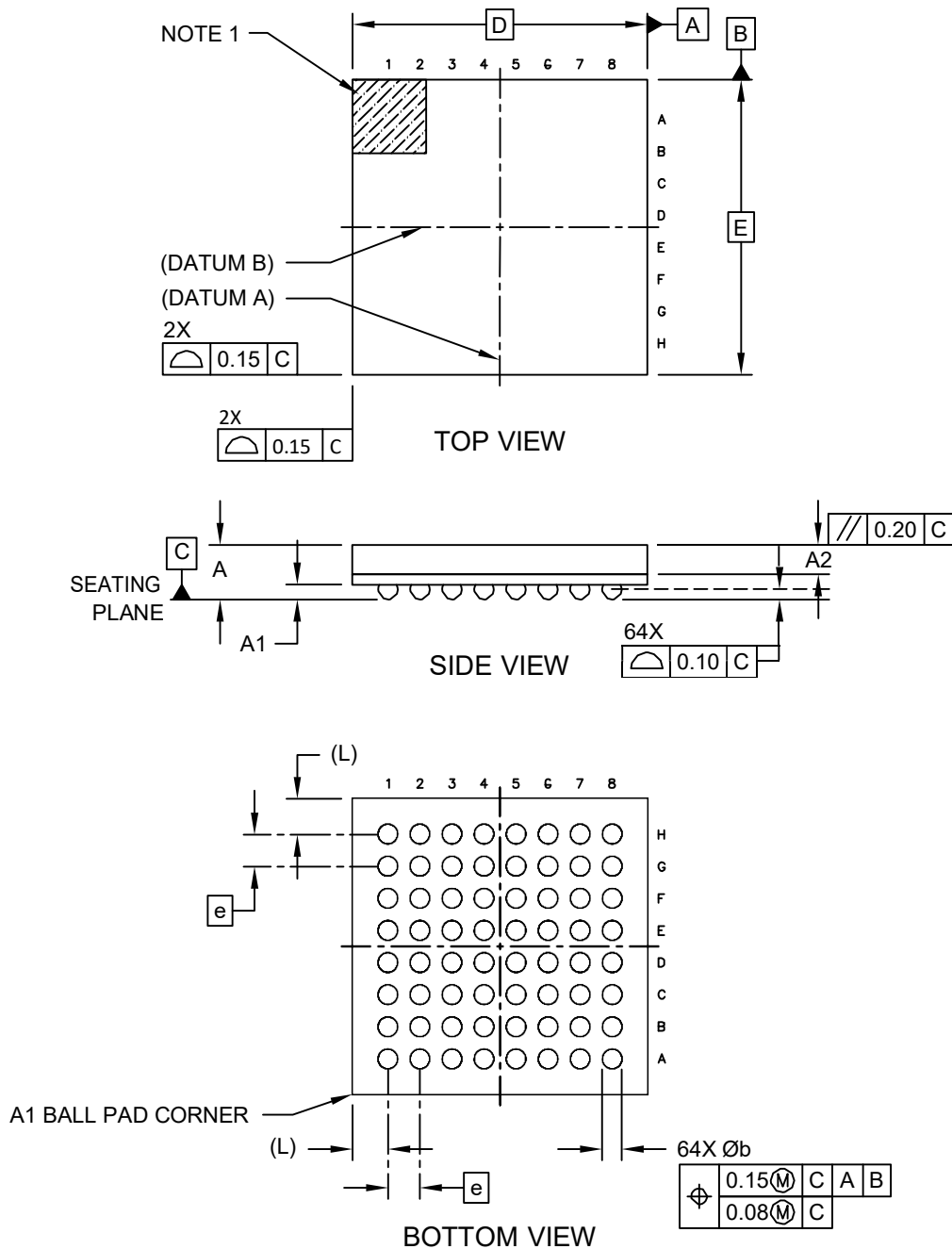
Note 1: The number of CC registers (CC_NUM) for each TCC corresponds to the number of compare/capture channels to ensure that a TCC can have more Waveform Outputs (WO_NUM) than CC registers.

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7.0 PACKAGING INFORMATION

64-Lead Thin, Fine Pitch Ball Grid Array Package (7JX) - 6x6 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

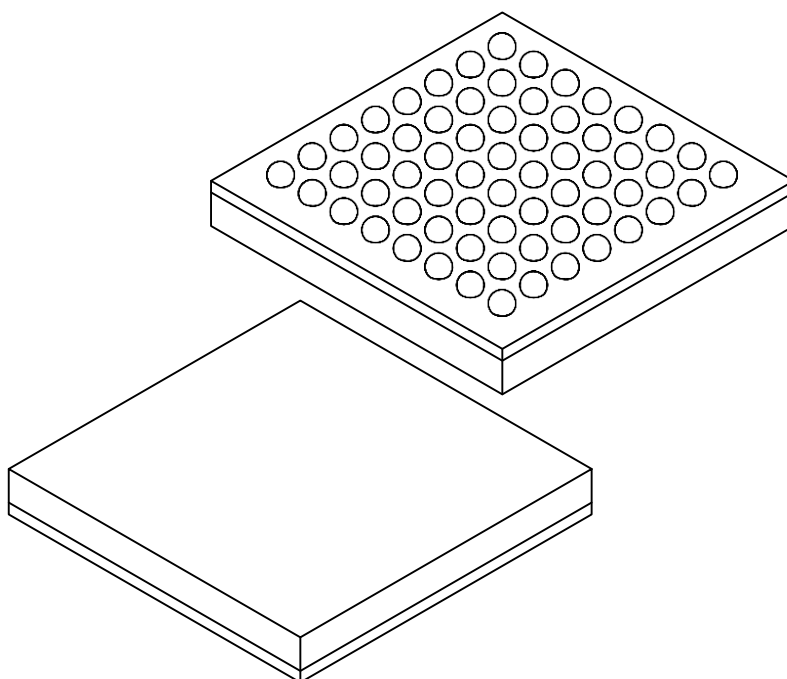


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64-Lead Thin, Fine Pitch Ball Grid Array Package (7JX) - 6x6 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	64		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Ball Height	A1	0.21	0.30	-
Mold Cap Thickness	A2	0.55	0.60	0.65
Overall Length	D	6.00 BSC		
Overall Width	E	6.00 BSC		
Terminal Ball Diameter	b	0.35	0.40	0.45
Edge to Ball Center	(L)	0.725 REF		

Notes:

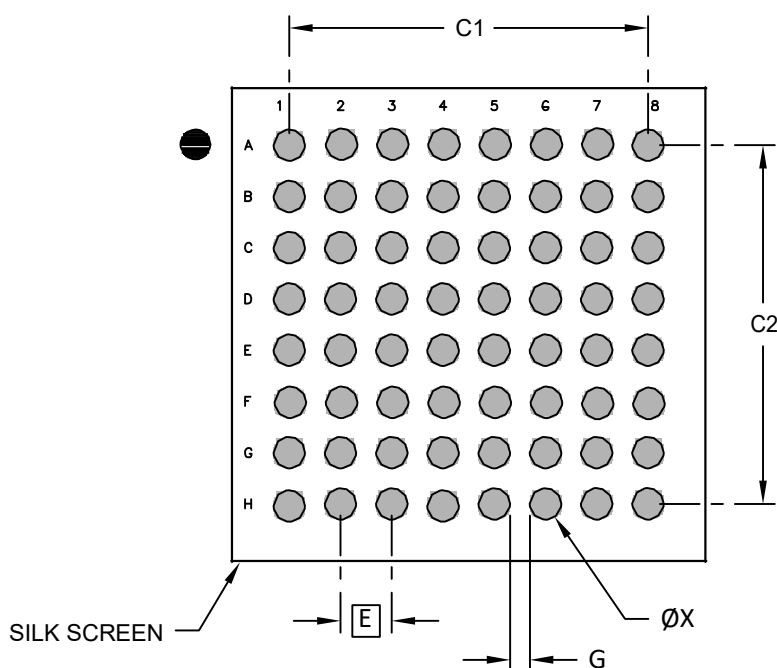
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-443 Rev B Sheet 2 of 2

SAM R34/R35 64-PIN

64-Lead Thin, Fine Pitch Ball Grid Array Package (7JX) - 6x6 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		4.55	
Contact Pad Spacing	C2		4.55	
Contact Pad Diameter (X64)	X			0.40
Space Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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APPENDIX A: REVISION HISTORY

Revision A (April 2017)

This is the initial release of this document.

Revision B (August 2017)

This revision includes the following updates:

- Updated [Figure 4.1](#).
- Updated [Table 1-1](#), [Table 2-1](#), [Table 4.1](#), [Table 5-1](#), [Table 6-1](#), [Table 6-2](#), [Table 6-6](#), and [Table 6-7](#).
- Updated [Section 2.0 "Ordering Information"](#) and [Section 4.1 "BGA Diagram for SAM R34/R35"](#).

Revision C (September 2017)

This revision includes the following updates:

- Updated [Figure 4.1](#).
- Updated [Section 2.0 "Ordering Information"](#).
- Updated [Table 2-1](#) and [Table 2-2](#).

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