Jaeyoung Kang

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EDUCATION

University of Illinois at Urbana Champaign | *Doctor of Philosophy in Electrical Computer Engineering*

- Expected graduation: December 2029

University of Illinois at Urbana Champaign | *Bachelor of Science in Computer Engineering*

- GPA: 3.93/4.0
- Relevant Courses: Computer Organization and Design, Computer Systems Engineering, Digital Systems Laboratory, Applied Parallel Programming, Intro to Algorithms & Models of comp

SUMMARY OF SKILLS

- Languages: Python, C++, C, SQL, CUDA C++, System Verilog, x86 Assembly
- Hardware & Simulation Tools: Quartus Prime, Gem5 simulator, RTL Simulation

WORK & RESEARCH EXPERIENCE

Software Engineer Intern Summer 2024
(C++, Python) Xcena Pangyo, South Korea

- Evaluated vector database performance via micro-benchmarking various filtering implementations.
- Focused on leveraging the Hierarchical Navigable Small World (HNSW) index to improve search efficiency in high-dimensional spaces

Intel In-memory Analytic Accelerator (Intel IAA) Spring 2024 - Fall 2024
(C++) (FAST lab, Prof. Nam Sung Kim) Champaign, IL

- Co-authored a conference paper (ISPASS 2025) on Intel's In-Memory Analytics Accelerator (IAA), featuring performance benchmarks, comparisons in real-world applications, and a practical usage guide.
- Investigated in evaluating micro-benchmarks on functions in IAA and integration into real-world database systems, such as Citus (a PostgreSQL extension) and Clickhouse, to demonstrate optimization strategies for high-performance data analytics.

ECE 220(Computer Systems & Programming) Teaching Assistant Spring 2024 - Fall 2024
(C++, LC3) Champaign, IL

- Leading office hours and lab sessions to help students' understanding of the lecture and assignment
- Designing challenging exam questions to check student's understanding

UPP: Universal Predicate Pushdown to Smart Storage Summer 2023 - Fall 2023
(C++, Python) (FAST lab, Prof. Nam Sung Kim) Champaign, IL

- Co-authored a conference paper (ISCA 2025)
- Filtered data with platform-neutral methods by hash

SUMMARY OF PROGRAMMING PROJECT

Linux Capable RISC-V CPU (System Verilog, RISC-V) Oct. 2023 – Dec. 2023

- Designed and verified a 5-stage pipelined CPU with L1 Cache, Victim Cache, Branch Predictor, and Wallace-Tree Multiplier
- Ran gate-level synthesis on RTL design to generate power, area and critical path statistics
- Simulated design with customized thorough test cases

Linux-like Operating System Design (C, x86 Assembly Linux) Oct. 2022 – Dec. 2022

- Constructed basic paging support for tasks, separated 4 MB pages for the kernel and user
- Wrote the system call interface along with ten system calls
- Provided support for six tasks from program images in the file system which interface with the kernel via system calls, multiple terminals, and basic scheduling