# Digital System Laboratory

## FPGA

T. Hui

# Introduction to FPGA

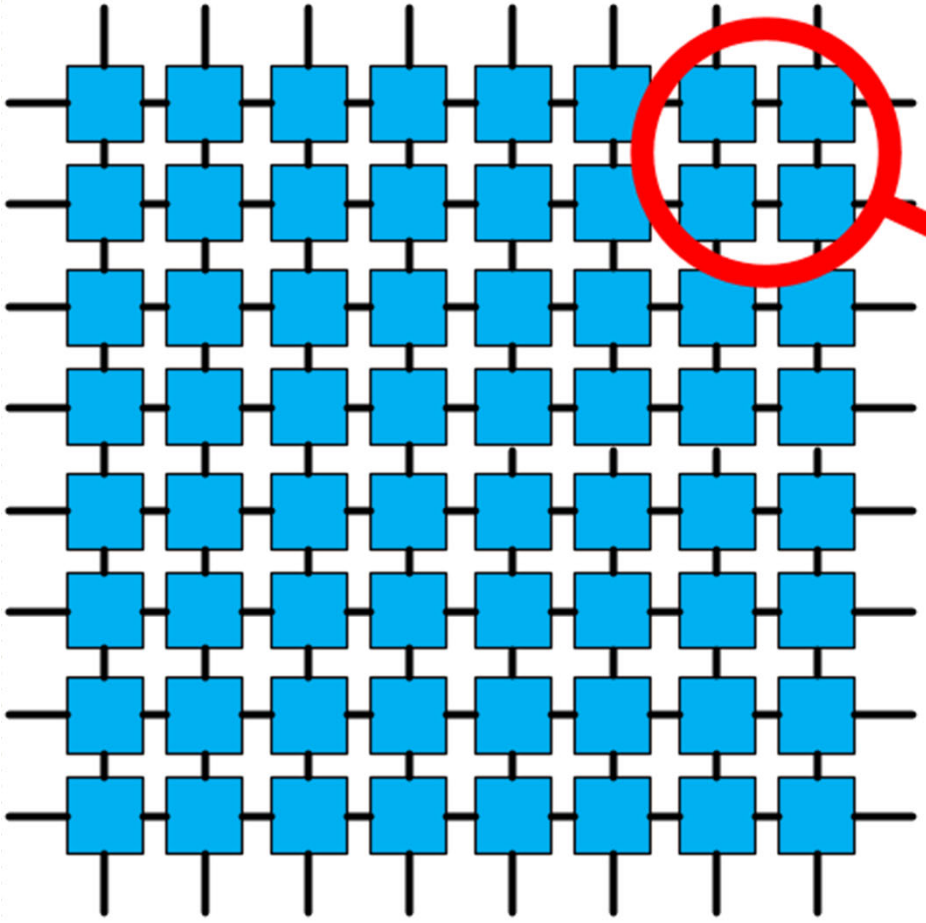
# Lesson Plan

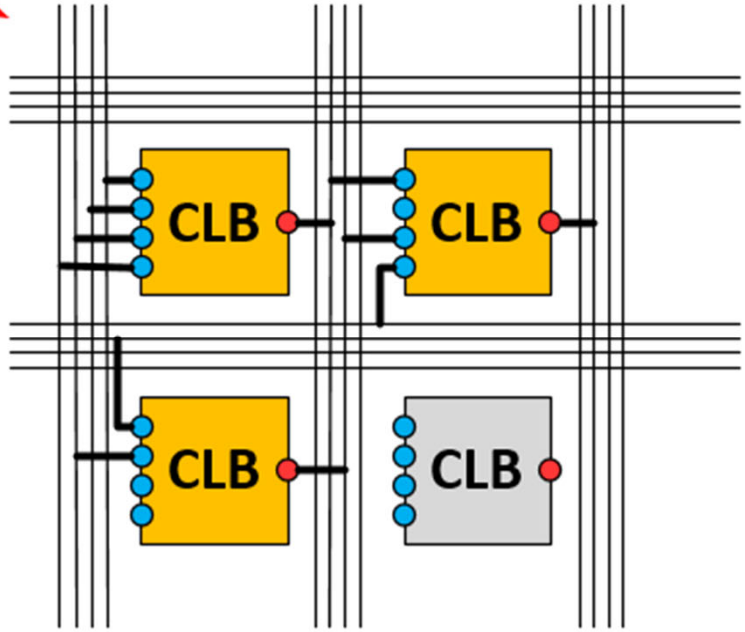
- Introduction to FPGA
- FPGA boards briefing
- FPGA software setup
- Handson – Tasks

# Introduction to FPGA

- FPGA:  Field Programmable Gate Array

# FPGA Fabric

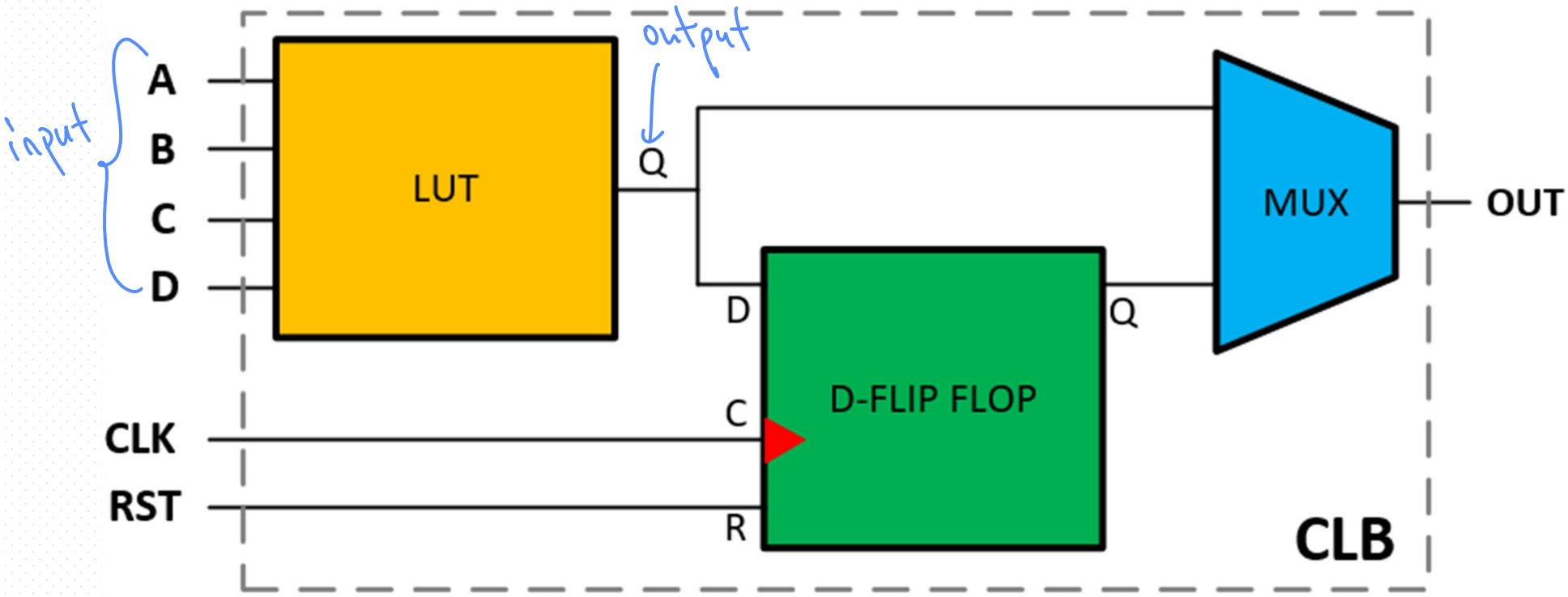



CLBs: Configurable Logic Block
CLB
CLB
CLB
CLB
interconnect

CLB

~~CBLs~~

**LUT: Lookup Table**



# Parameterizing a CLB

- FPGA is about parameterizing a CLB, by bitstream.
- Bitstream is generated from HDL through synthesis.

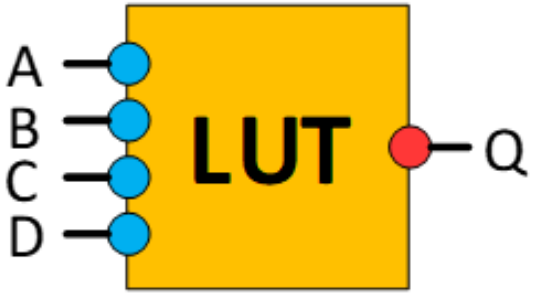
input

output

| D | C | B | A | Q |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| : | : | : | : | : |
| 1 | 1 | 1 | 1 | 0 |

4 bits

: $2^4$ combi



# Input/Output

- Interface blocks (called IOBs)
- Input, Output or InOut
- Push-pull, open drain, etc.

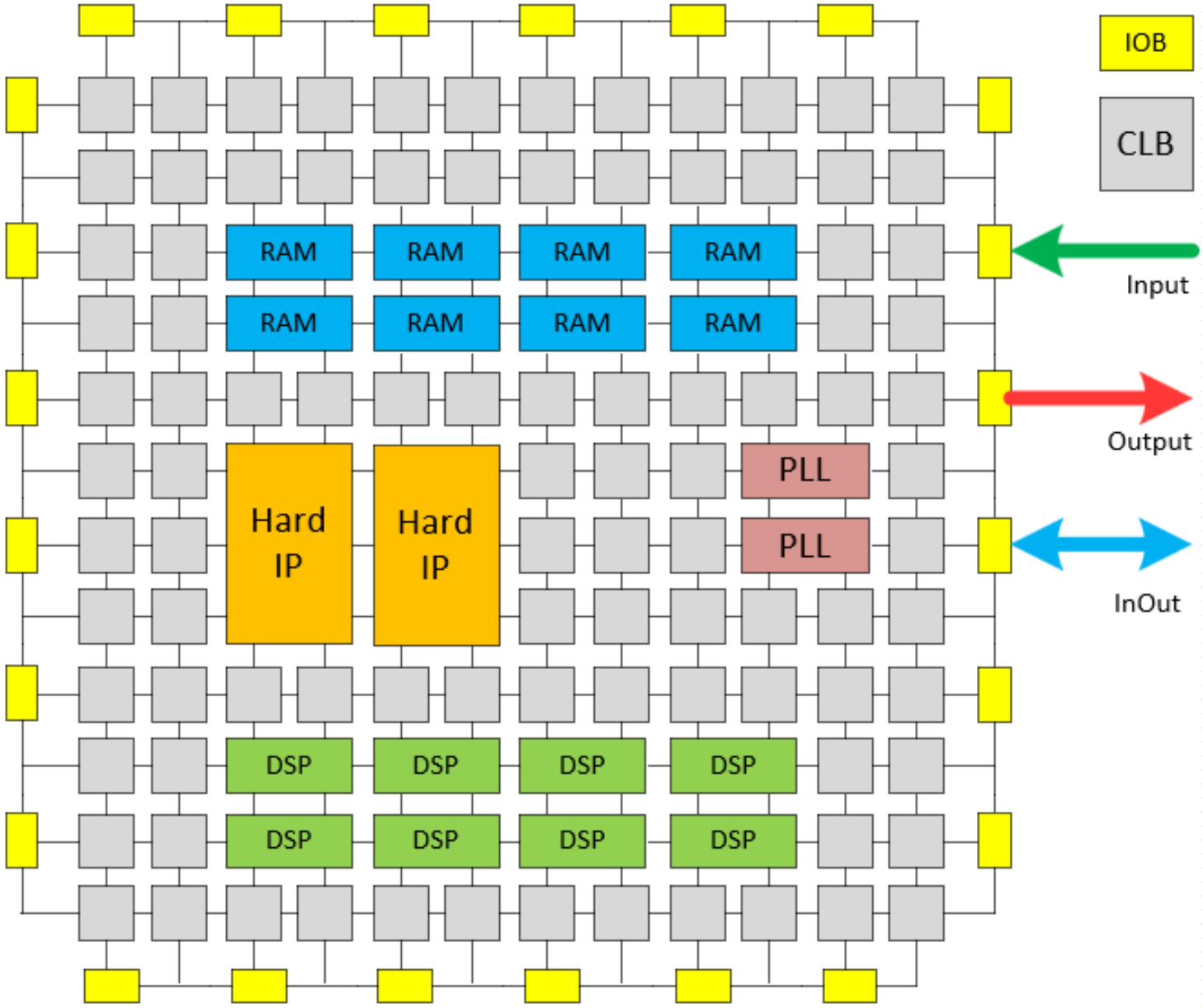
MOSFETS

# Special Blocks

- Memories
  - RAM banks
- DSP (digital signal processing)
  - arithmetic blocks
- PLL (phase lock loop)
  - multiple clock signals, at different phases and frequencies
- serdes (Serializer-Deserializer)
  - allow parallel/serial conversion and vice versa at speeds of several Gb/s
- Others
  - controllers for external DRAM, Ethernet modules, A/D and D/A converters etc

# PLL

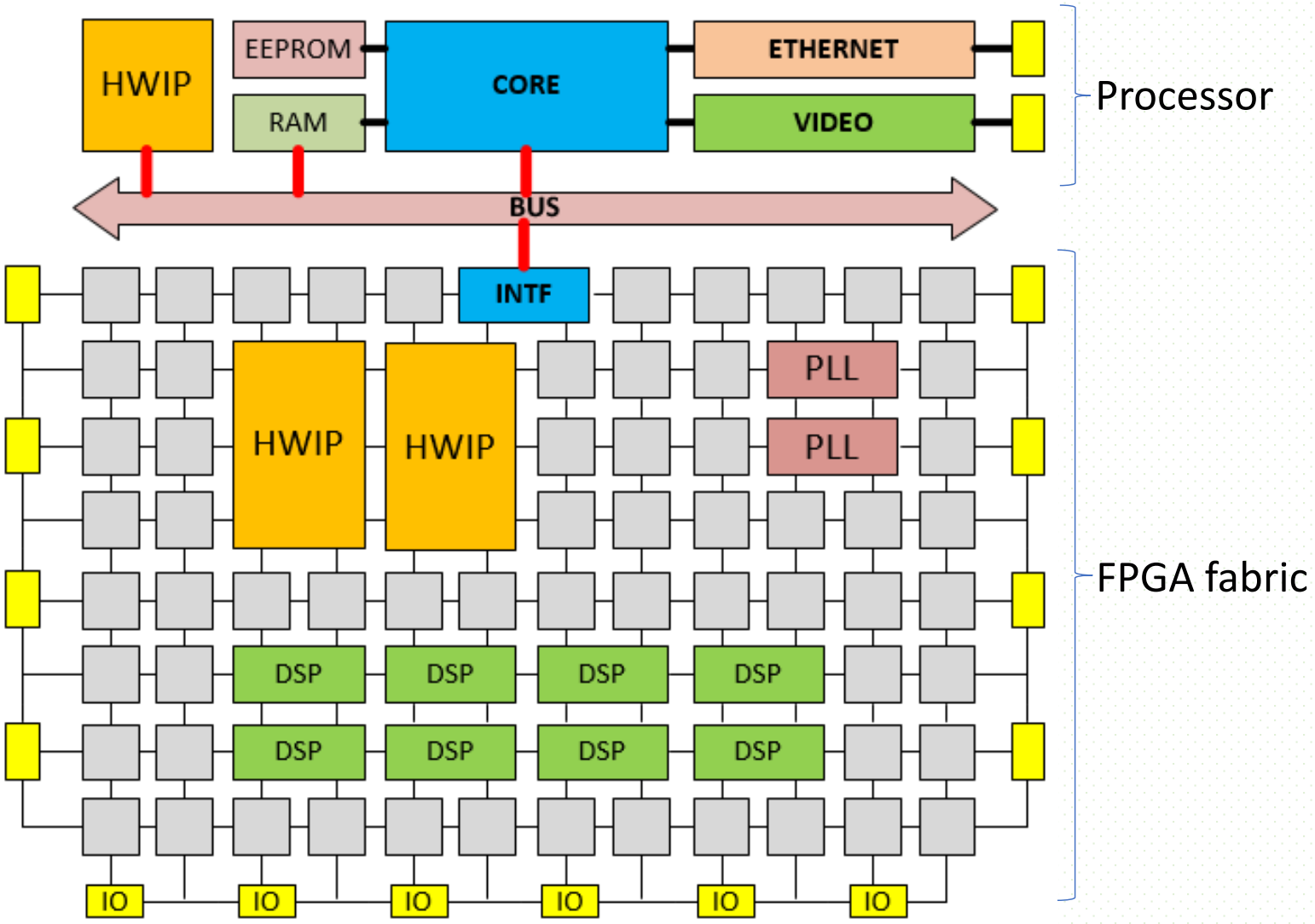
- PLL
  - multiple clock signals, at different phases and frequencies


IOB
CLB
RAM
RAM
RAM
RAM
RAM
RAM
RAM
RAM
Input
Output
Hard IP
Hard IP
PLL
PLL
InOut
DSP
DSP
DSP
DSP
DSP
DSP
DSP
DSP

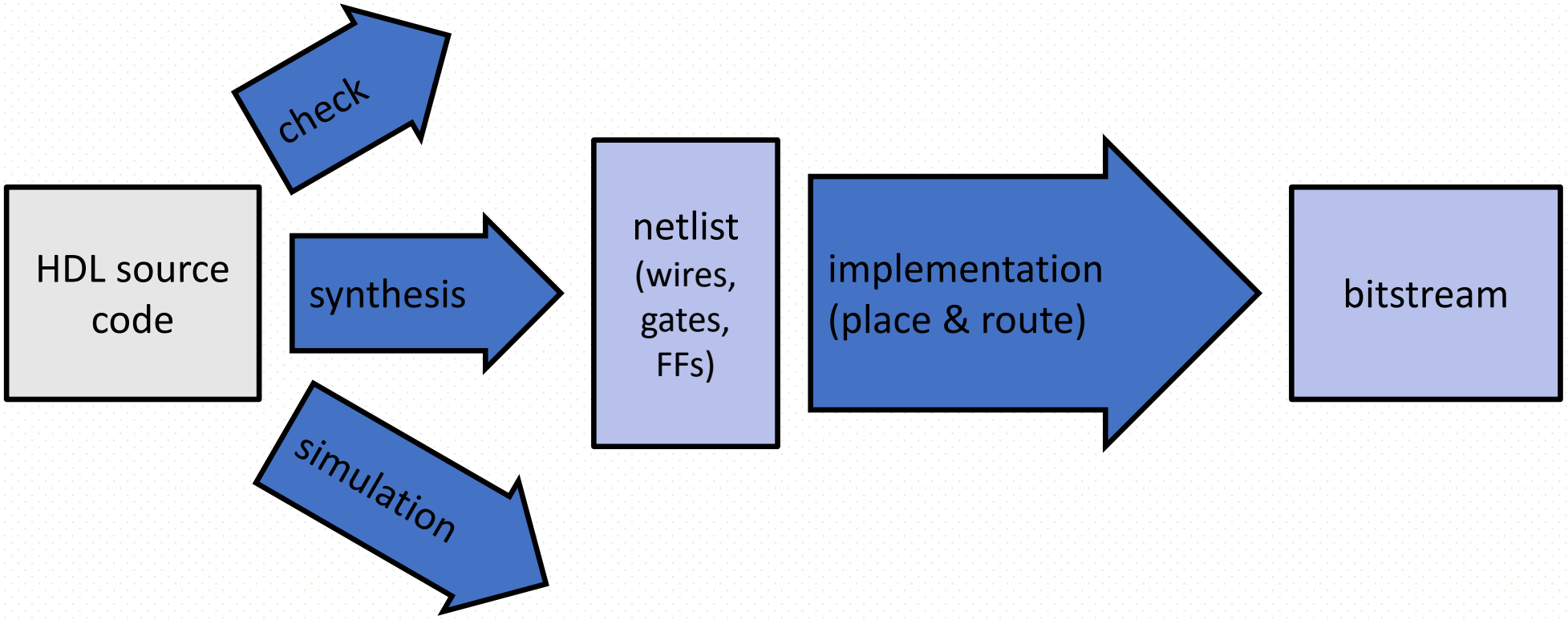
# FPGA - SoC

- SoC (System on Chip)
  - FPGA fabric
  - HPS (Hard Processor Systems), generally ARM or RISC-V core

# SoC


HWIP
EEPROM
RAM
CORE
ETHERNET
VIDEO
Processor
BUS
INTF
HWIP
HWIP
PLL
PLL
DSP
DSP
DSP
DSP
DSP
DSP
DSP
DSP
IO
IO
IO
IO
IO
IO
FPGA fabric

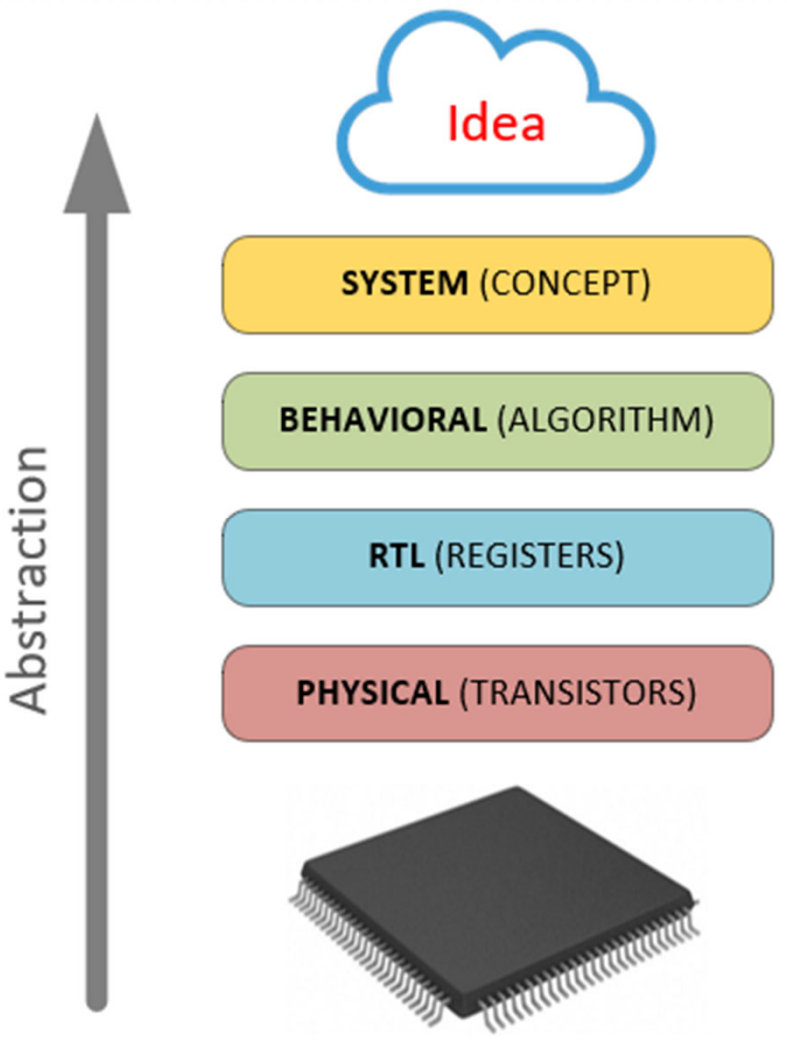
# FPGA Design Flow



# Programming a FPGA

- Programming a FPGA means establishing the parameterization of the individual blocks and their interconnections.
- Programming methodologies
  - System: Processor
  - Behavioral: HLS
  - RTL (Register Transfer Level): Verilog HDL
  - Physical: ASIC

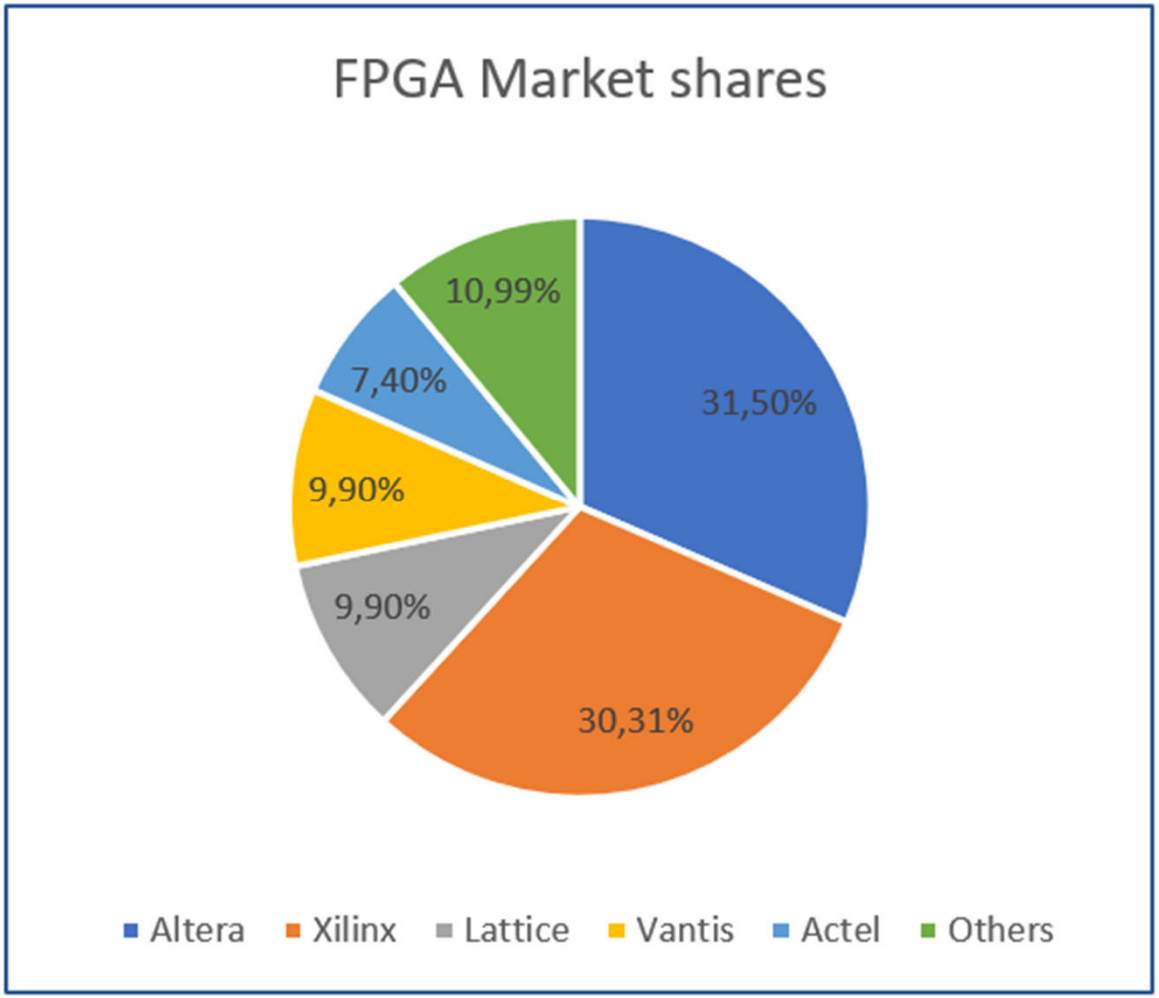
# Programming a FPGA



# Programming a FPGA

- Graphical
  - Schematic entry (NAND & NOR gates)
- Textual
  - Verilog HDL entry
  - VHDL

# FPGA Providers (old data)

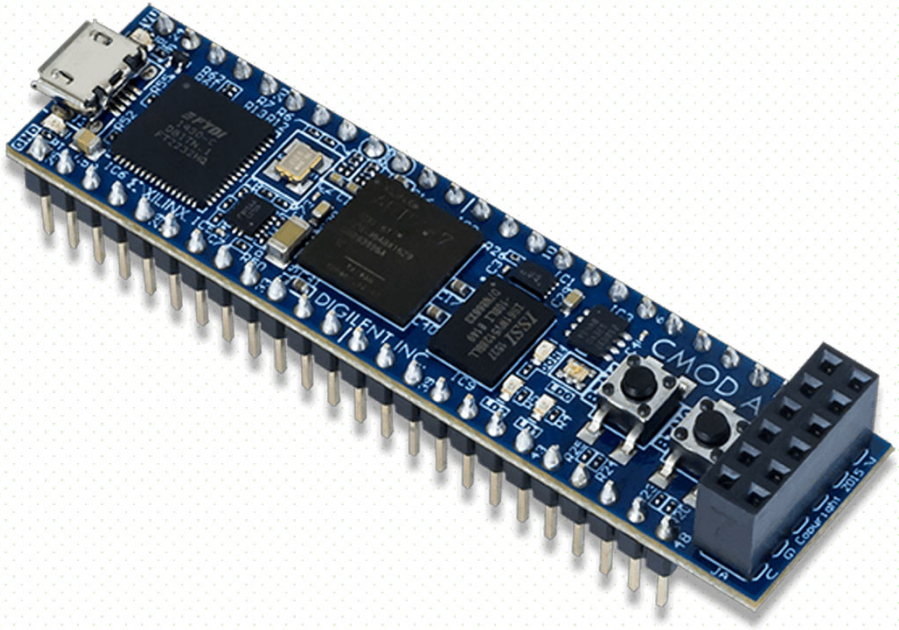


# FPGA Board

**Digilent Cmod A7-35T**

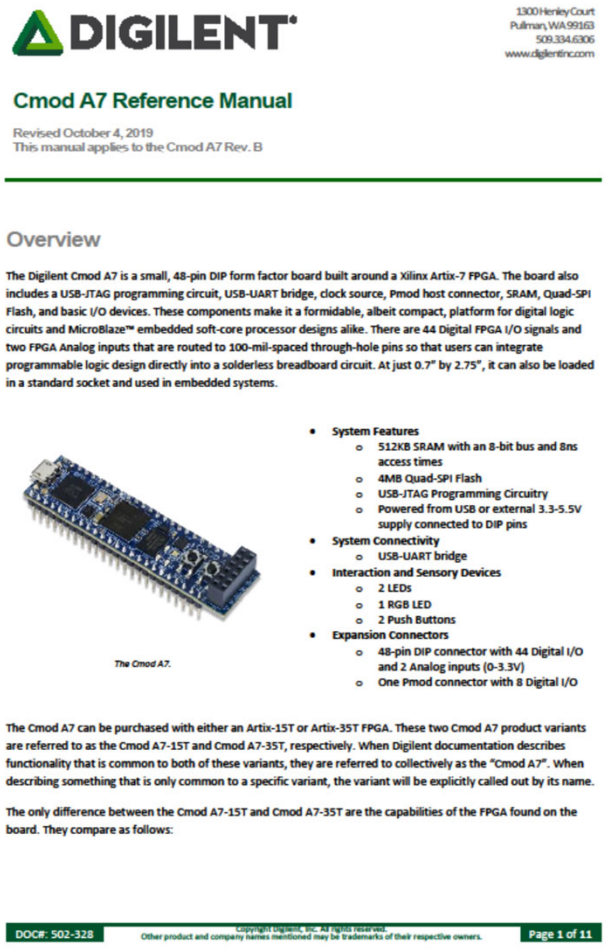
- Xilinx Artix-7 XC7A35T
- 33,280 CLBs, 1,800Kb of RAM blocks, 90 DSPs, 5 Transceivers at 6.6 Gb/s
- 512MB of SRAM
- Cmod A7-35 T is the board for 2D
- https://digilent.com/shop/cmod-a7-35t-breadboardable-artix-7-fpga-module/

**Breadboardable**



# Digilent Cmod A7-35T

- Cmod A7 Reference Manual
- https://digilent.com/reference/programmable-logic/cmod-a7/reference-manual?redirect=1



DIGILENT

1300 Henley Court
Pullman, WA 99163
509.334.6306
www.digilentinc.com

**Cmod A7 Reference Manual**

Revised October 4, 2019
This manual applies to the Cmod A7 Rev. B

## Overview

The Digilent Cmod A7 is a small, 48-pin DIP form factor board built around a Xilinx Artix-7 FPGA. The board also includes a USB-JTAG programming circuit, USB-UART bridge, clock source, Pmod host connector, SRAM, Quad-SPI Flash, and basic I/O devices. These components make it a formidable, albeit compact, platform for digital logic circuits and MicroBlaze™ embedded soft-core processor designs alike. There are 44 Digital FPGA I/O signals and two FPGA Analog inputs that are routed to 100-mil-spaced through-hole pins so that users can integrate programmable logic design directly into a solderless breadboard circuit. At just 0.7" by 2.75", it can also be loaded in a standard socket and used in embedded systems.

*The Cmod A7.*

- System Features
  - 512KB SRAM with an 8-bit bus and 8ns access times
  - 4MB Quad-SPI Flash
  - USB-JTAG Programming Circuitry
  - Powered from USB or external 3.3-5.5V supply connected to DIP pins
- System Connectivity
  - USB-UART bridge
- Interaction and Sensory Devices
  - 2 LEDs
  - 1 RGB LED
  - 2 Push Buttons
- Expansion Connectors
  - 48-pin DIP connector with 44 Digital I/O and 2 Analog inputs (0-3.3V)
  - One Pmod connector with 8 Digital I/O

The Cmod A7 can be purchased with either an Artix-15T or Artix-35T FPGA. These two Cmod A7 product variants are referred to as the Cmod A7-15T and Cmod A7-35T, respectively. When Digilent documentation describes functionality that is common to both of these variants, they are referred to collectively as the "Cmod A7". When describing something that is only common to a specific variant, the variant will be explicitly called out by its name.

The only difference between the Cmod A7-15T and Cmod A7-35T are the capabilities of the FPGA found on the board. They compare as follows:

# Digilent Cmod A7-35T

- System Features
- 512KB SRAM with an 8-bit bus and 8ns access times
- 4MB Quad-SPI Flash
- USB-JTAG Programming Circuitry
- Powered from USB or external 3.3-5.5V supply connected to DIP pins
- System Connectivity
- USB-UART bridge
- Interaction and Sensory Devices
- 2 LEDs, 1 RGB LED, 2 Push Buttons
- Expansion Connectors
- 48-pin DIP connector with 44 Digital I/O and 2 Analog inputs (0-3.3V)
- One Pmod connector with 8 Digital I/O

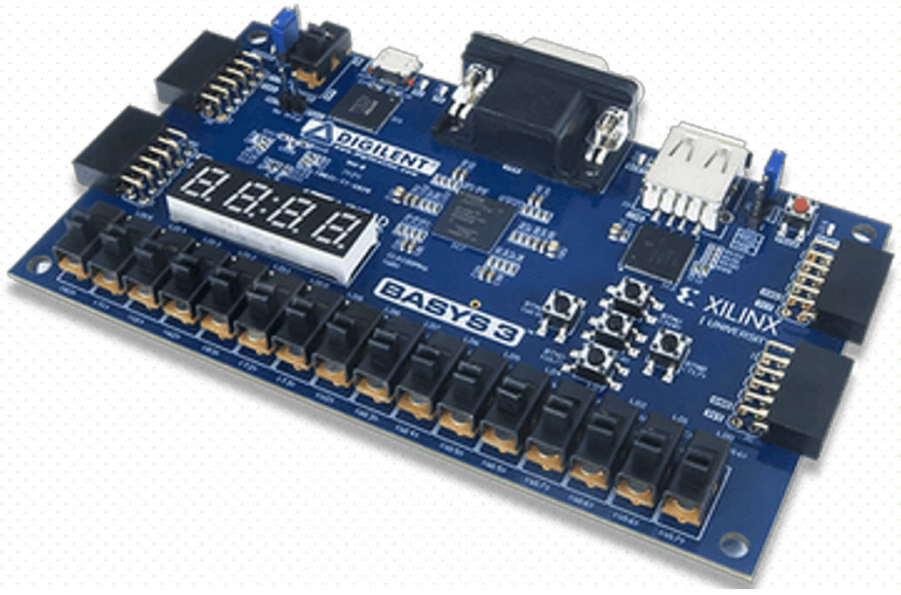
| Product Variant | Cmod A7-35T |
|---|---|
| FPGA Part | XC7A35T-1CPG236C |
| 1 MSPS On-chip ADC | Yes |
| Programming options | Quad-SPI Flash/JTAG |
| Look-up Tables (LUTs) | 20,800 |
| Flip-Flops | 41,600 |
| Block RAM | 225 KB |
| Clock Management Tiles | 5 |

# FPGA Board

**Digilent Basys 3**

- It has the same chip as the Cmod A7 35-T (to be used for 2D)
- It is a learning-oriented board, with
  - 16 switches, 5 buttons, 4 7-segment displays and a 12-bit VGA output
- Basys 3 will be used for Handson / Learning only
- https://digilent.com/reference/programmable-logic/basys-3/start

**Learning-oriented**



# FPGA Software

- Register an account with Xilinx
  - You need this registration for download, and installation
- Download Vivado-design-tools
  - 2023.1
- Please refer to the below Guide for detail setup

https://pe8sutd.larksuite.com/docx/NfZid9uy5oiYvbxoEWMui94HsfY?from=from_copylink

# 2D Briefing

- This 2D is a Group work.
- The Theme is Cybersecured Systems.
- The group needs to design a Pseudo-Random Numbers Generator, using Cmod A7 board.
- You can propose your project as well but limited to use CMOD A7, with external components.
- Evaluation criteria are:
  - Functionality, able to demonstrate working prototype, and show the evaluation processes
    - how to proof that your board is working as PRNG, e.g. the number is random?.
  - Innovativeness, able to implement unique ideas,
    - such as using a unique random source.
    - the design itself is conventional, but the process is new, e.g. using own fine-tuned generative AI to perform the design automatically.
  - Educational contribution, the documentation and prototype are comprehensive and be able to be used as learning materials for public
    - Compulsory to host in the accessible github, with proper documentation, source files.
    - Name the github for this project as Y23T6_PRNG_g***X***, where is the group number.

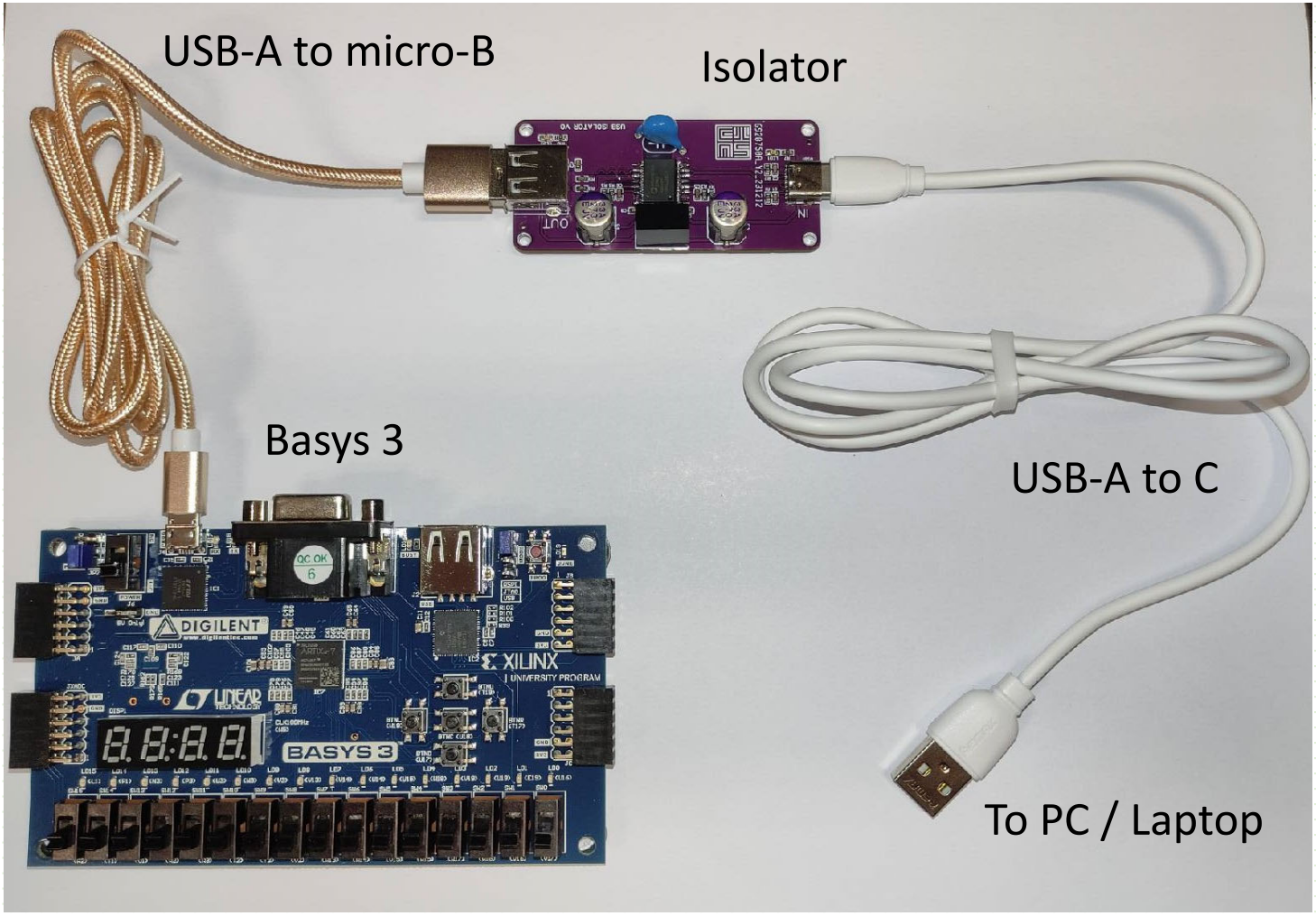
# 2D Briefing

| Week | | Task | Deliverable | % |
|---|---|---|---|---|
| Week 12 | 2D | project evaluation | in class demo, interview, accessible Github; | |
| | | | 15 min per group (10 min demo, 5 min q&a) | 25% |
| Week 13 | 2D | report submission | innovativeness | 10% |
| | | | education | 5% |
| | | | Total | 40% |

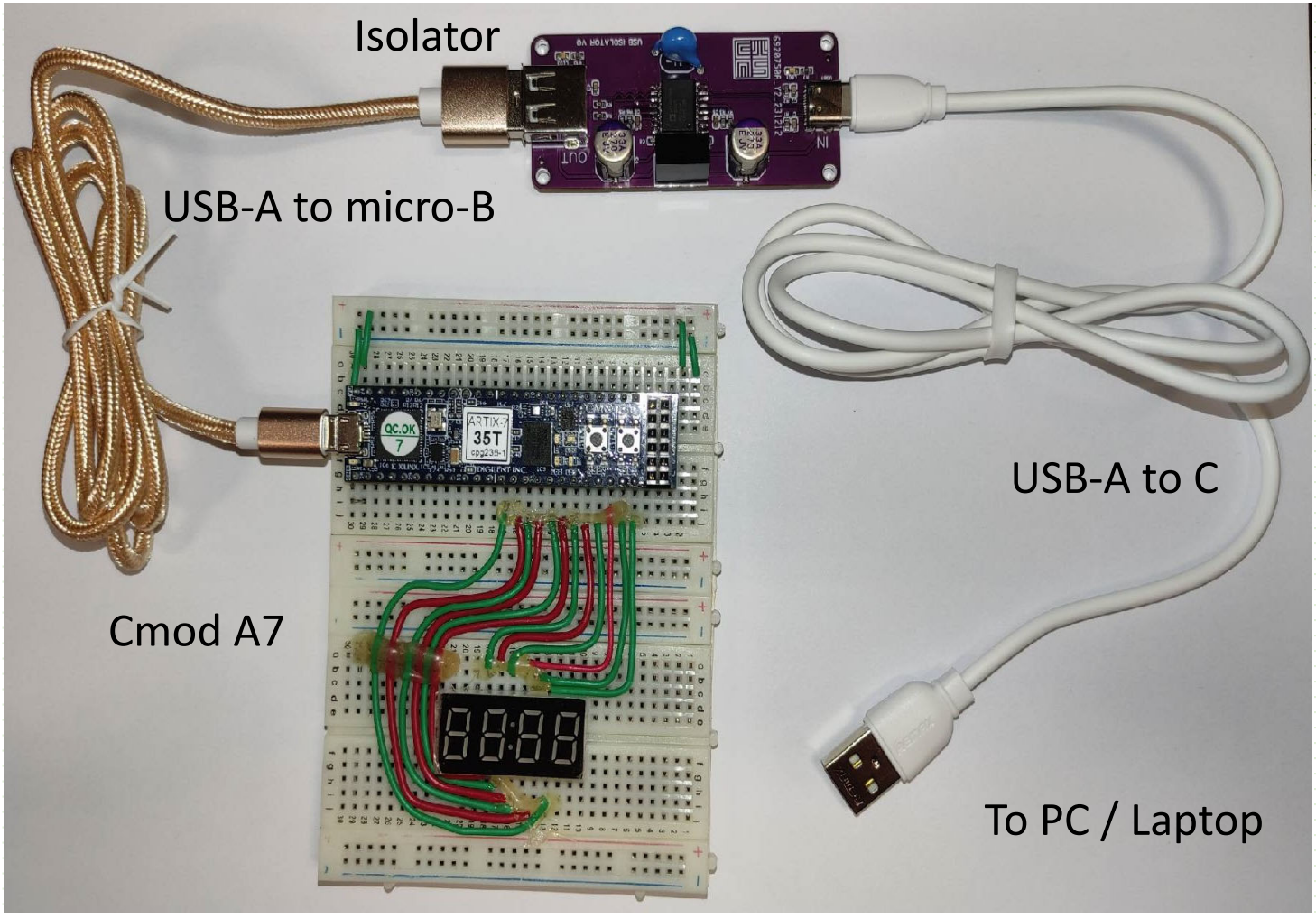
# FPGA Hardware Setup – Basys 3, Cmod A7

- Basys 3, Cmod A7 FPGA board x1
- Isolation board x1 (USB-C in, USB-A out): ***optional***
- Please prepare one USB cable (micro-B) to program the Basys 3 FPGA board
  - Example, USB-A – micro B (Charging & Transfer Cable)
  - If your laptop has USB-C only, you can use USB-C – micro B cable or through USB-C extension
  - Not all USB-A – micro B cable is working well with fpga board
    - Example, the USB-A – micro B from Daiso is working (sgd2.16)
  - *It is hard for lab to prepare the cables as different computer require different cable*

# FPGA Hardware Setup – Basys 3



# FPGA Hardware Setup – CMOD A7



# FPGA Software Setup - Vivado

- Register an account with Xilinx
  - You need this registration for download, and installation
- Download Vivado-design-tools
  - 2023.1
- Please refer to the below Guide for detail setup

https://pe8sutd.larksuite.com/docx/NfZid9uy5oiYvbxoEWMui94HsfY?from=from_copylink

# Handson – T01 (Basys 3-Group)

- Basys 3 – Logic Gates
- Group work: only one member needs to submit
- Please refer to his link for the handson instruction.

https://pe8sutd.larksuite.com/docx/W7yQdjBk1ohFT5xWEL2uvsfIsCb?from=from_copylink

# Handson – T02 (Basys 3-Group)

- Basys 3 - StopWatch
- Group work: only one member needs to submit
- Please refer to his link for the handson instruction.

https://pe8sutd.larksuite.com/docx/PTJudpWubouUNoxrNdzueuvNsIc?from=from_copylink

# Handson – T03 (CMOD A7-Group)

- CMOD A7 - StopWatch
- Group work: only one member needs to submit
- Please refer to his link for the handson instruction.

https://pe8sutd.larksuite.com/docx/QlTjdxNogoEYY0x4gdhu5hrBsEc?from=from_copylink

# Handson – T04 (CMOD A7-Group)

- CMOD A7 – PRNG (2D)
- Group work: only one member needs to submit
- Please refer to his link for the handson instruction.

https://pe8sutd.larksuite.com/docx/E9NldHApPoR0fBxAmoPuT3dtsmd?from=from_copylink