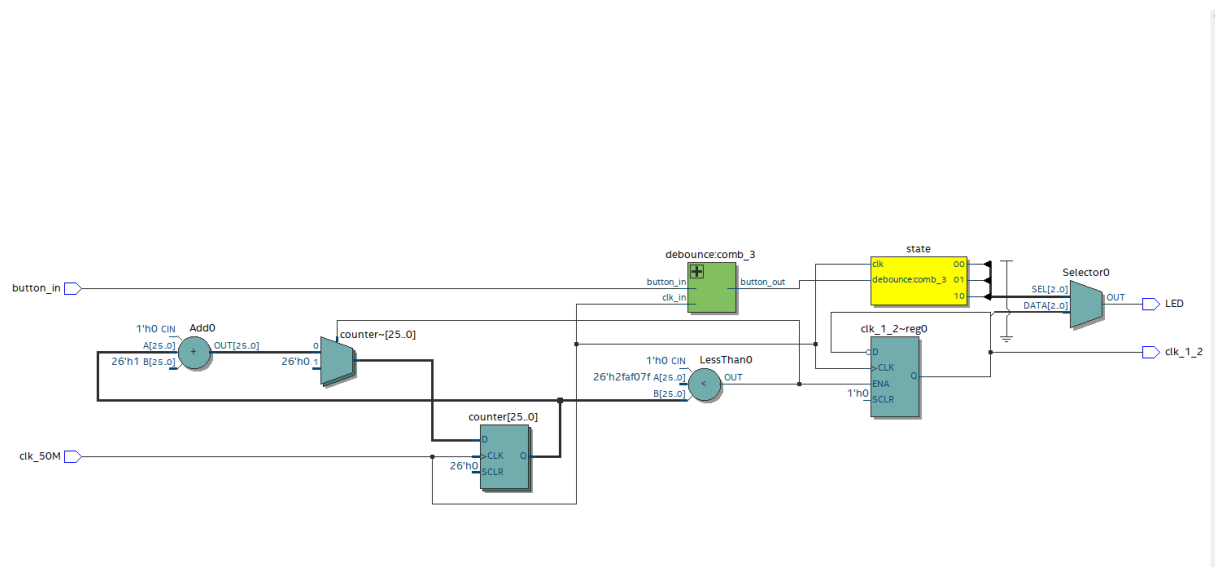


Lab#3 Sequential Circuit Design Using State Diagram

Code:

```
Quartus Prime Lite Edition - C:/Users/Imso2/OneDrive/Desktop/B0829002_Perlab3/B0829002_Perlab3 - B0829002_Perlab3
File Edit View Project Assignments Processing Tools Window Help
B0829002_Perlab3.v
Compilation Report - B0829002_Perlab3
debounce.v
267 268
EntityInstance
Cyclone IV E: EP4CE115F29C7
> perlab3
1 module perlab3(clk_50M, LED, button_in, clk_1_2);
2 input clk_50M, button_in;
3 output reg LED, clk_1_2;
4 wire button_out;
5 reg [1:0] state;
6 reg [25:0] counter;
7 debounce(clk_50M, button_in, button_out);
8 always @(posedge clk_50M) begin
9     if(button_out) begin
10         case(state)
11             2'b00: state<=2'b01;
12             2'b01: state<=2'b10;
13             2'b10: state<=2'b00;
14         endcase
15     end
16 end
17
18 always @(posedge clk_50M) begin
19     counter <= counter+1;
20     if(counter > 26'd50000000-26'd1) begin
21         counter <= 0;
22         clk_1_2 <= ~clk_1_2;
23     end
24 end
25 always @(*) begin
26     case(state)
27         2'b00: LED<=0;
28         2'b01: LED<=1;
29         2'b10: LED<=clk_1_2;
30         default: LED<=0;
31     endcase
32 end
33 endmodule
Tasks
Compilation
Task
> Compile Design
> Analysis & Synthesis
> Filter (Place & Route)
> Assembler (Generate program)
> Timing Analysis
> EDA Netlist Writer
> Edit Settings
Messages
Type ID Message
> 332148 Timing requirements not met
> 332146 Worst-case setup slack is -1.203
> 332146 Worst-case hold slack is 0.174
> 332140 No Recovery paths to report
> 332140 No Removal paths to report
> 332146 Worst-case minimum pulse width slack is -3.000
> 332102 Design is not fully constrained for setup requirements
> 332102 Design is not fully constrained for hold requirements
System (9) Processing (113) 100% 00:00:53
```

RTL-Design:



Pin planner:

Pin Planner - C:\Users\lms02\OneDrive\Desktop\B0829002_Perlab3\B0829002_Perlab3 - B0829002_Perlab3

File Edit View Processing Tools Window Help

Report

Report not available

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment
 - Export Pin Assignment
- Highlight Pins
 - I/O Banks
 - VREF Groups
 - Edges
- Clock Pins

Top View - Wire Bond
Cyclone IV E - EP4CE115F29C7

Named: * Edit: X

Node Name	Direction	Location	I/O Bank	VREF Group	Iter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	IOCT Preservation
LED	Output	PIN_G19	7	B7_N2	PIN_G19	2.5 V		8mA (default)	2 (default)		
button_in	Input	PIN_M23	6	B6_N2	PIN_M23	2.5 V		8mA (default)			
clk_1_2	Output				PIN_D24	2.5 V ...fault		8mA (default)	2 (default)		
clk_50M	Input	PIN_Y2	2	B2_N0	PIN_Y2	2.5 V		8mA (default)			
<<new node>>											

Difficult in this Lab:

I think the most difficult part in this lab is trying to write the “debounce.v” file to make the bottom signal stable. First of all, we need to know the frequency of CPU in FPGA board, to define a counter to count a mount of number for recognize the bottom was be pressed. After counting to this number, the board need to send a signal to make the other part of board know that there is a signal from bottom and make sure the signal is stable. Overall, the concept to stable signal is using counter to check the bottom was be pressed and using detected function to check the counter has counted a mount of number. After then send a stable signal to main.v.

Discussion:

In this Lab, we have to make a statement changing LED displayer, which is get the bottom signal and change the state, that are off, on, and shinnying. And the bottom signal must be filtered by “debounce.v” and we need to using mux to select the state, which the LED display mod will be showed.