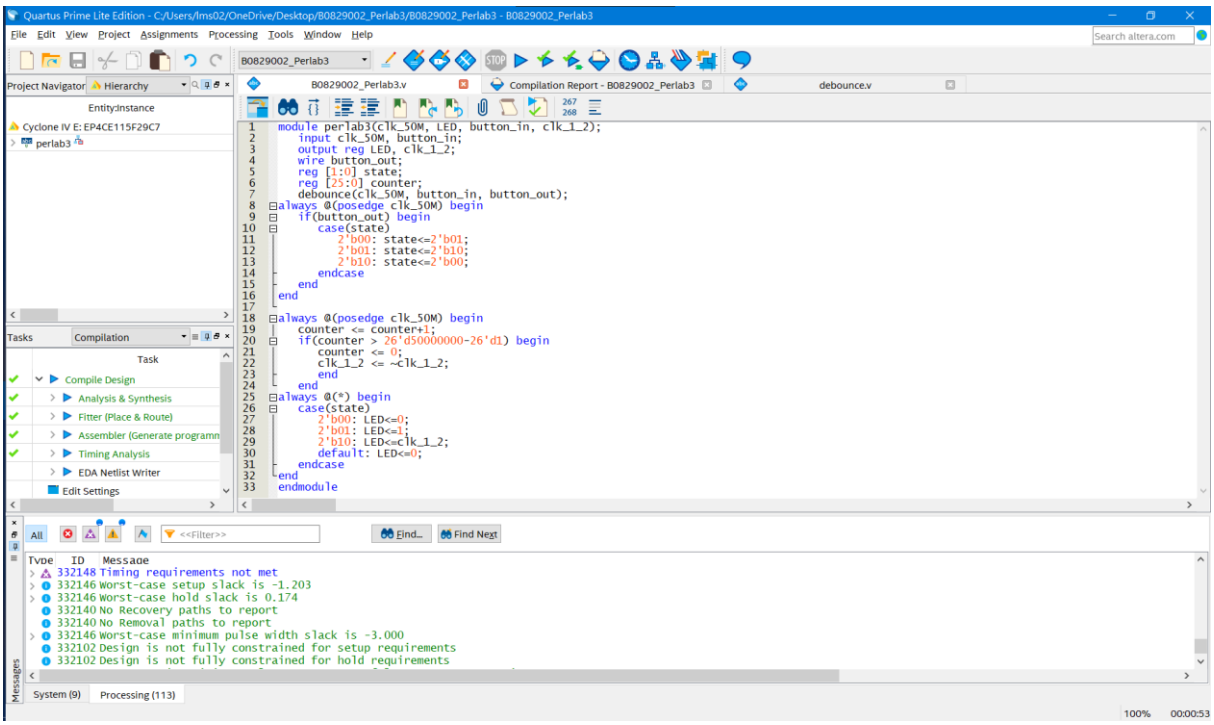
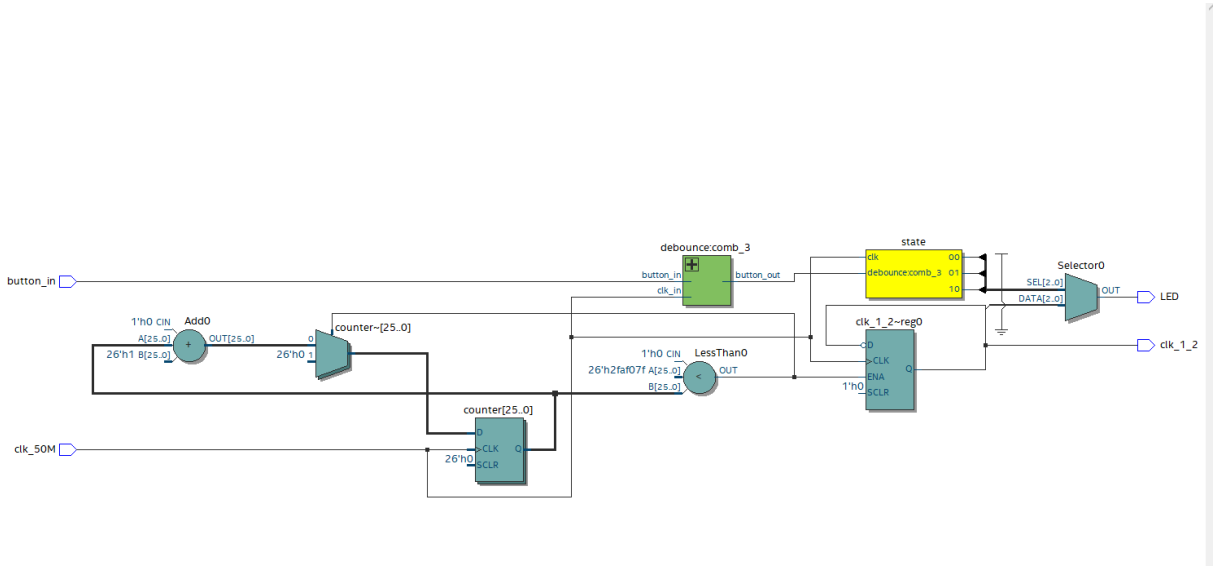
Lab#3 Sequential Circuit Design Using State Diagram

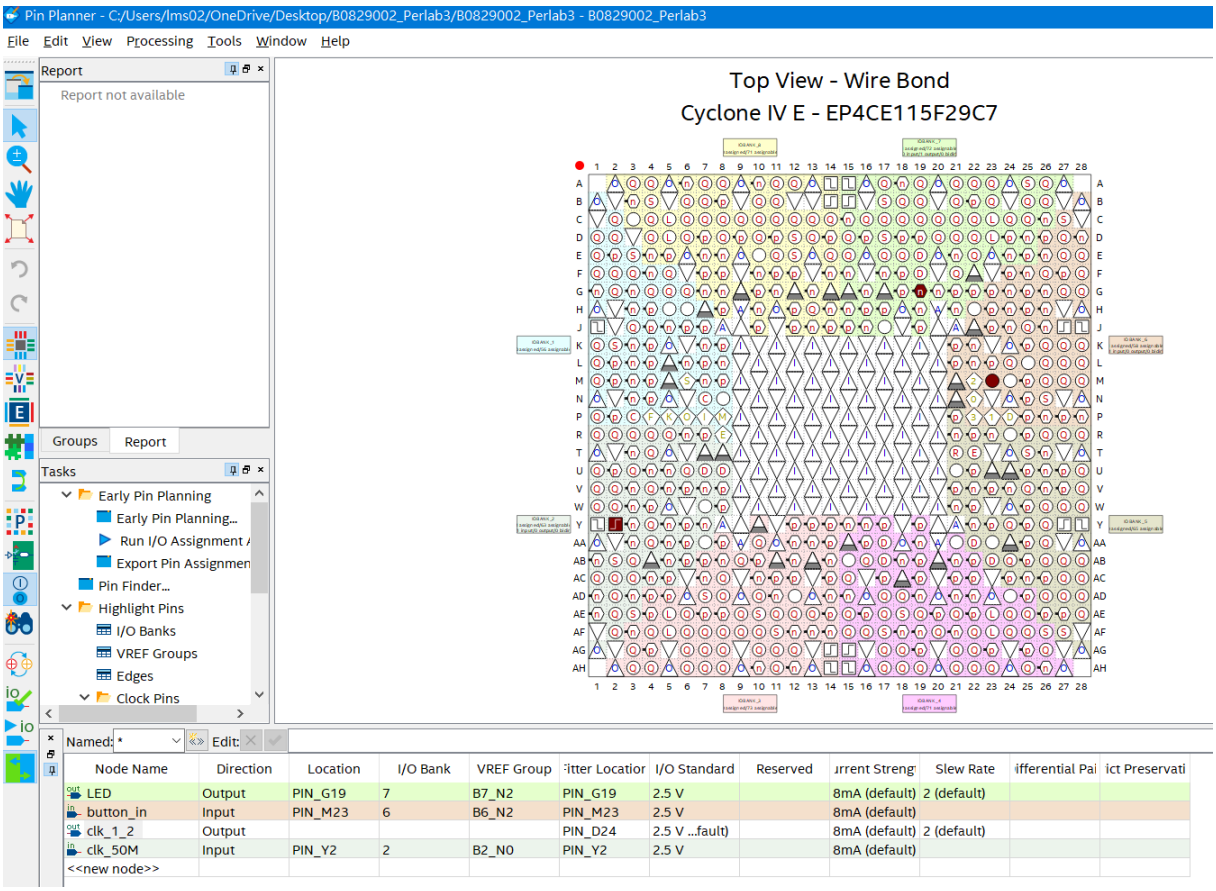
Code:



RTL-Design:



Pin planner:



Difficult in this Lab:

I think the most difficult part in this lab is trying to write the “debounce.v” file to make the bottom signal stable. First of all, we need to know the frequency of CPU in FPGA board, to define a counter to count a mount of number for recognize the bottom was be pressed. After counting to this number, the board need to send a signal to make the other part of board know that there is a signal from bottom and make sure the signal is stable. Overall, the concept to stable signal is using counter to check the bottom was be pressed and using detected function to check the counter has counted a mount of number. After then send a stable signal to main.v.

Discussion:

In this Lab, we have to make a statement changing LED displayer, which is get the bottom signal and change the state, that are off, on, and shinnying. And the bottom signal must be filtered by “debounce.v” and we need to using mux to select the state, which the LED display mod will be showed.