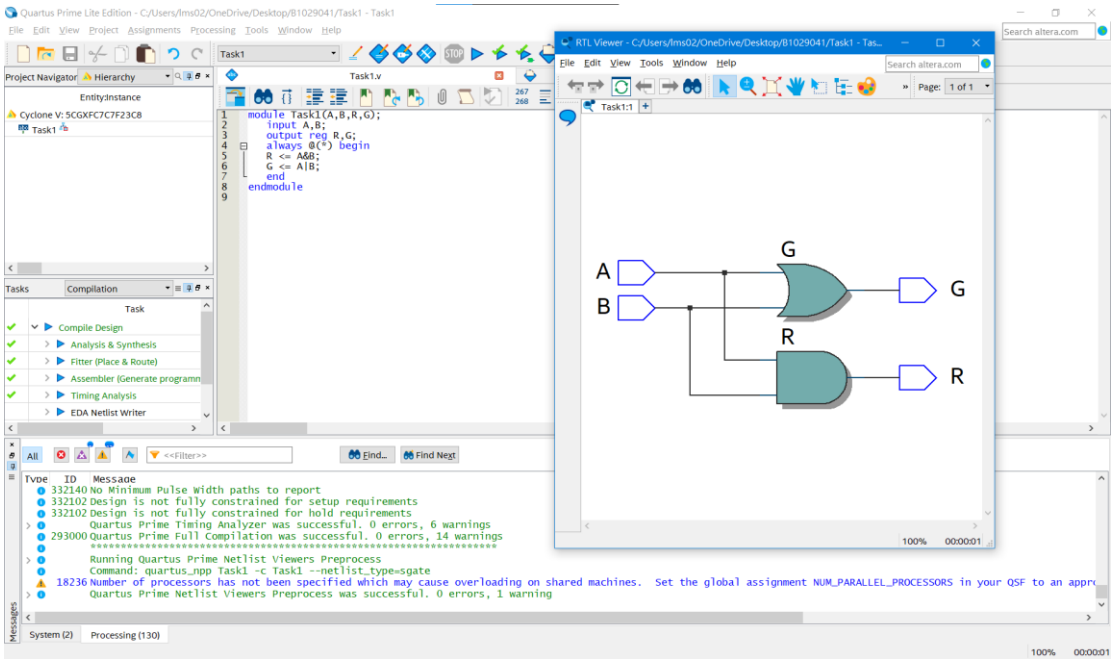
Perlab02 B0829002

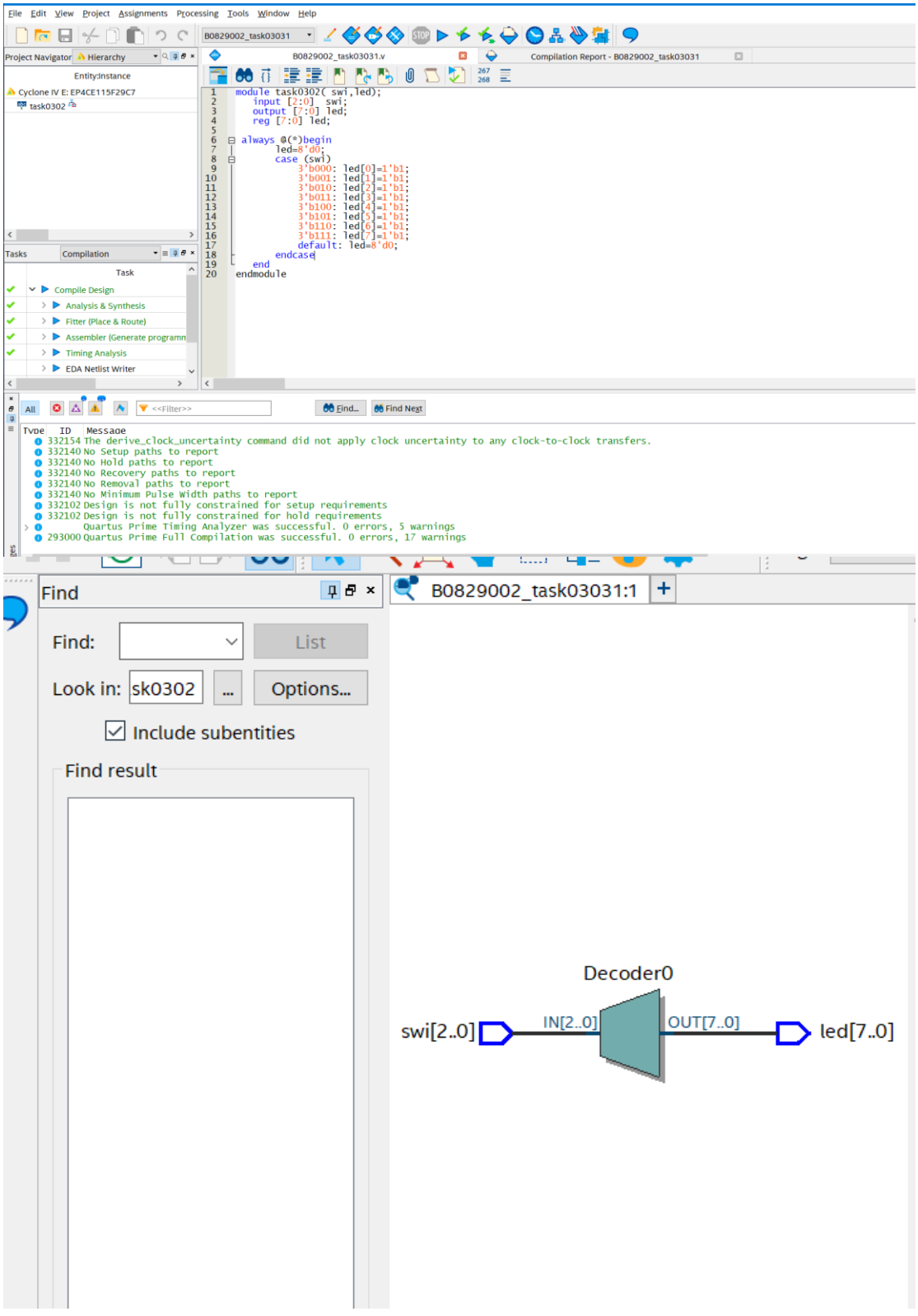
Task 01:

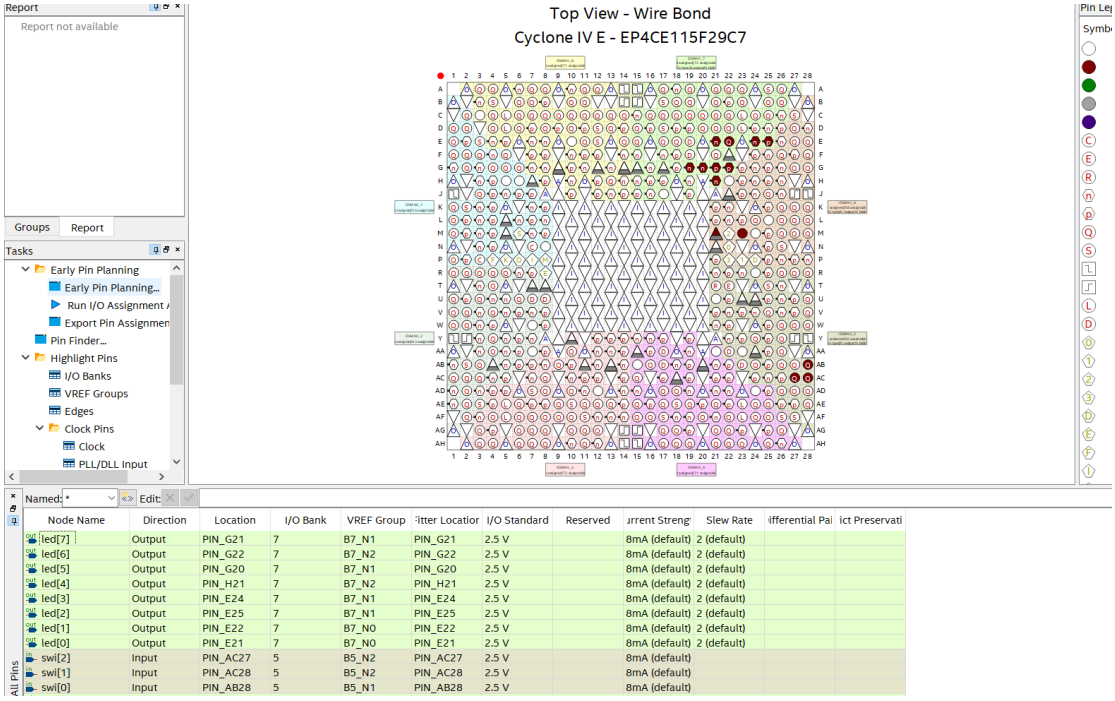
In this task we need to make a combinational circuit, that will use the and gate and or gate to show result of 2 button inputs, and the Verilog code module will be always determine the inputs.



Task 02:

This task will use a decoder to recognize the input value of 3-bits binary number and the different output will lead them to the specific 8 LED lights. In the task will use switch and this module determines also always.

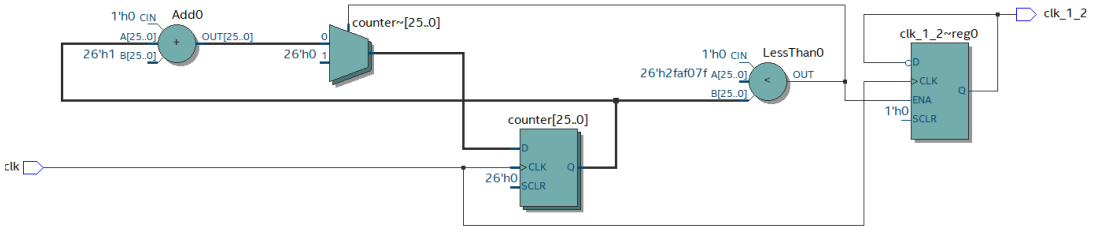

File Edit View Project Assignments Processing Tools Window Help
B0829002_task03031
Project Navigator Hierarchy
Entity:Instance
Cyclone IV E: EP4CE115F29C7
task0302
B0829002_task03031.v
Compilation Report - B0829002_task03031
module task0302(swi,led);
input [2:0] swi;
output [7:0] led;
reg [7:0] led;
always @(*)begin
led=8'd0;
case (swi)
3'b000: led[0]=1'b1;
3'b001: led[1]=1'b1;
3'b010: led[2]=1'b1;
3'b011: led[3]=1'b1;
3'b100: led[4]=1'b1;
3'b101: led[5]=1'b1;
3'b110: led[6]=1'b1;
3'b111: led[7]=1'b1;
default: led=8'd0;
endcase
end
endmodule
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
Timing Analysis
EDA Netlist Writer
All
<<Filter>>
Find...
Find Next
Type ID Message
332154 The derive_clock_uncertainty command did not apply clock uncertainty to any clock-to-clock transfers.
332140 No Setup paths to report
332140 No Hold paths to report
332140 No Recovery paths to report
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 17 warnings
Find
Find:
List
Look in: sk0302
...
Options...
Include subentities
Find result
B0829002_task03031:1
Decoder0
swi[2..0]
IN[2..0]
OUT[7..0]
led[7..0]

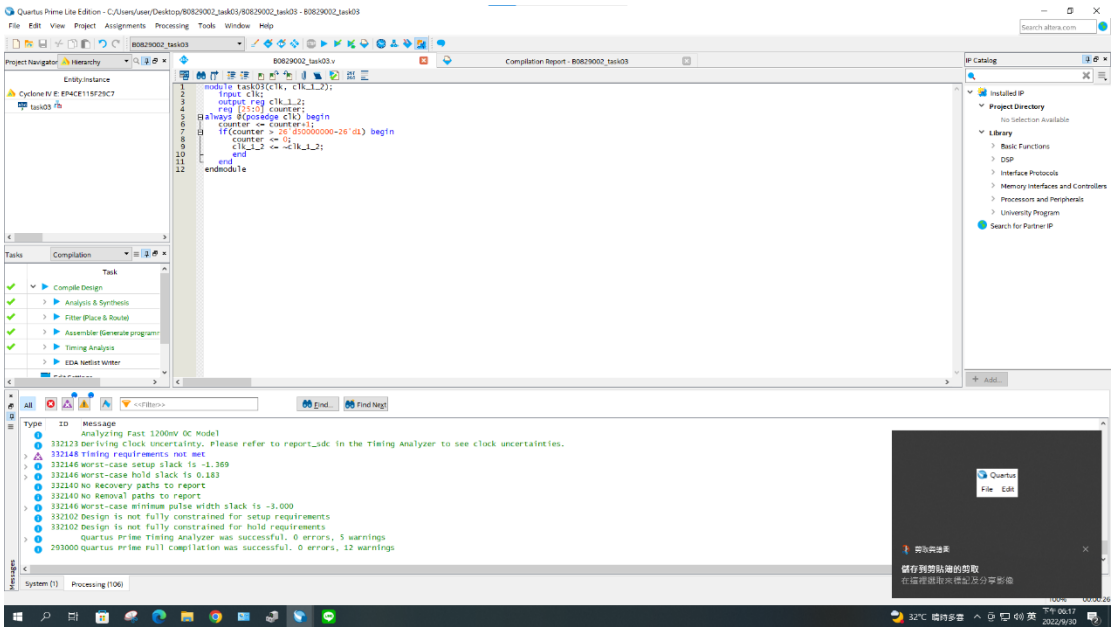


Node Name	Direction	Location	I/O Bank	VREF Group	itter Locatior	I/O Standard	Reserved	urrent Streng	Slew Rate	ifferential Pai	ict Preservati
led[7]	Output	PIN_G21	7	B7_N1	PIN_G21	2.5 V		8mA (default)	2 (default)		
led[6]	Output	PIN_G22	7	B7_N2	PIN_G22	2.5 V		8mA (default)	2 (default)		
led[5]	Output	PIN_G20	7	B7_N1	PIN_G20	2.5 V		8mA (default)	2 (default)		
led[4]	Output	PIN_H21	7	B7_N2	PIN_H21	2.5 V		8mA (default)	2 (default)		
led[3]	Output	PIN_E24	7	B7_N1	PIN_E24	2.5 V		8mA (default)	2 (default)		
led[2]	Output	PIN_E25	7	B7_N1	PIN_E25	2.5 V		8mA (default)	2 (default)		
led[1]	Output	PIN_E22	7	B7_N0	PIN_E22	2.5 V		8mA (default)	2 (default)		
led[0]	Output	PIN_E21	7	B7_N0	PIN_E21	2.5 V		8mA (default)	2 (default)		
swi[2]	Input	PIN_AC27	5	B5_N2	PIN_AC27	2.5 V		8mA (default)			
swi[1]	Input	PIN_AC28	5	B5_N2	PIN_AC28	2.5 V		8mA (default)			
swi[0]	Input	PIN_AB28	5	B5_N1	PIN_AB28	2.5 V		8mA (default)			

Task 03:

This task is a little bit different with the last 2 tasks. This task needs to use the clock to turn the output lighting every second on and off, thus we need to check the frequency of the cpu in the FPGA plate. And then we have to calculate the clock ticks per second is $5*10^7$ times per second, so we need a counter to record the clock ticks and make sure the clock ticks will be reset to 0 after 5*10^7 and the output will be complement.





After this lab, I have learned a lot of thing about sequential circuit and the using about clock. In the first task, we finish a simple combinational circuit using AND and OR gates, that trained me to setting the pin on FPGA Plate. And the second task is to make a 3x8 decoder using switch to input signals and we need to plan more pin for the led output and switch inputs. The third task, which I think is the most difficult task in this lab, is using the clock to make a sequential circuit with a output led lighting, which complement the value each second. In this task, the part full of challenge is to divide the clock from 5*10^7 to 1 per second, thus we need a counter to count the ticks after each clock trigger ,and after 5*10^7 times the counter will be reset and the output signal will also be complemented.