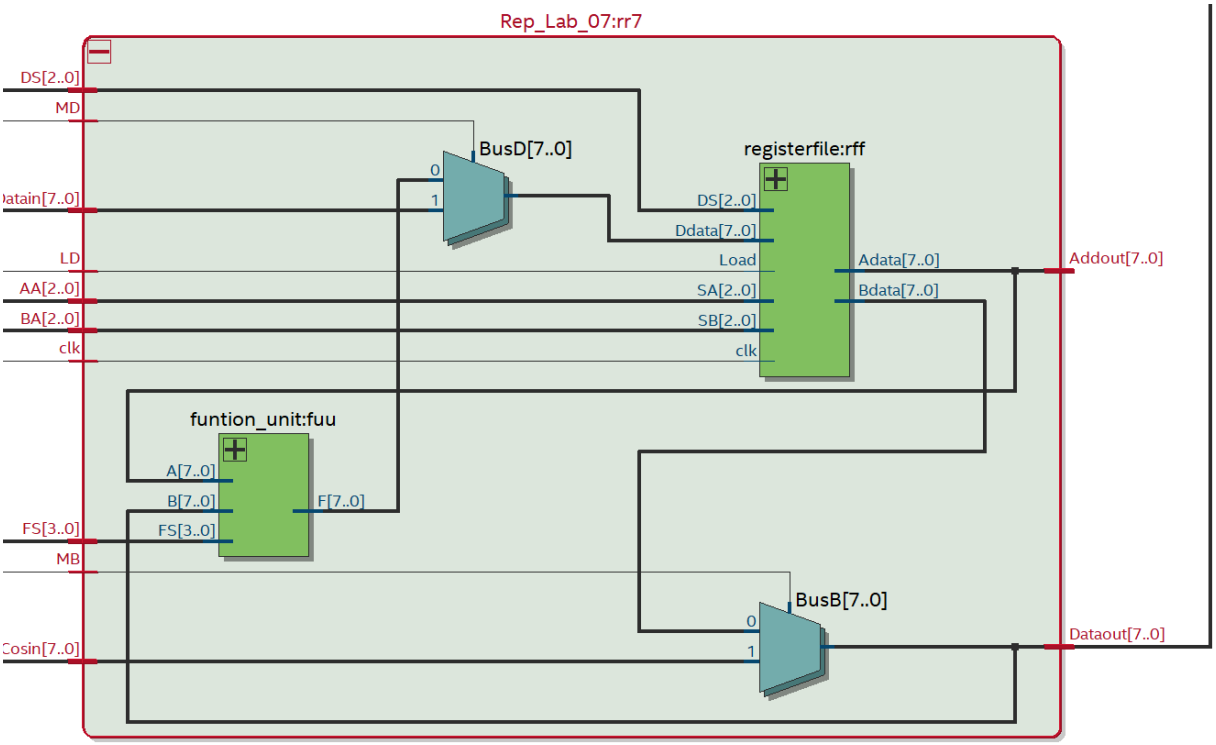
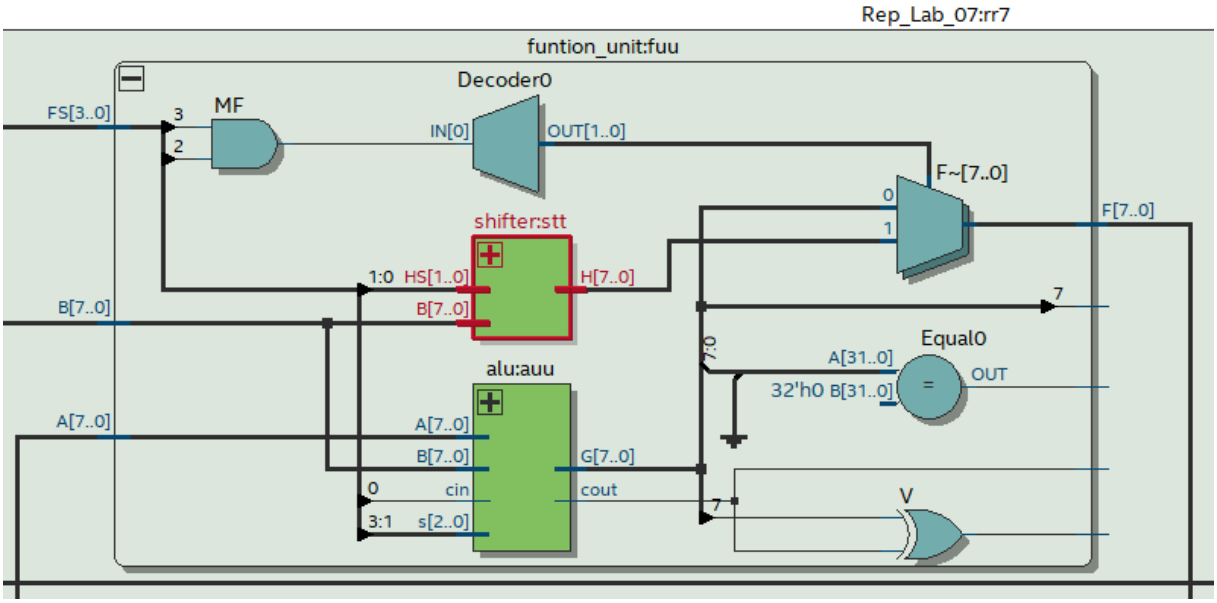
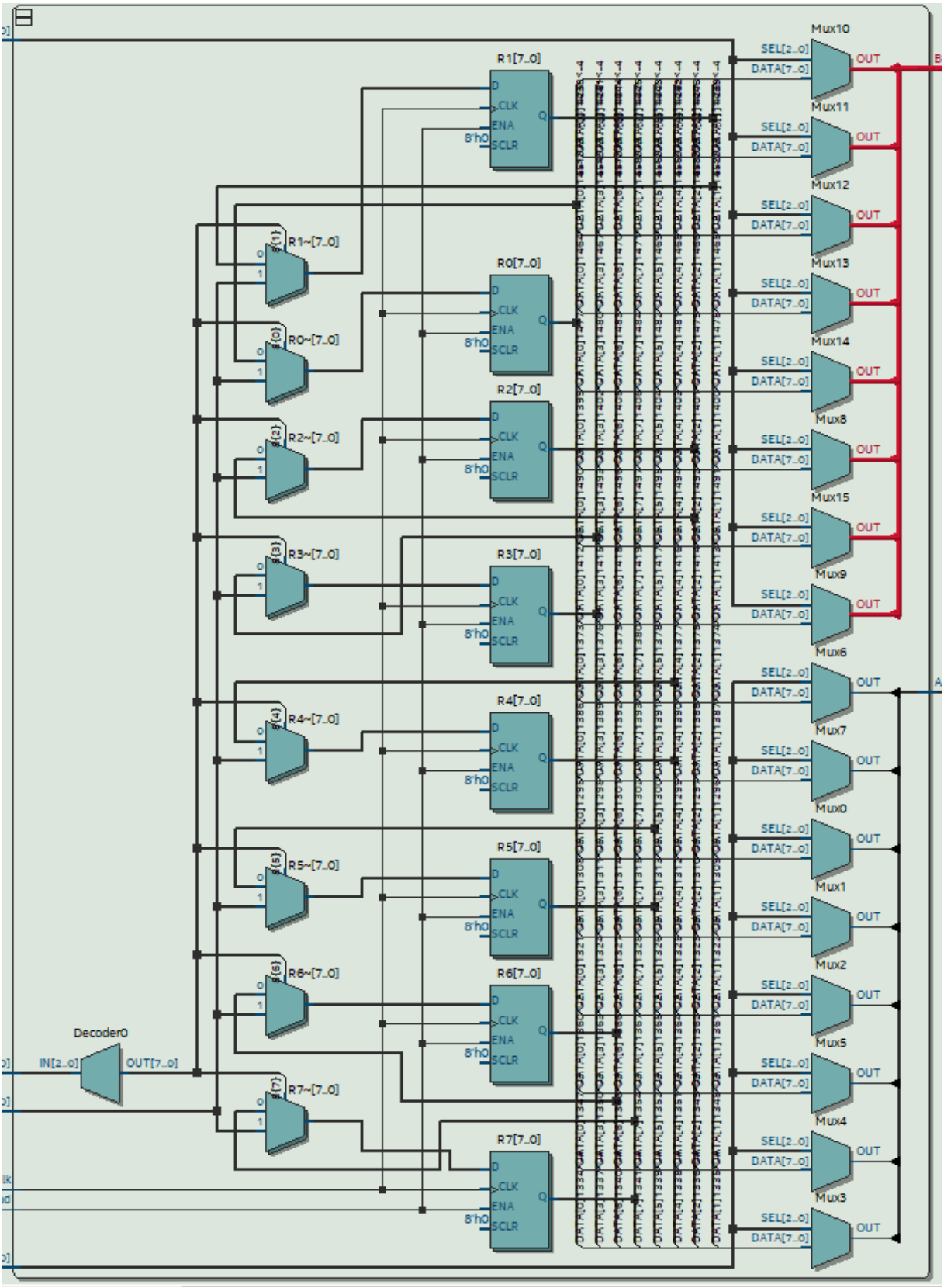
Rep_Lab07_B0829002

In this Lab, we are going to make a Datapath to make sure the Simple computer can do operation without branch.

RTL view:






Mux10
Mux11
Mux12
Mux13
Mux14
Mux8
Mux15
Mux9
Mux6
Mux7
Mux0
Mux1
Mux2
Mux5
Mux4
Mux3
SEL[2..0]
DATA[7..0]
OUT
R1[7..0]
R0[7..0]
R2[7..0]
R3[7..0]
R4[7..0]
R5[7..0]
R6[7..0]
R7[7..0]
D
CLK
ENA
SCLR
Q
8'h0
R1~[7..0]
R0~[7..0]
R2~[7..0]
R3~[7..0]
R4~[7..0]
R5~[7..0]
R6~[7..0]
R7~[7..0]
Decoder0
IN[2..0]
OUT[7..0]

In this task, we need the ALU from LAB06 and a registerfile, function_unit with shifter and ALU inside.

In the registerfile, we need to use a decoder to decode the destination, which register the value will load in. And A Select and B Select are going to select the signal to send signal to the BusA and BusB.

In Funtion_unit, we need to do operation with ALU and shifting and also we cannot use registers inside.

The most important part I thought was MUXB and MUXD because this 2 multiplexer have the most important task to select the value from branch control and memory address.

In this Task, I met a lot of problem, such as some file didn't import or and some wrong messages, which need to deal with. For dealing with this problem, I have to thank TA and Professor a lot because they deal with these problems with me until quite late night.

In this lab, I learn how to construct a simple computer datapath with some Function operation. In my opinion, this lab is quite important for students in CSIE to learn how simple computer work that can make me know more about the construction of computers and how can I design my operation for my simple computer.