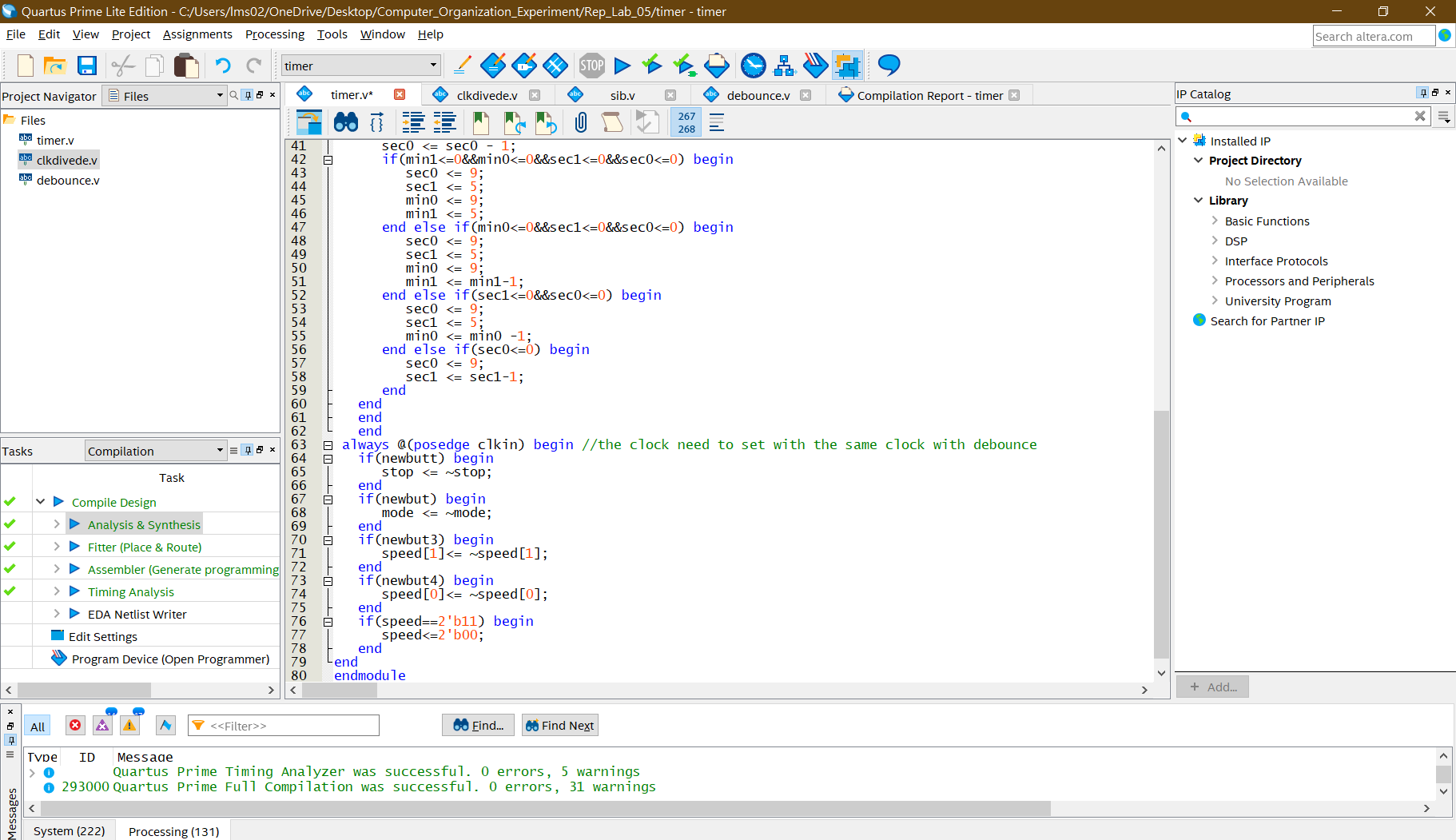
Lab 5 Sequence and Control; Digital clock design

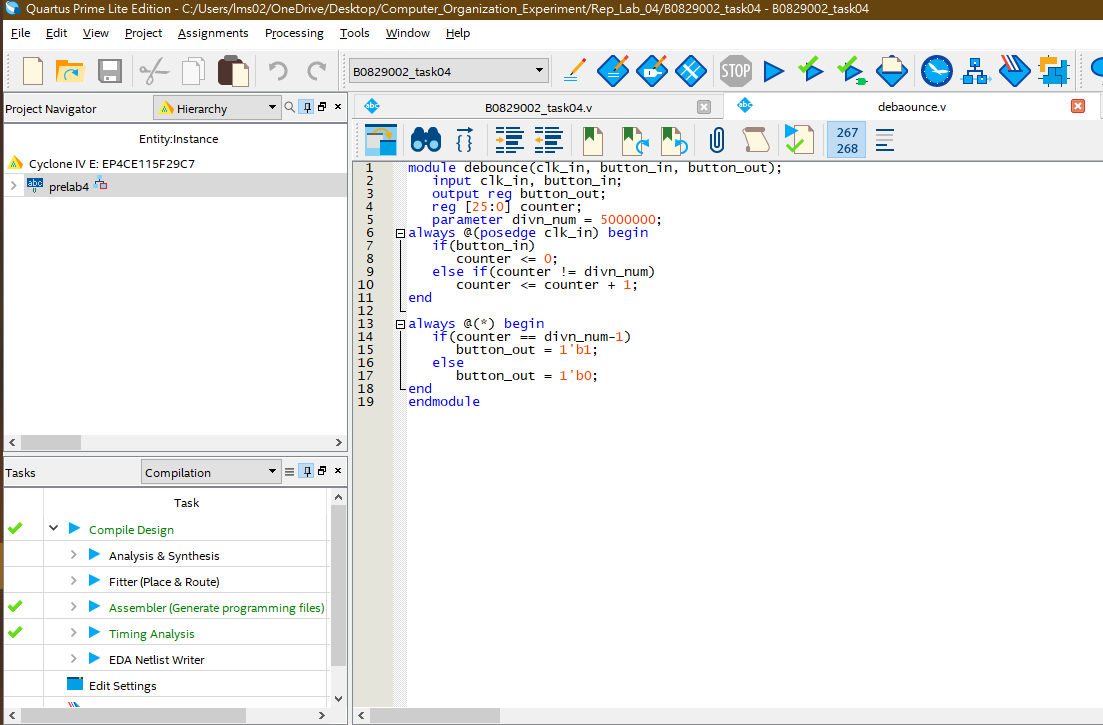
Description:

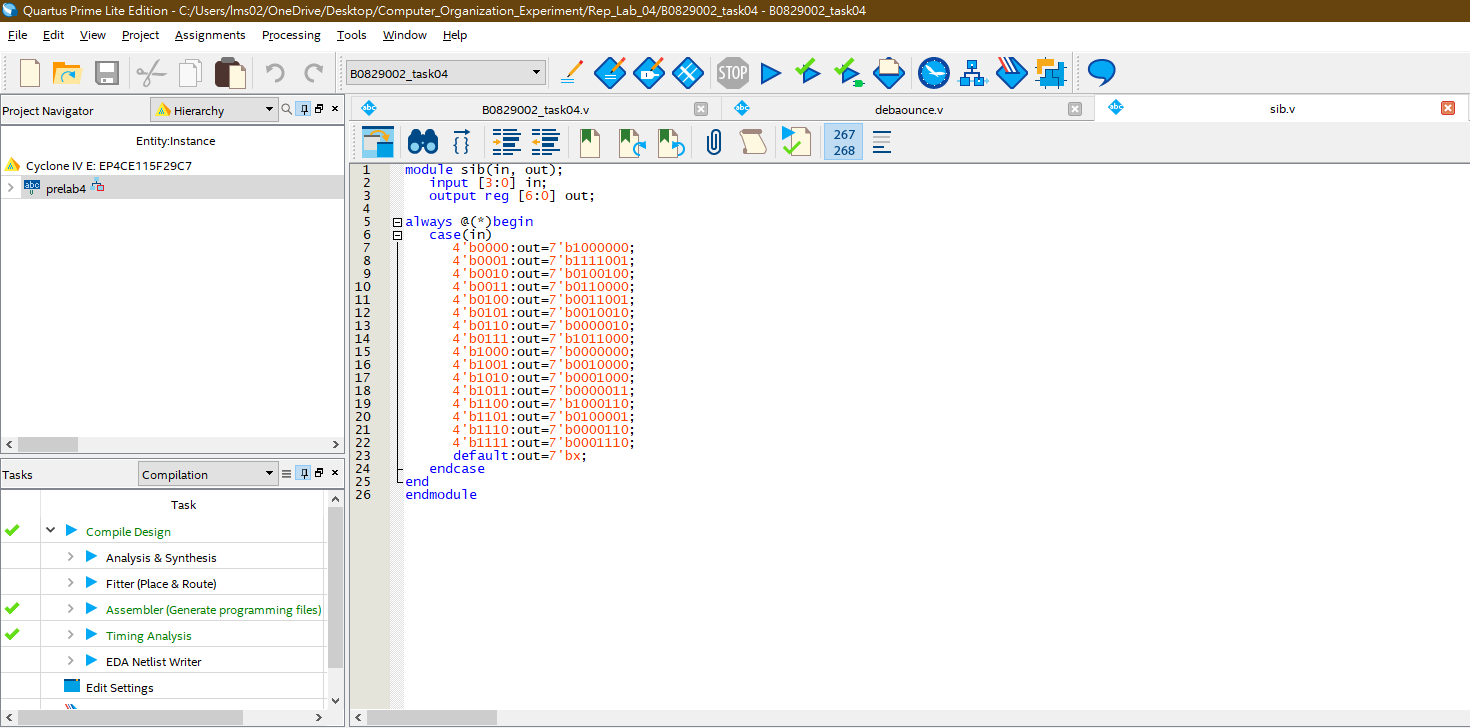
In this lab, we are going to make a timer, which has a lot of function to make it count faster, slower, count up, and count down. Furthermore, we also need a button to make the timer stop and start.

Code:

一張含有 文字 的圖片

自動產生的描述



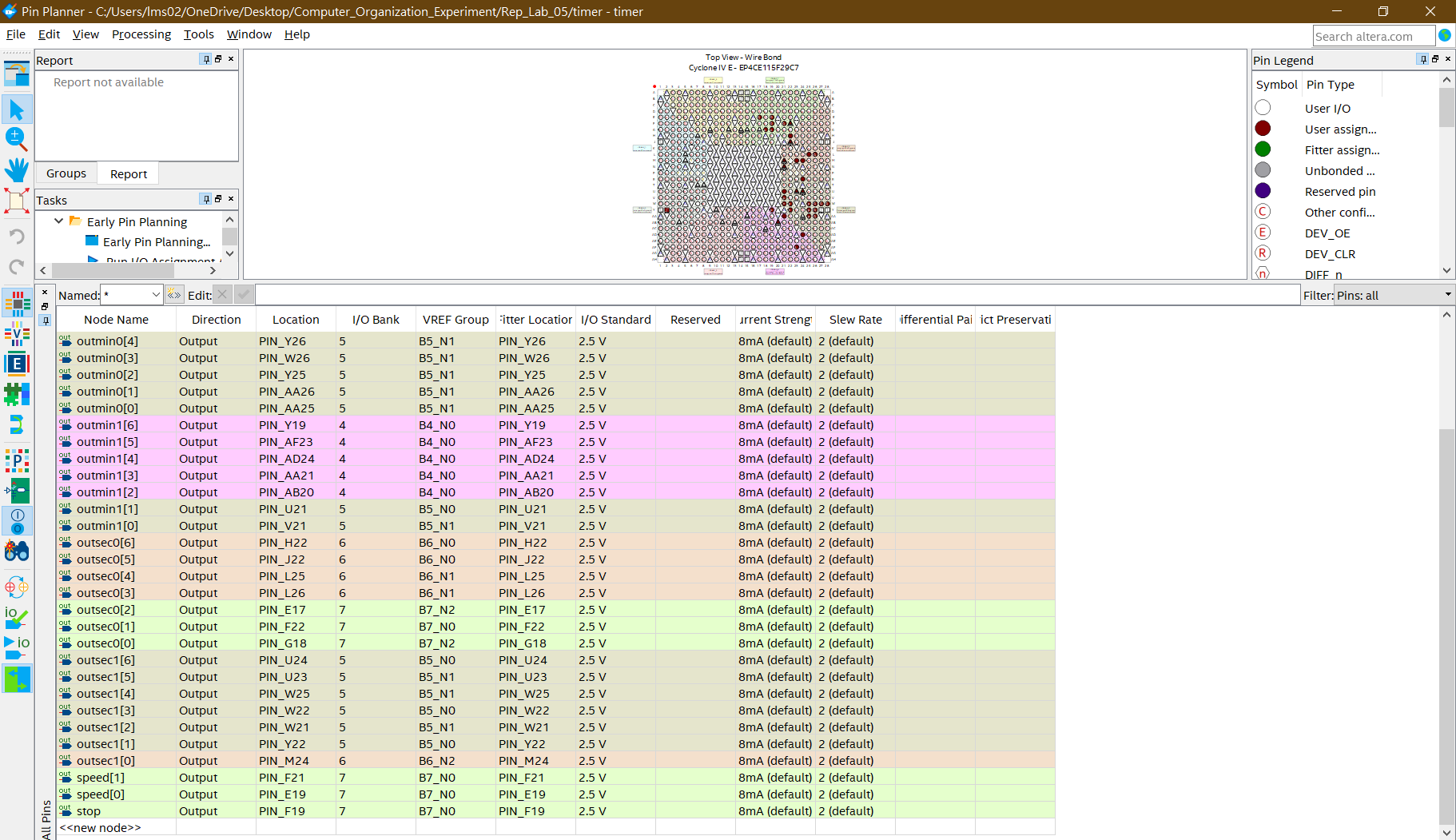


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自動產生的描述

RTL Design:



Pin planer:

Explanation:

For count up, we just determine count to 9+1 or 5+1 need the back signal reset to zero and the next signal add 1. For counting down, we use another method to determine when it count to 0-1 and the back signal will reset to 9 or 5. And the front signal will minus 1.

If we need to use start and stop, it is easy to use control unit to achieve the action. We can use a if-else determination when stop==1, then the timer stop to count and stop ==0, the timer start counting.

Discussion for difficulties and problems:

Last but not least, when we face to the speed of counting, we can divide the clock trigger to achieve the faster 2x or 0.5x times (using n-bit counter or module-n counter), then we also using the control unit (if-else statement) to control the state of speed.

The most difficult problem I met is, when I using the different clock trigger for state determination and changing, it will happen that the trigger of clock for state changing and debounce.v is different, thus the state will not change. It also lead to most of control unit can not take action because when the clock trigger the state of button has changed and there is no clock trigger or different signal yet.

Therefore, the solution is using the same clock for all of the non-blocking function.