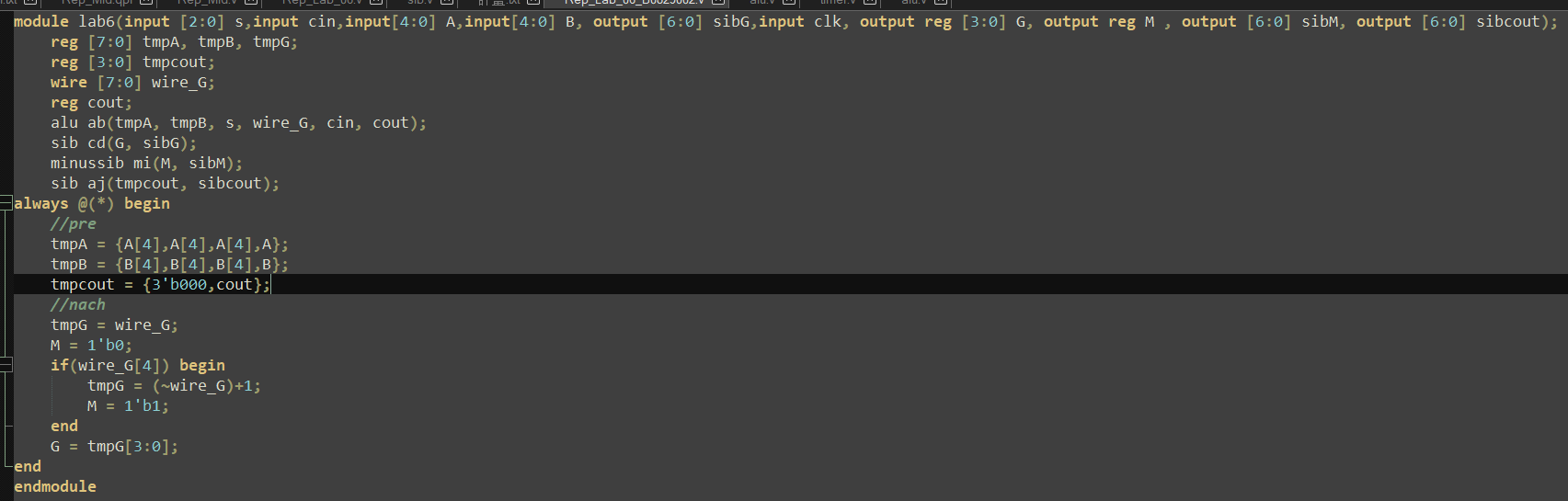
Pep\_Lab\_06

In this Task, we’re going to design an ALU module and write a test module for FPGA borad.

一張含有 文字 的圖片

自動產生的描述



In this design, we cannot use any register or latch for the ALU module, thus only one way we can store value is write in the test module and send it to the seven segment v file to render out the LED light.

The most difficult part I thought was let the mux do not generate a latch because when we didn’t set the all case for determination in multiplexer, after compiling this module will generate a latch to store the status, which was undefined.

After finished this task, I learned how to design a ALU module with high-efficient way and how to combine 2 different part of module with the best way. I think that will be quite helpful for the next task to demonstrate a simple computer design.