mcrb synthesis and timing

mcrb.v is RTL code for a small sequential circuit. The top-level is “mcrb”. There is only one clock, and its source is the input port “mc_rb_ef1_sclk_i”. You will synthesize mcrb with the Skywater “HS” library.

(i) Invoke Genus

(ii) Read “mcrb.v” and the standard cell library’s Liberty file for the P-V-T corner ss, 150 °C, 1.6V.

(iii) Elaborate mcrb and synthesize to generic gates (“gcells”). Write out the gcell-based netlist.

(iv) Define a clock called “sclk” using the “create_clock” command. The clock source is indicated above. The clock frequency should be 200 MHz.

(v) Continue the synthesis with mapping to the standard cell library followed by optimization. Export the gate-level netlist and optimization.

(vi) What is the instance count and total cell area? You can use the “report_area” command.

(vii) What Genus tcl commands would you use to report the count of input ports and output ports? Run these commands and generate the port counts.

(viii) Report the “top path”, i.e, the timing path with the minimum setup skew, using the report_timing command.

a. What are the startpoint and the endpoint of the timing path?

b. How many combinational cells are in the timing path, and what is the total combinational cell path delay? Do not include any clock-to-Q delay in the combinational path delay.

c. What is the instance name and cell type of the combination cell with the largest delay in the path?

d. What is the highest drive strength of any cell in the timing path?

e. What is the clock-to-Q delay at the startpoint and the setup time at the endpoint?

f. The setup slack will be positive. How much is it?

(ix) If you were to change the clock frequency, to what value would you have to change it to start seeing paths with negative slack? This is without running an additional optimization.

(x) Generate a table indicating instance count and area versus frequency, going from 200 MHz up to 1 GHz in steps of 50 MHz. Write a tcl script to do this in which you use a “for” loop to change the frequency, optimize, and report area.

Constraining I/O paths

Report timing from the input port mc_rb_fuse_vld_i. Force the timing to be reported even if paths from this input port are unconstrained. What is the endpoint of the “top” reported path?

Find the count of endpoints from the input port mc_rb_fuse_vld_i, using the “all_fanout -endpoints_only” command.

Write a script that tabulates the count of endpoints from each input port except the clock input. Submit the script and the output table.

Create a collection of all inputs except the clock input. Constrain timing paths from all these inputs using the “set_input_delay” command, and set the input delay to half the clock period. Resynthesize with paths from input ports so constrained, and with clock period set to 800 MHz. By how much does the instance count and cell area change?