



Start point :skew\_addr\_cntr\_reg[0]/Q (^) triggered by leading edge of 'sclk'

End point : skew\_addr\_cntr\_reg[0]/D (v) checked with leading edge of 'sclk'

|                                |          |
|--------------------------------|----------|
| clock-to-Q delay of startpoint | 0.438 ps |
| hold timing of endpoint        | 0.011 ps |

transition time at outputs of all cells

| Cell                  | Slew (ps) |
|-----------------------|-----------|
| skew_addr_cntr_reg[0] | 0.120     |
| skew_addr_cntr_o[0]   | 0.120     |
| g468__8428            | 0.023     |
| n_10                  | 0.023     |