# Jagadeesh Pradhani

## ELECTRICAL & ELECTRONICS ENGG.

Skilled Electrical & Electronics Engineering student with a passion for Digital VLSI, Computer Architecture, and Design for Test (DFT). Proficient in DFT methodologies like scan-based testing and fault modeling and experienced in GEM5 for architecture simulation . Hands-on with Tessent for scan insertion, Cadence Genus for synthesis, and Tempus for timing analysis. Strong understanding of scan chains, ATPG, fault detection, and testability enhancement, ensuring efficient chip validation.

## CONTACT


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## EDUCATION

2022-2025
B.E Electrical & Electronics Engineering
CGPA : 8.35
K L E Technological University - HUBLI

2019-2021
P U C Science (93%)
Sukruti PU science College-HUBLI

2019
SSLC (86%)
Sukruti Public School - HUBLI

## SOFT SKILLS

- Problem Solver
- Creative Mindset
- Quick Grasper Adaptivity
- Good listener
- Communication
- Manager
- Team Player

## LANGUAGES

- Kannada(first language)
- English
- Hindi

## EXPERIENCE

**01/2025 - Present**
Intern @ Centre for Integrated Circuits and Systems

### DFT Intern

- Implemented scan-based test architectures using Tessent, Genus, and Tempus.
- Optimized TCL scripting for Cadence tools.
- Enhanced scan chain design to improve fault coverage and streamline testing.

**01/2024 - Present**
Fiverr- Freelancer - online

### GEM5 DEVELOPER

- Created and customized various GEM5 simulations for clients, including complex cache memory architecture.
- Cache coherence protocol implementation for increased Hit rates in CPU.
- Memory Management and power analysis of custom coherence protocols.

## CERTIFICATIONS

ICDCOT & CONIT 2024 IEEE conference.
Cadence Training DFT Fundamentals course
Aerothon-2023 from SAE-India

## CAREER OBJECTIVES

- To solve problems in an effective/creative manner in a challenging position.
- Seeking a responsible job with an opportunity for professional challenges

## ACHIEVEMENTS & PUBLICATIONS

- **AIR #1** in **SAE India's ADC(2022), AIR #2** in **ADDC** & **AIR #4** in **Aerothon(2023)**
- **Prototype Development for Water Leakage Monitoring System with RTOS Implementation** presented at ICDCOT-2024.
- **Autonomous Detection of Landing Pad in Challenging Terrains for Precise Aerial Supply** presented at the CONIT-2024 conference.

## TECHNICAL SKILLS

- **DFT & Verification Tools:** Tessent, Cadence Genus, Tempus, Virtuoso, Yosys, OpenSTA.
- **FPGA & Hardware Simulation:** Xilinx vivado, MATLAB.
- **Computer architecture :** ChampSim, Gem5.
- **Operating System :** Windows, Linux (RHEL, Ubuntu).
- **Programming Language :** Verilog, SystemVerilog, C, C++ ,Python.
- **Scripting :** TCL, bashScript
- **Others :** MS office

# Projects

## DFT Analysis on s298 benchmark

I conducted DFT analysis on the **s298 benchmark**, implementing **scan chain** insertion and **fault** modeling techniques using industry-standard tools. Synthesized the design with **Genus**, performed timing analysis with **Tempus**, and evaluated fault coverage and test efficiency, optimizing design modifications with **Tessent** for enhanced reliability.

## TCMP ARCHITECTURE ANALYSIS

Implemented stride prefetching using a **tiled chip multi-core** processor on the **GEM5** simulator to explore **cache optimization techniques**. Analyzed performance metrics such as hit ratio, miss rate, and prefetcher block placement, enhancing memory access efficiency in multi-core systems

## CMOS LAYOUT DESIGN

Designed a 2:4 line decoder using **CMOS** and **Pseudo NMOS** logic in **Cadence Virtuoso**. Conducted transient analysis to verify output performance, showcasing proficiency in digital circuit design and layout implementation

## RISC-V MIPS 5-STAGE PIPELINED SOC DESIGN

Developed a **RISC-V MIPS 5-stage pipelined System on Chip (SoC)** using **Verilog in Cadence Virtuoso**. The project involved designing and implementing the pipeline architecture, coding in Verilog, and performing extensive simulations to verify functionality and performance. This work demonstrated my ability to manage complex digital design projects, optimize pipeline stages for efficiency, and utilize Cadence tools for comprehensive SoC development and analysis.

## TARGET DETECTION & LOCALIZATION [Publication]

I authored a **machine learning** paper detailing a novel technique for the **autonomous detection** of landing pads in challenging terrains, crucial for **precise aerial supply** operations. Implemented and validated this technique in real-time scenarios, demonstrating its effectiveness in practical applications. Published **IEEE paper** in **CONIT-2024**

## RTOS BASED WATER LEAKAGE DETECTION SYSTEM [Publication]

As the lead designer, I spearheaded the development of an innovative RTOS-based water leakage detection system, leveraging the capabilities of an **Arm Cortex M3** board to ensure efficient and reliable performance. Published **IEEE paper** in **ICDCOT-2024.**