

VLSI/FPGA Projects Using Intel DE10-Lite

Beginner-Level FPGA Projects

- 4-bit ALU Design on FPGA

Design and implement a 4-bit ALU in Verilog, simulate using ModelSim, and display output via LEDs on DE10-Lite.

- Traffic Light Controller using FSM

Use a Finite State Machine modeled in Verilog to simulate a smart traffic light system on DE10-Lite.

- Digital Thermometer with ADC Interface

Interface an LM35 temperature sensor with the onboard ADC of DE10-Lite to display temperature on 7-segment.

- PWM Generator using Verilog

Generate PWM signals to control brightness of LEDs or motor speed using registers and counters on FPGA.

- 4-Digit Counter with 7-Segment Display

Use Verilog to implement a 4-digit BCD counter with time-multiplexed 7-segment display output.

- Binary to Gray Code Converter

Design a Verilog module to convert binary inputs into Gray code format with LED output.

- Debounce Circuit for Switch Input

Create a hardware debounce module using counters and state machines for clean button input.

- Multiplexer/Demultiplexer Implementation

Use Verilog to model and implement 4:1 MUX and 1:4 DEMUX circuits on DE10-Lite.

- LED Dice Roller

Implement a random number generator using LFSR logic and display output as dice using LEDs.

- Simple Stopwatch

Design a stopwatch with start/stop/reset functionality using Verilog and display time on 7-segment.

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Intermediate-Level FPGA Projects

- 8-bit RISC CPU on FPGA

Design a simple 8-bit CPU architecture in Verilog, simulate and synthesize on DE10-Lite with instruction set demo.

- FFT Processor Using Intel FFT IP

Use the Quartus FFT IP core to process signal data and visualize FFT bin magnitudes via UART or LED array.

- UART TX/RX Communication

Implement UART modules in Verilog to transmit and receive data between FPGA and PC terminal.

- SPI Master Interface

Design SPI master module in Verilog to communicate with external EEPROM or temperature sensor.

- Sobel Filter Edge Detection

Use FPGA fabric to implement Sobel kernel-based edge detection on low-resolution image inputs streamed via UART.

- I2C Master for Sensor Reading

Implement an I2C master in Verilog to fetch data from temperature or accelerometer sensors.

- Digital Clock with Alarm

Build a real-time clock using counters and display current time and alarm on 7-segment displays.

- PWM Servo Motor Controller

Control a servo motor's angle using PWM signal generated on FPGA and regulated by user switches.

- Infrared Remote Decoder

Decode IR signals using FSM and show corresponding outputs on DE10-Lite LED display.

- VGA Pattern Generator

Generate patterns or characters on a VGA display interface using timing logic implemented in Verilog.

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Advanced-Level FPGA Projects

- Minimal RISC-V Processor Core

Implement a simplified RISC-V core in Verilog, load programs into instruction memory, and verify over LEDs/UART.

- AES-128 Encryption Engine

Create a hardware-accelerated AES-128 encryption/decryption engine using FSM and pipelining.

- Basic CNN Accelerator

Design and implement a matrix multiply hardware block to accelerate CNN inference layers.

- Triple Modular Redundancy (TMR) System

Develop fault-tolerant logic blocks by replicating modules and voting logic in critical systems.

- CRC Generator for Communication

Implement a cyclic redundancy check (CRC) block for use in UART/SPI transmission verification.

- SD Card Data Logger

Use SPI interface to write sensor data to an SD card in FAT32 format.

- Neural Network Digit Recognizer

Implement a small-scale neural network for digit recognition (e.g., MNIST subset) on FPGA.

- Multicycle MIPS Processor

Design a multicycle MIPS processor with register file, ALU, control unit, and memory interfaces.

- HDMI Video Generator

Output colored video or patterns over HDMI using precise TMDS and pixel clock logic.

- Cache Memory Simulation

Simulate and implement direct-mapped and set-associative cache memory architecture on FPGA.