Digital Design Interview Questions - Part 2: Sequential Circuits

1. What is a sequential circuit? How is it different from a combinational circuit?

A sequential circuit is a logic circuit whose output depends not only on the current inputs but also on past inputs (i.e., it has memory). Combinational circuits have no memory; outputs depend only on current inputs.

2. Explain the working of an SR latch.

An SR (Set-Reset) latch is a basic memory element using two cross-coupled NOR or NAND gates. When S=1, R=0 -> Output Q=1 (Set); S=0, R=1 -> Q=0 (Reset); S=0, R=0 -> Holds previous state; S=1, R=1 -> Invalid state (for NOR).

3. What is a flip-flop? Explain different types of flip-flops.

A flip-flop is a clocked bistable circuit used to store a bit of data. Types include SR, D, T, and JK flip-flops. Each has a unique behavior for storing or toggling states.

4. Describe the working of a JK flip-flop with characteristic table.

Characteristic table:
J K | Q(next)
0 0 | Q
0 1 | 0
1 0 | 1
1 1 | Q' (toggle).

5. How is a master-slave flip-flop implemented?

It uses two flip-flops in series: the master is active on the rising edge, and the slave on the falling edge, ensuring the output changes only once per clock cycle.

6. What is a register? Explain types of shift registers.

A register stores multiple bits of data. Types of shift registers include SISO, SIPO, PISO, and PIPO, depending on input/output configurations.

7. Explain the difference between synchronous and asynchronous counters.

Synchronous counters trigger all flip-flops simultaneously, while asynchronous counters trigger flip-flops one after another, causing delay and glitches.

8. Design a 3-bit synchronous counter.

Use three T flip-flops: T0 = 1, T1 = Q0, T2 = Q0 & Q1. It counts from 0 to 7 synchronously with the clock.

9. What is race condition in sequential circuits?

It occurs when two or more signals change simultaneously and the final output depends on the order of changes, causing unpredictability.

Digital Design Interview Questions - Part 2: Sequential Circuits

10. How does a D flip-flop differ from a T flip-flop?

D Flip-Flop: Output follows input D on clock edge. T Flip-Flop: Toggles output on clock edge if T=1.

11. What are timing diagrams and why are they important in sequential design?

They graphically represent signal transitions over time. Useful for understanding and validating circuit behavior with timing constraints.

12. What is clock skew and how does it affect circuit performance?

Clock skew is the timing difference in clock signal arrival at different parts of a circuit. It can lead to setup/hold violations.

13. Explain setup time and hold time in flip-flops.

Setup time is the minimum time before the clock edge that input must be stable. Hold time is the minimum time input must remain stable after the clock edge.

14. How is a finite state machine (FSM) designed?

Steps: Define states, draw state diagram, assign binary codes, create transition table, and implement using flip-flops and logic gates.

15. Differentiate between Mealy and Moore machines.

Mealy: Output depends on state and input (faster). Moore: Output depends only on state (more stable).

16. What is the use of excitation tables in sequential circuit design?

They show the required flip-flop inputs for state transitions, aiding in logic design of sequential circuits.

17. Design a sequence detector for the sequence '101' using a state diagram.

Create states for each sequence bit. A ->1-> B ->0-> C ->1-> Output=1. Use state transitions based on input.

18. How can a counter be used to divide clock frequency?

Each stage in a binary counter divides the clock frequency by 2. A 3-bit counter divides by 8.

19. Explain the working of a ring counter and Johnson counter.

Ring Counter: A single '1' shifts in a circle. Johnson Counter: Inverts last bit and feeds it to input, offering more states.

20. What is metastability in sequential logic?

It occurs when a flip-flop fails to resolve to a stable 0 or 1 due to violations in setup/hold time, leading to unpredictable output.

21. Describe the role of feedback in sequential circuits.

Feedback paths store previous outputs and influence future states, enabling memory and sequential

operation.

22. How is a synchronous reset different from asynchronous reset?

Synchronous Reset: Acts with clock edge. Asynchronous Reset: Acts immediately, regardless of clock.

23. What is a timing constraint and how is it verified?

Timing constraints define setup, hold, and delay requirements. Verified using static timing analysis tools.

24. Explain the process of state minimization in FSM.

Identify equivalent states with identical outputs and transitions, then merge to simplify the FSM.

25. What are the key challenges in designing large sequential circuits?

Issues include timing closure, metastability, clock distribution, power, area optimization, and testability.