JAGADEESH J

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EDUCATION

Vellore Institute of Technology **2021 – 2025**
B.Tech Electronics and Communication Engineering | ***CGPA - 8.61*** *Chennai, Tamil Nadu, India*

Maharishi Vidya Mandir **2021**
Higher Secondary School | ***Score - 93%*** *Erode, Tamil Nadu, India*

Bhaktavatsalam Vidyashram **2019**
Secondary School | ***Score - 80.4%*** *Chennai, Tamil Nadu, India*

SKILLS

- **PROGRAMMING LANGUAGES:** Verilog, SystemVerilog, C, Python
- **TOOLS:** Modelsim, Intel Quartus Prime, Vivado, Cadence Virtuoso, FPGA boards (Altera and Xilinx)

EXPERIENCE

Silicic Innova Technologies Pvt Ltd **Chennai, India**
VLSI Design Intern | Tools used: Modelsim, Quartus Prime, Vivado, Altera DE2-70, Artix-7 *Jun 2024 - Jul 2024*

- Gained exposure to real-time image processing applications using FPGA-based systems and Verilog HDL.
- Developed familiarity with industry-standard tools and communication protocols (I2C & UART).

Maven Silicon **Bengaluru, India**
VLSI Design Intern | Tools used: Modelsim, Quartus Prime *Aug 2023 - Oct 2023*

- Gained practical expertise in VLSI Design Methodologies, including RTL synthesis and Verilog HDL.
- Designed and implemented an SPI (Serial Peripheral Interface) protocol using Verilog HDL.

PROJECTS

APB VeriPilot: A Push-Button DV Execution Framework for APB-Based Designs

- Designed and implemented an APB to SRAM interface, ensuring efficient data transfer and protocol compliance.
- Developing a UVM-based APB VIP, configurable as an active or passive agent, supporting both simulation and emulation.

Optimized Image Processing on FPGAs: Comparative Performance Analysis of Adder Designs in Image Smoothing Applications (Published at IEEE-SCEECS'25) | Tools used: Vivado

- Developed an FPGA-based image smoothing application (512x512 grayscale) using Verilog, optimizing performance, power, and resource utilization.
- Compared adder architectures (Approximate, Kogge Stone, Brent Kung) integrated with image smoothing to evaluate efficiency in real-time applications.

Comparative Analysis of Dynamic and Static Circuits (GPDK90 Technology) | Tools used: Cadence Virtuoso

- Analyzed and simulated dynamic vs. static circuits, evaluating delay, power, performance, and area.
- Studied standard cell characterization and the process for generating .lib and .lef files.

Automated Waste Segregation System (Accepted by *IEEE-iSES*)

- Designed a waste segregation prototype using ESP32 and ESP-CAM modules, enabling segregation of waste into different bins based on type.
- Integrated object detection to identify and classify waste, transmitting data to ESP32 for processing.

CERTIFICATIONS

- **VLSI Design Methodologies** - Maven Silicon
- **VLSI Design Internship** - Maven Silicon

ACHIEVEMENTS & EXTRA-CURRICULAR

- **Attendance Excellance Award** - VIT Chennai
- **VITeach - School Outreach Program:** Assisted in preparing math assignments for children in grades 3-5.
- **Cricket:** Represented school cricket team and a cricket academy in various tournaments, demonstrating teamwork, leadership and sportsmanship.