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USN

School of Computer Science and Engineering
B.Tech (Hons.)
CIE-1
Academic Year 2024-2025

Course: Embedded Systems and Microcontrollers	**Course Code: CS1120**	**Semester: II**
Time: 2:30pm to 4pm	**Max Marks:20**	**Date :11-03-25**

Sl. No.	Part A-Questions	Marks	L1-L6	CO
1.	A system that operates without an RTOS and directly executes code on hardware is called a bare metal system.	1	L1	CO1
2.	Which of the following best describes a General-Purpose Operating System (GPOS)? a) Designed for real-time constraints b) Provides a non-deterministic scheduling approach c) Ensures real-time performance in critical systems d) Runs only one application at a time	1	L2	CO1
3.	Which of the following best describes an ASIC? a) A programmable microcontroller for general use b) A chip designed for a specific application with fixed functionality c) A standard processor that can run multiple applications d) A software program running on an embedded system	1	L2	CO1
4.	Where are micro-opcodes typically stored in ? a) Cache memory b) RAM c) ROM or Control Store d) Hard disk	1	L1	CO1
5.	**Computer architecture** is a set of rules and methods that describe the functionality, organization, and implementation of computer systems.	1	L1	CO1
6.	The **Program counter** keeps track of the address of the next instruction to be executed.	1	L1	CO1
7.	The **Cache** memory hierarchy exploits the principle of locality to improve system performance.	1	L2	CO1
8.	Unit of Transfer (x_i) of Lower level of memory is less than Higher Level.	1	L3	CO1
9.	Which of the following storage devices directly interacts with the CPU? A) Secondary storage B) Primary storage C) Hard disk	1	L2	CO1
10	FPGA/PAL is an example of Programmable Logic Device .	1	L1	CO1
11	Systems design focuses only on the CPU and does not include components like memory or cache. A)TRUE B)FALSE	1	L2	CO1

L1- Remember, L2- Understand, L3 – Apply, L4- Analyse, L5 – Evaluate, L6 – Create

12	The **inclusion property** states that any data present at a lower level (closer to the processor) must also exist at a higher level in the memory hierarchy. Which of the following statements correctly follows this principle? A) If a cache block is present in **L1 cache**, it must also be in **L2 cache**. B) If data is evicted from **L1 cache**, it may still exist in **L2 cache**. C) The inclusion principle ensures that **registers** hold all data present in cache. D) Inclusion ensures that the **CPU always accesses the highest level of memory first**.	1	L3	CO1
13	Filename.asm file is the output of compile stage of SW Program Development	1	L2	CO1
14	ROM is a type of non-volatile memory that allows data to be stored permanently and cannot be modified after initial programming.	1	L1	CO1

15	In the below given code ,
	A) The function square() is repeatedly used, leading to **temporal locality**.
	B) Accessing elements of arr[] in sequence improves **spatial locality**.
	C) Function calls disrupt cache behavior, reducing **temporal locality**.
	D) The code does not exploit any principle of locality.
	
	`#include <stdio.h>`
	`int square(int x) {`
	`  return x * x;  // Function will stay in cache due to repeated calls`
	`}`
	`int main() {`
	`  int a = 5;`
	`  int b = square(a);`
	`  int c = square(10);`
	`  printf("%d %d %d\n", b, c);`
	`  return 0;`
	`}`
		1	L3	CO1

Course Outcomes:

CO1: Understand the basic concepts of embedded system, microcontroller, different components of microcontroller and their interactions as applied to RP2040.
CO2: Develop embedded solutions using Embedded C and Assembly language.
CO3: Program ARM microcontroller to perform various tasks and stack implementation in Cortex-M0+.
CO4: Understand the key concepts of such as Instruction cycle execution, I/O, DMA, interrupts and interaction with peripheral devices in embedded system

Marks Distribution									
L1	L2	L3	L4	L5	L6	CO1	CO2	CO3	CO4
6	6	3	5	--	--	15	5	--	--

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