JAGADHEESVAR N

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PROFESSIONAL SUMMARY

- The detailed and motivated Physical Design Engineer trained in complete RTL-to-GDSII flow has hands-on experience in synthesis, floor planning, placement, CTS, routing, and PPA optimization.
- Skilled in using Synopsys and Xilinx toolchains (Fusion Compiler, ICC2, Design Compiler, PrimeTime, and Vivado) to develop high-performance ASICs.
- Knowledgeable in STA, IR/EM analysis, PV sign-off (DRC, LVS, ERC), and clock tree optimization techniques. Solid understanding of FinFET nodes and low-power design (UPF, MV domains).
- Demonstrated leadership in the execution of physical design projects and in driving QoR improvements. Strong in scripting using TCL and Embedded C, with a keen interest in design automation and mentoring.

PROFESSIONAL TRAINING

Advanced Physical Design and Verification, *Maven Silicon Softech Pvt. Ltd.* *(Sept 2024 - Present)*

- Trained in advanced backend VLSI design, with hands-on experience executing the complete physical design flow from netlist to GDSII using industry-leading EDA tools such as Synopsys Fusion Compiler, ICC2, Design Compiler, PrimeTime, Xilinx Vivado, and ISE.
- Gained practical knowledge on optimizing design for Performance, Power, and Area (PPA). Additionally, assisted in RTL design using Verilog and demonstrated proficiency in integrating DFT features into designs.

PG Program in Embedded and SOC Design *(Sept 2024 - Present)*

National Institute of Electronics and Information Technology, Ministry of Electronics and Information Technology

- Gained in-depth knowledge of Embedded Systems architecture, SoC design methodologies, and real-time system integration. Hands-on experience with ARM-based microcontrollers, Verilog HDL, and FPGA prototyping.
- Developed projects involving device drivers and real-time OS (RTOS) basics. Trained in system-level design, hardware-software partitioning, and low-power embedded system design.

PROFESSIONAL EXPERIENCE

Junior Engineer, *M/s. Neopal Aircon Engineers - Part Time (Hybrid)* *(Feb 2022 - Aug 2024)*

- Designed and developed Electrical designs and PCB layouts using AutoCAD Electrical and KiCad. Provided service support for electrical and electronic systems. Managed billing, documentation, and report generation for projects.
- Maintained and updated site records to ensure project compliance. Assisted in troubleshooting and resolving technical issues in electrical systems. Coordinated with teams to ensure smooth project execution and maintenance.

TECHNICAL SKILLS

- **Physical Design Tools** : Synopsys Fusion Compiler, ICC2, PrimeTime, Design Compiler, Calibre
- **Signoff & Analysis** : STA, IR/EM, CLP, DRC, LVS, ERC, Antenna Checks, LEC, SI
- **Scripting & Programming** : TCL, Python, Embedded C, Verilog
- **Low Power Design** : Multi-voltage domains, Power gating using UPF
- **Synthesis** : Xilinx Vivado, ISE
- **Other Tools** : AutoCAD Electrical, KiCad

EDUCATION

- **B.E. in Electrical and Electronics Engineering** *76.3%*
  University College of Engineering, (BIT Campus), Tiruchirapalli *(2024)*
  - In-Plant Training : TamilNadu Newsprint and Papers Limited (TNPL), Karur District.
  - Workshop : Integration of renewable energy with energy storage systems.
- **Higher Secondary** *61%*
  Don Bosco Matric. Hr. Sec. School, Egmore, Chennai. *(2020)*
- **SSLC** *80%*
  Don Bosco Matric. Hr. Sec. School, Egmore, Chennai. *(2018)*

PROJECTS

- **RISC - V : Digital and Physical Design** *(Apr 2025)*

  Tools: **Design Compiler, ICC2 Compiler, Prime Time**
  - Developed a Risc-V project from synthesis, Placement & Routing and Timing Analysis, Macro creation.
  - Logic Synthesis done using the Design Compiler, Placement & Routing done using the ICC2 Compiler, Timing Analysis Done using Prime Time.

- **ROUTER 1X3 : Digital and Physical Design** *(Mar 2025)*

  Tools: **ISE, Fusion Compiler, Prime Time**
  - Developed a router 1x3 from RTL designing, Testbench designing, and Fusion Compiler.
  - Logic Synthesis, Floorplanning, Placement, Clock tree synthesis, Routing, Timing Analysis, DRC, ERC, Signoff.

- **PHASOR MEASUREMENT UNIT - For a Small Scale Power System** *(Mar 2024)*

  Tools: **Embedded C, Arduino, Design Assembly**
  - Developed a phasor measuring system to measure phase-shifted sinusoidal waves in transmission lines, ensuring accurate monitoring of the power system.

- **FASTAG - Radio Frequency Identification** *(Nov 2023)*

  Tools: **Embedded C, Java Script, Arduino**
  - Developed a project on the FASTAG technology used in toll gates, focusing on RFID systems and their applications.

COURSES

- **Embedded Systems Designs & Applications** *(May 2024)*
- **Integrated Building Services** *(Apr 2024)*
- **Design of Photovoltaic Systems** *(Aug 2023)*
- **Electric Vehicle Charging Systems** *(Mar 2023)*

CERTIFICATIONS

- **P**articipated in Satish Dhawan Space Center, SHAR, **(Indian Space Research Organisation)** Expo.
- **Event Coordinator**, Hosted Events on National Level Symposium hosted events - Circuit Crush.

ACHIEVEMENTS

- Secured first place in a 10 km marathon race.
- Won the inter-school basketball competition.

SOFT SKILLS

- Design Flow Coordination
- Multi-Tasking in High-Priority Environments
- Specification and Report Drafting
- Technical Discussion and Team Sync
- Constraint Violation Analysis and Fix

HOBBIES

- Movies
- Swimming
- Cycling
- Music

LANGUAGES

- English
- Tamil
- Hindi
- Malayalam

DECLARATION

I hereby declare that all the information provided is true to the best of my knowledge.

Place: Bengaluru **Jagadheesvar N**
Date: