CMOS BASED D FLIP FLOP

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ABSTRACT:

In today's world, the VLSI designer totally dependent on Flip-flops as it has wide range of applications in various field of electronics. Flip-flops are widely used in spacecraft for numerous processes; these are also used in telecommunication sector for exchange the information and storage the data. In term of power consumption, MTCMOS based D flip-flop is reduced by 8.2 %, power gating-based D flip-flop is decreased by 7.42% while more reduction in SVL based D flip-flop is brought down by 10% as compared to conventional CMOS based D flip-flop at 45nm technology.

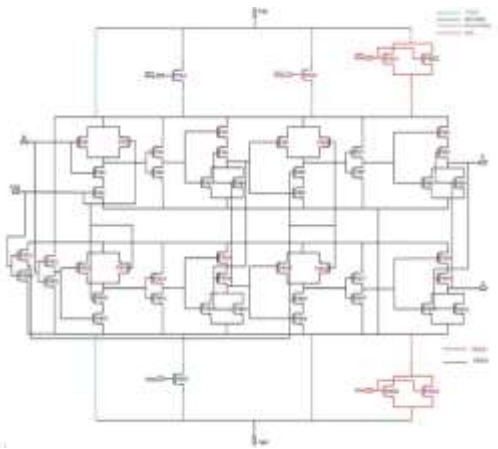
Keywords—Flip-Flop, CMOS, MTCMOS, Power Gating, SVL, Power Dissipation, Delay, Power Delay Product, Leakage Current, Layouts.

REFERENCE CIRCUIT DETAILS:

CMOS is called as "Complementary Metal Oxide Semiconductor" [4]. CMOS technique is one of the most well-known technique in the computer chip design industry and widely used today to compose integrated circuits in several miscellaneous applications. CMOS technology uses of both PMOS and NMOS transistors i.e. pull up and pull-down network that's why it is called as complementary Metal Oxide Semiconductor. CMOS is quite suitable technique for various components such as microprocessors, microcontrollers, and memories- RAM, ROM and ASICs. A Complementary MOS circuits has negligible static power dissipation like NMOS or BIPOLAR circuits.

Most of the time, power is exhausted when switching takes place in the circuit. More number of gates can be integrated on an IC by CMOS technology than NMOS or bipolar technology, so lowering the power consumption. Power consumption is a critical concern in the VLSI circuits due to regular decrease in feature size of CMOS circuits and a subsequent increase in chip density and operating frequency.

DIAGRAM:



REFERENCE OUTPUT WAVEFORM:

REFERENCE:

https://www.researchgate.net/publication/323642788_Design_and_Performance_analysis_of_CMOS_based_D_Flip-Flop_using_Low_power_Techniques