Multiplexer as Function Generator in FPGA

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Problem Statement

Designs used in the Space and Military applications uses Micro-sim based FPGA, Where programming is done using the Antifuse Technology. The basic logic cell used in the implementation is C-Cell. All the combinational and sequential circuits are implemented using C-cell and R-cell.

The main Objectives of the Project

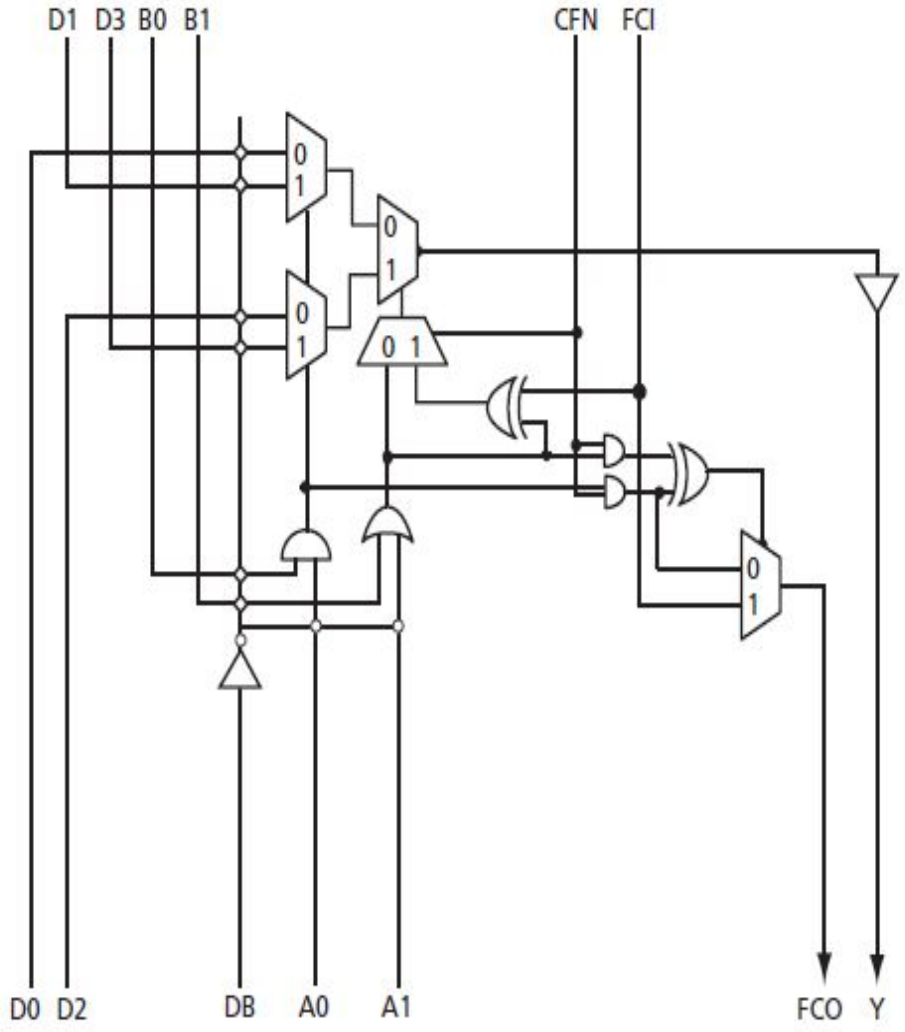
- The objective of this work is do error analysis on the C-cell based combinational and sequential circuits.
- Device a mechanism for fault tolerant design.
- Fault analysis on C-Cell and Fault Modeling of C-Cell.

Fault analysis of C-Cell

- An FPGA contains a large number of logic cells. Each logic cell can be configured to implement a certain set of functions.
- A multiplexer-based logic module is typically composed of a tree of 2X1 MUXes using different primitive gates like NOT, AND, OR, NOR, NAND, XOR, XNOR gates.
- A multiplexer-based logic module is typically composed of a tree of 4-to-1 MUXes using different Primitive gates.
- Fault Analysis is done with Multi-bit Adders using full-Adder C-Cell and multi-bit Array multiplier using single C-Cell.
- There are few required steps in order to measure the for SEU(Single Event Upset) tolerance analysis.

These steps are generally used for fault injection experiment, which cover three processes

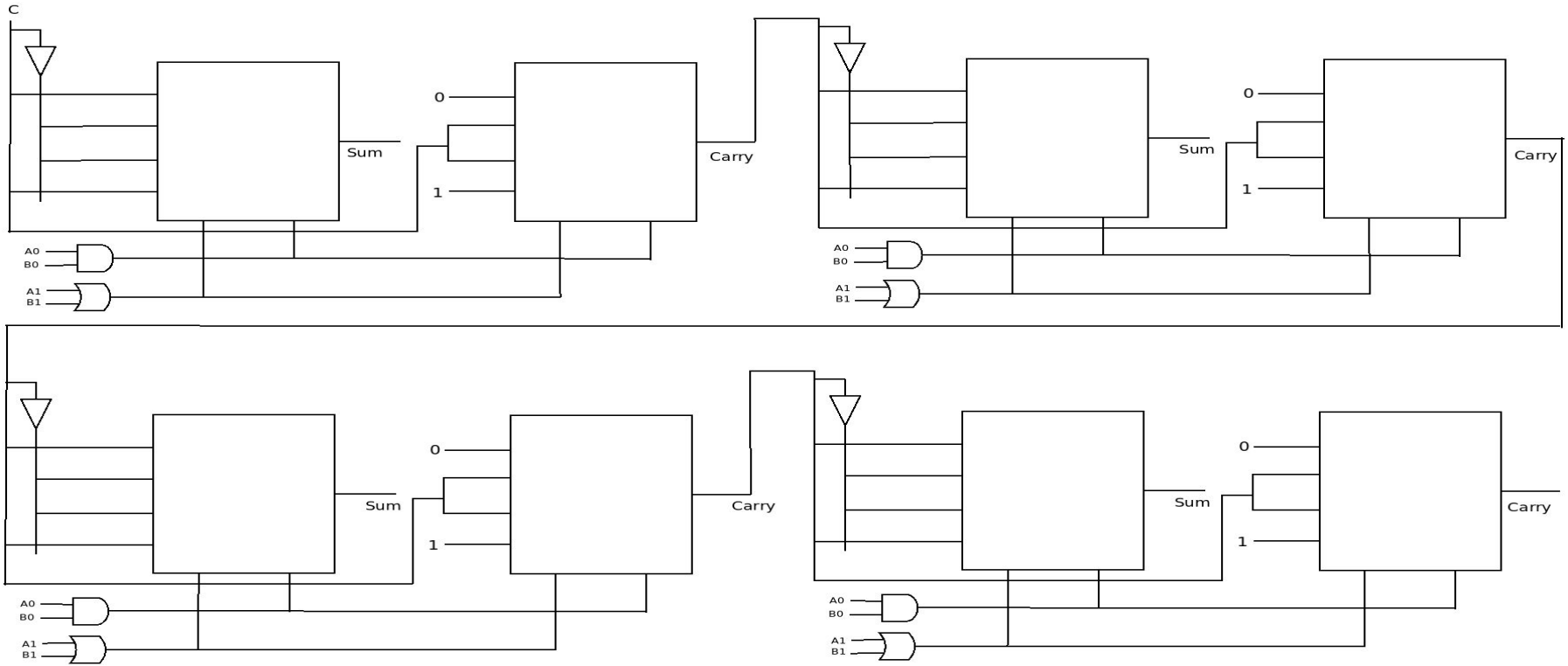
- Fault Target Location
- Fault Injection.
- Observation of Fault Consequences



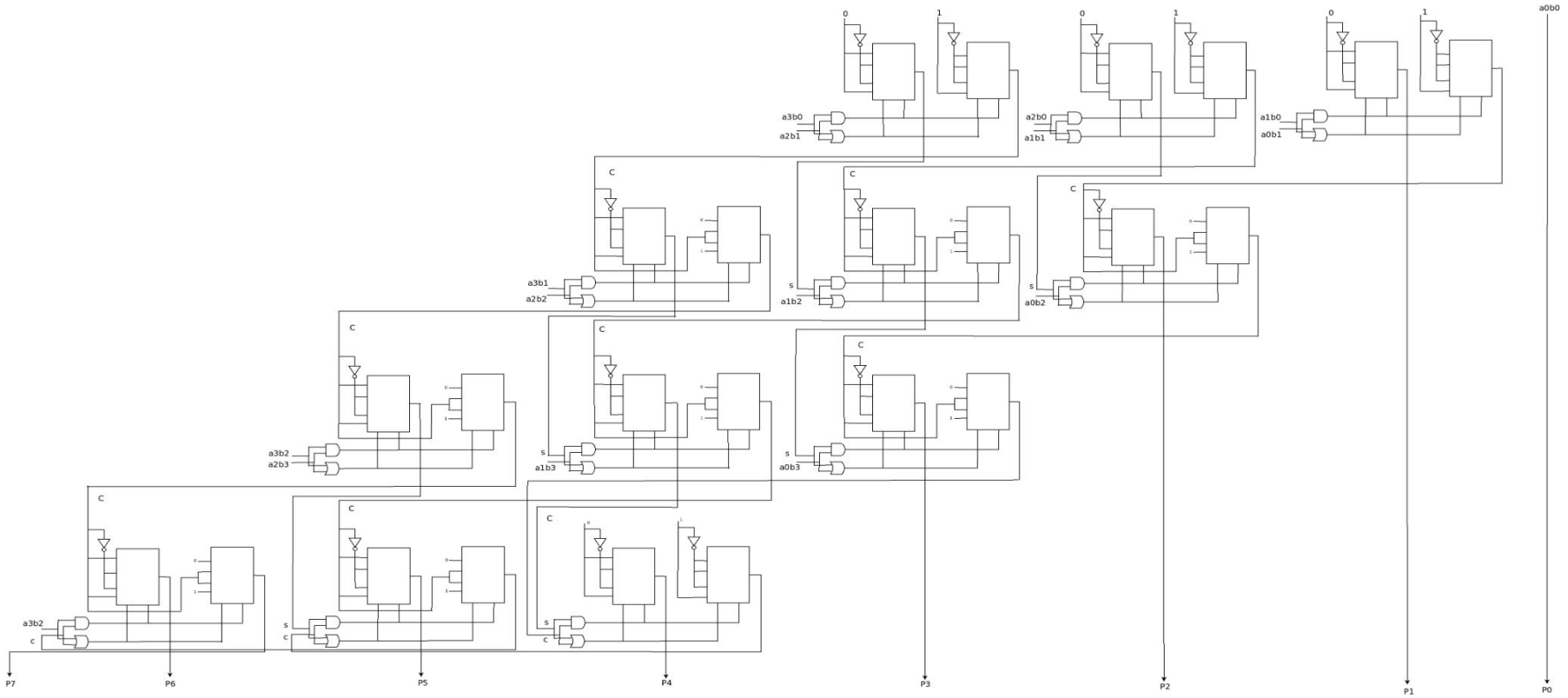
Work Done

- The Basic 4 x 1 MUX
  - Out = D0S1'S0' + D1S1'S0 + D2S1S0' + D3S1S0.
- C-Cell consist of S0 = (A0 * B0) as AND gate and S1 = (A1 + B1) as OR gate
  - Out = D0(A0*B0)'(A1+B1)' + D1(A0*B0)'(A1+B1) + D2(A0*B0)(A1+B1)' + D3(A0*B0)(A1+B1)
- The Implementation of C-cell using Equivalence gate
- We cannot implement using universal gates.
- Implemented Half Adder and Full Adder C-cells.
- Implemented multi-bit Adders and multi-bit array multipliers using C-cell.

Multibit C-cell Adders



Multibit Array C-cell Multiplier

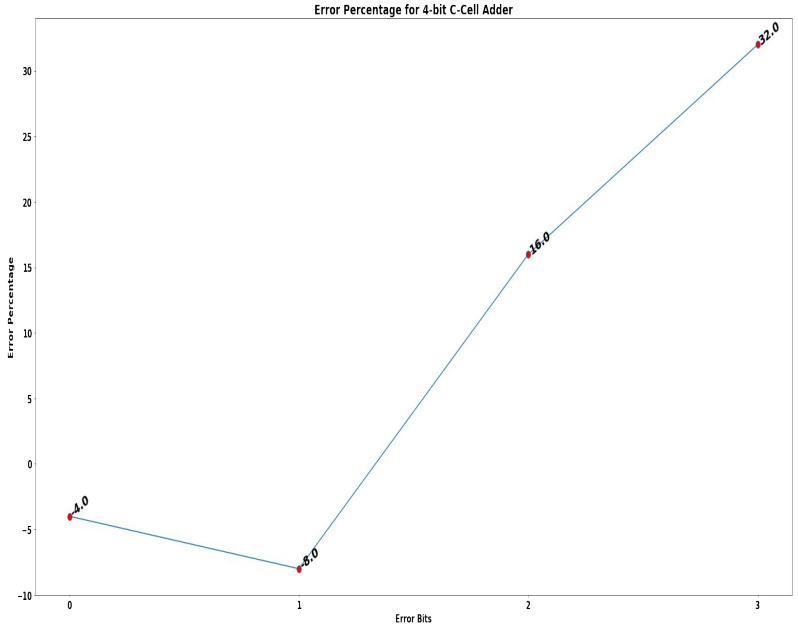


Results & conclusion

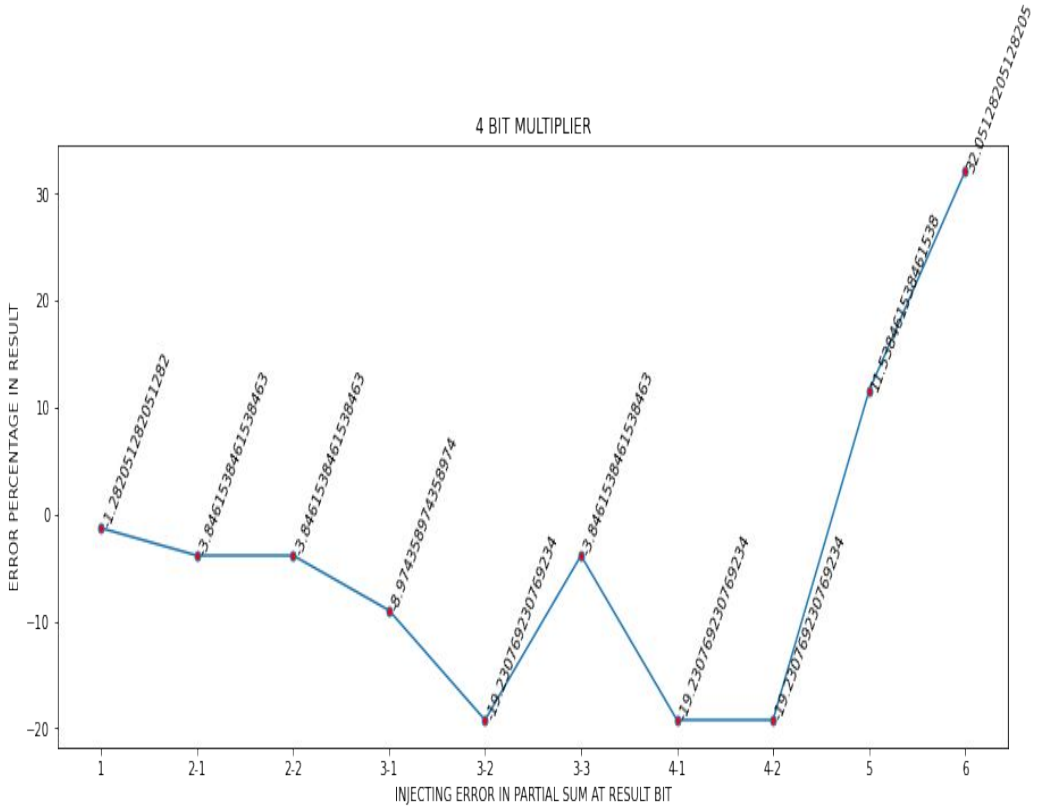
- In C-Cell ,the single event upset can occur at the select line of multiplexer.
- Error injection in different bit positions of adder with respective 4-bit ,8-bit and so on upto 128 bit.
- Generating the Error Difference between original Result and Error Result.
- Generating the Error Percentage.
- This analysis can be helpful to add the fault tolerance techniques at the highest error percentage bit.

4-bit C-Cell adder with Error injection at S0&S1 select line

Original value	Error value	Difference Original and Error	Error Percentage
25	26	-1	-4
25	27	-2	-8
25	21	4	16
25	17	8	32



4X4 C-cell array multiplier with Error Analysis



Original value	Error value	Difference Original and Error	Error Percentage
156	158	-2	-1.282051
156	162	-6	-3.846154
156	162	-6	-3.846154
156	170	-14	-8.974359
156	186	30	-19.230769
156	162	-6	-3.846154
156	186	30	-19.230769
156	186	30	-19.230769
156	138	18	11.538462
156	42	50	32.051282

Future work

- The C-Cell connection with Registers or Flip-Flops will be analyzed.
- Sequential Circuit behavior will be estimated
- Errors in sequential circuits will be estimated

Thank you