# RATHOD JAGADISH

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## Education

IIITDM Kancheepuram 7.02/10

Bachelor of Technology in Computer Science Aug 2017 - May 2021

Sree Triveni Junior College, Hyderabad

Telangana State Board of Intermediate Education, MPC

Jun 2014 - Mar 2016

Govt. High School, Sangareddy 9/10

Board of Secondary Education, Andhra Pradesh

Jun 2013 – Apr 2014

#### Relevant Coursework

• The complete Full-Stack JavaScript (Udemy)

• The Joy of Computing using Python (NPTEL)

• Python Boot-camp 2020 (Udemy) 
• Social Networks (NPTEL)

Advanced Web developer (Coursera)
 Design and Analysis of Algorithm

• UX Design Fundamentals(Coursera) • Database Management system

## **Projects**

# Multiplexer as Function Generator in FPGA | (B.tech Project) IIITDM Kancheepuram

May 2021

89%

- All Combinational and Sequential Circuits are Implemented using C-cell and R-cell.
- Synthesized it on Micro-Sim FPGA, Where Programming is done using Anti-fuse technology.
- Fault Analysis and Fault Modeling on C-cell.
- Experimental Analysis is done in Python simulation and generating Error Percentage upon Original value and Error Value

## Hand Gesture Recognition | (Design Project) IIITDM Kancheepuram

Nov 2020

- Implemented a Hand Gesture recognition model using Python, Google based Media-Pipe.
- For minimalist Design using Hand Gesture used vPython.

## **Course Projects**

#### Water Leakage Detection System | Product Management Design

Apr 2020

- Implemented IOT based Water Leakage Detection System using arduino.
- The leakage detection at Home Appliance and Deep Irrigation system.
- Built Automated SMS system using WiFi-module when ever leak happen at bursting pipeline.
- Design and Prototypes a Water Leakage Detection System as a product. Sent it for startup Idea in MadeIT.

## Linear Discriminant Analysis using Python | VLSI System

Oct 2019

- Built a linear Discriminant model from the ground up using Verilog HDL and Python.
- To analysis the data-set of patients and non-patients using Linear Discriminant Analysis Model.
- Implementing 8bit Wallace tree multiplier using Verilog to extract the analysis of Linear Discriminant ML algorithm.

## Parking Slot Management System | Database Management System

Nov 2018

- Developed a full-stack Parking Slot Management with Database.
- User Interface Design is implemented using HTML, AJAX, JQUERY, JAVASCRIPT, for integrating Database used PHP and MySQL database.
- XAMPP Software is used for run the database system of the Project.

#### Tomosulo algorithm | Computer Architecture

**April 2019** 

- Developed a Tomosulo algorithm simulator using python.
- Compared fastness of the algorithm between scoreboard and Tomosulo.

## **Technical Skills**

Languages: Python, C/C++, JavaScript, Verilog

Technical skills: OpenCV, Adobe XD, Machine Learning Web Technologies: HTML5/CSS3, React JS, MySQL