Self Project- LTspice
Jagdish Meghwal
231040054
Technology File: TSMC018 (180nm PDK)
LTspice files:

Que 1.a to 1.d - Project.asc
Que 1.e - EProject.asc

1. Simulation of symmetrical and skewed CMOS inverter, and pass transistor:

1.a.

(Que) Do an analysis to find out the PMOS to NMOS size ratio of the minimum-sized CMOS inverter to have equal rise and fall time.

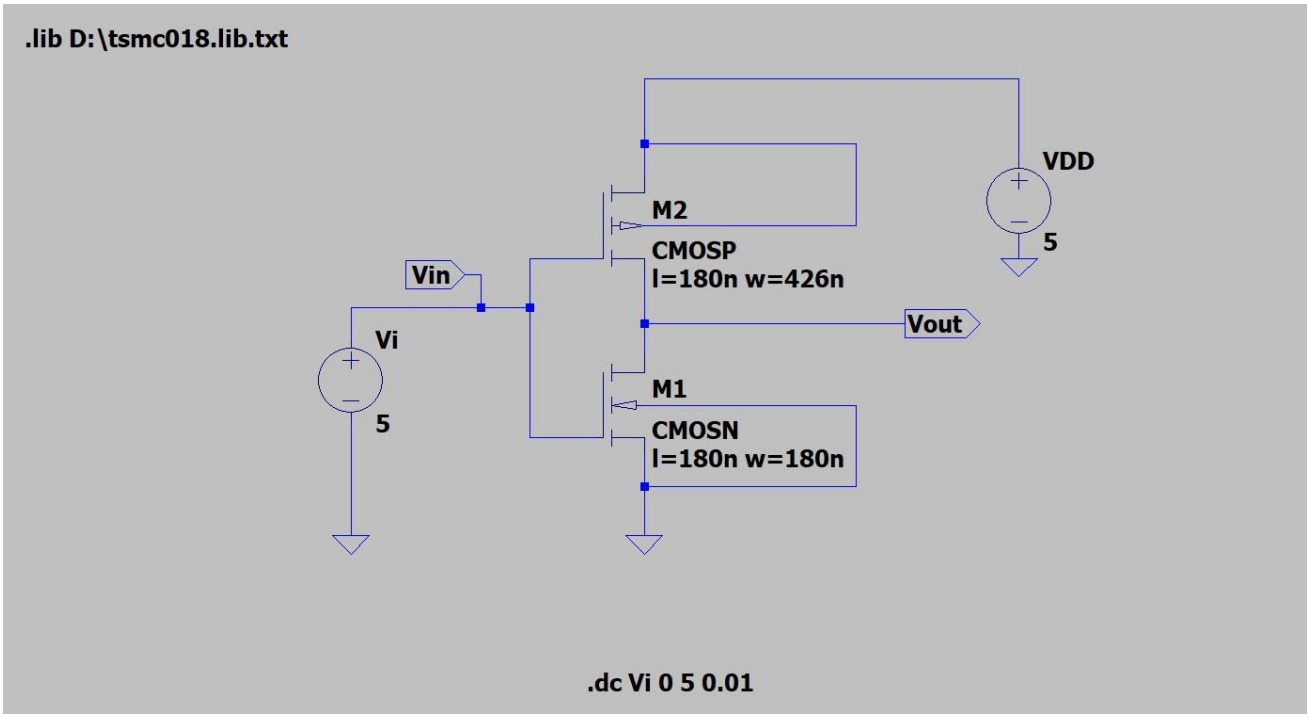
Analysis for Sizing NMOS & PMOS:

µn=273.8094484; µp=115.6894042

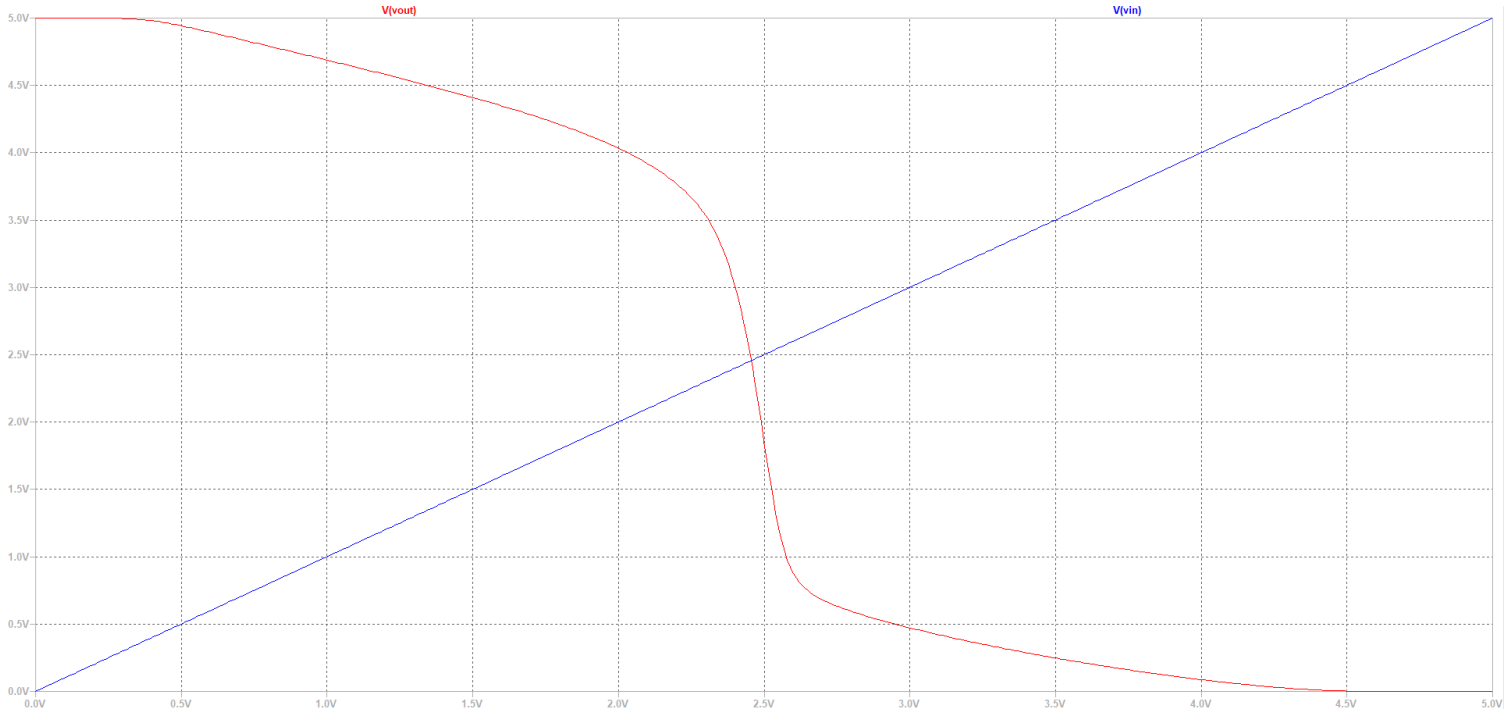
Size of PMOS = (µn/µp) x Size of PMOS = 2.36 of NMOS

Taking minimum sized NMOS W/L=180n/180n; PMOS W/L will be equal to 426n/180n

Circuit:

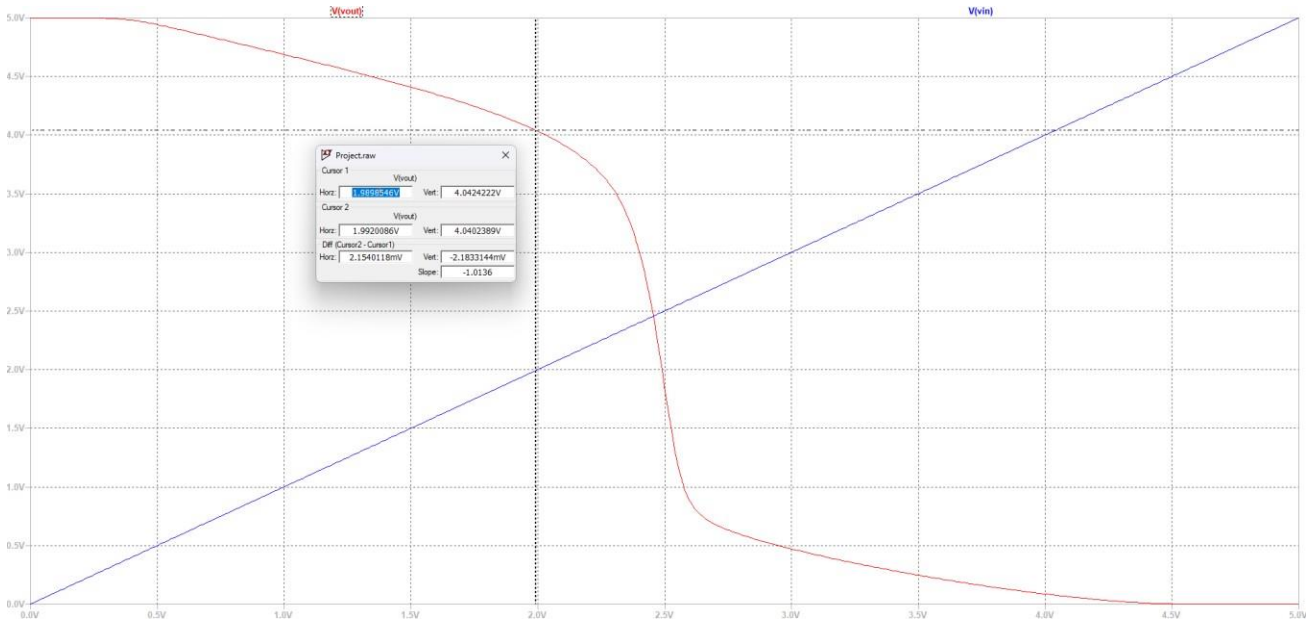


VTC:



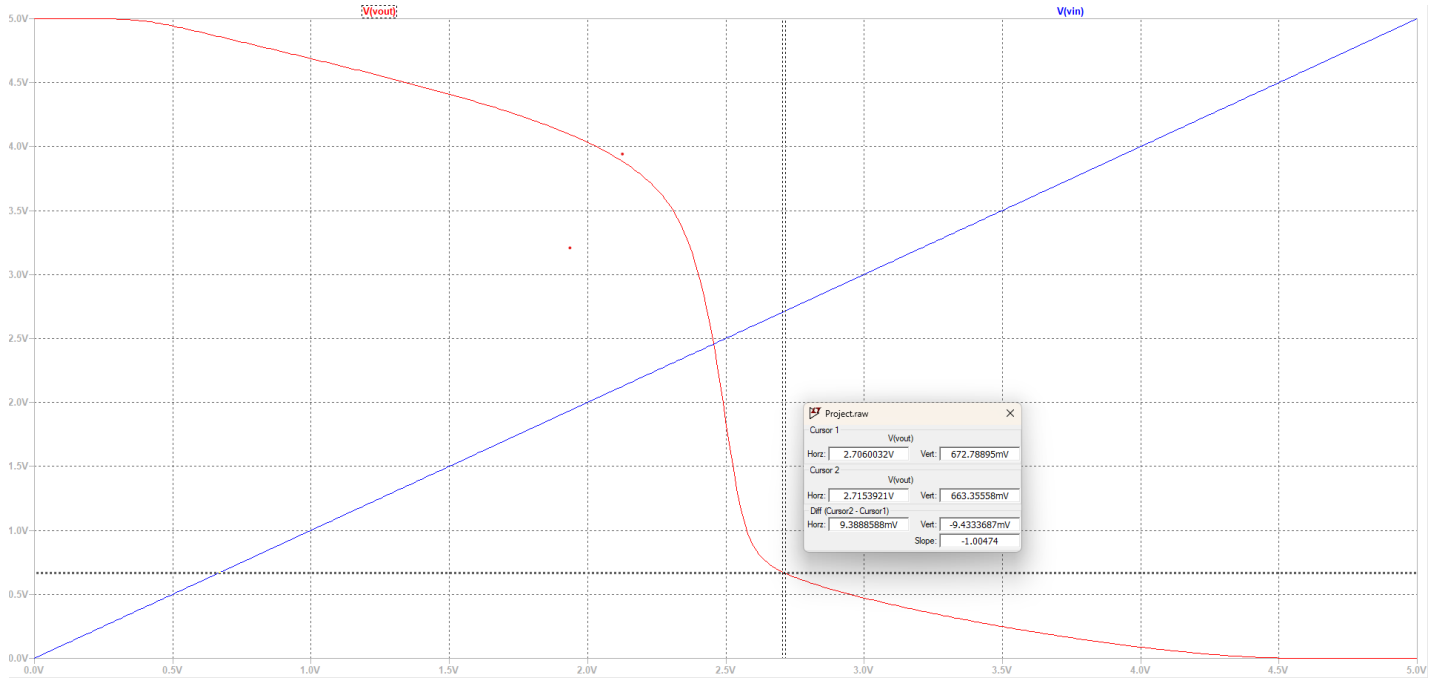
(Que) Simulate the static VTC of that inverter, and find out signaling threshold values (VIL, VIH, VOL, VOL) using the slope = –1 criterion from the VTC. Write down high and low noise margins, and the noise immunity of the inverter.

(V_{IL}, V_{OH}):



Slope -1 point from the plot: **(V_{IL}, V_{OH})**: (1.99V, 4.04V)

(V_{IH}, V_{OL}):



Slope -1 point from the plot: **(V_{IH}, V_{OL})**: 2.71V, 0.67V

(Que) Write down high and low noise margins, and the noise immunity of the inverter.

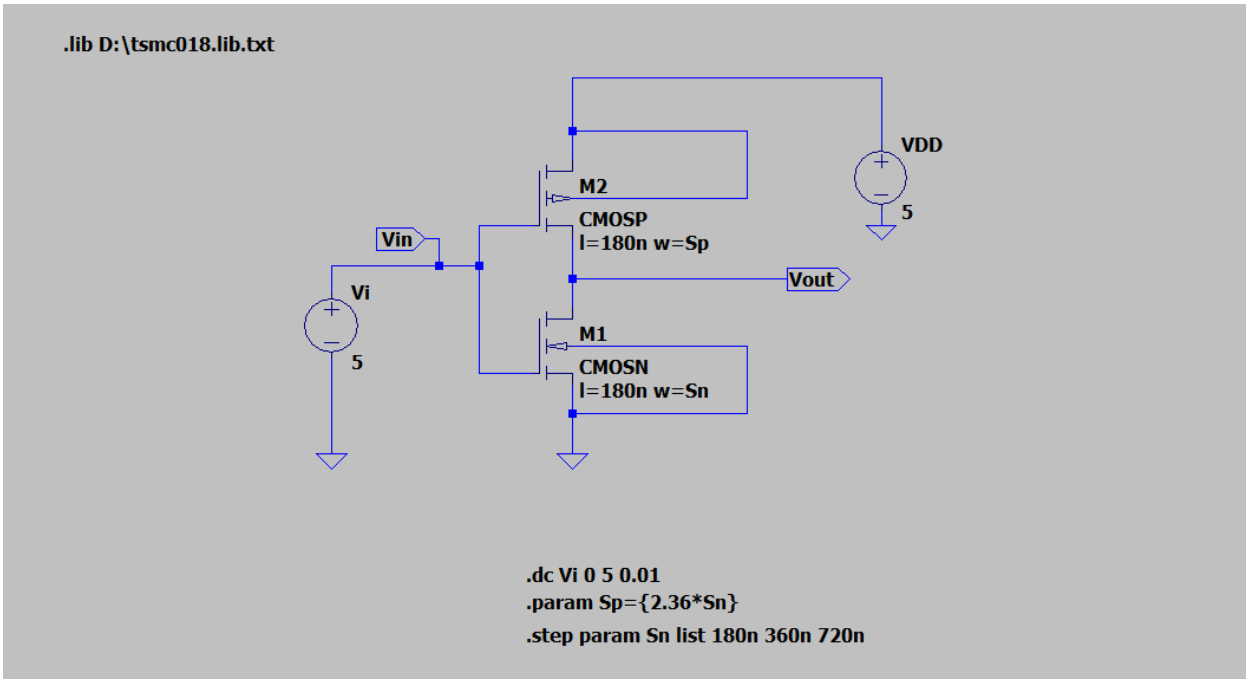
(V_{IL}, V_{OH}): 1.99V, 4.04V
(V_{IH}, V_{OL}): 2.71V, 0.67V

NM_L: V_{IL}-V_{OL}: 1.99-0.67 = 1.32V
NM_H: V_{OH}-V_{IH}: 4.04-2.71 = 1.33V

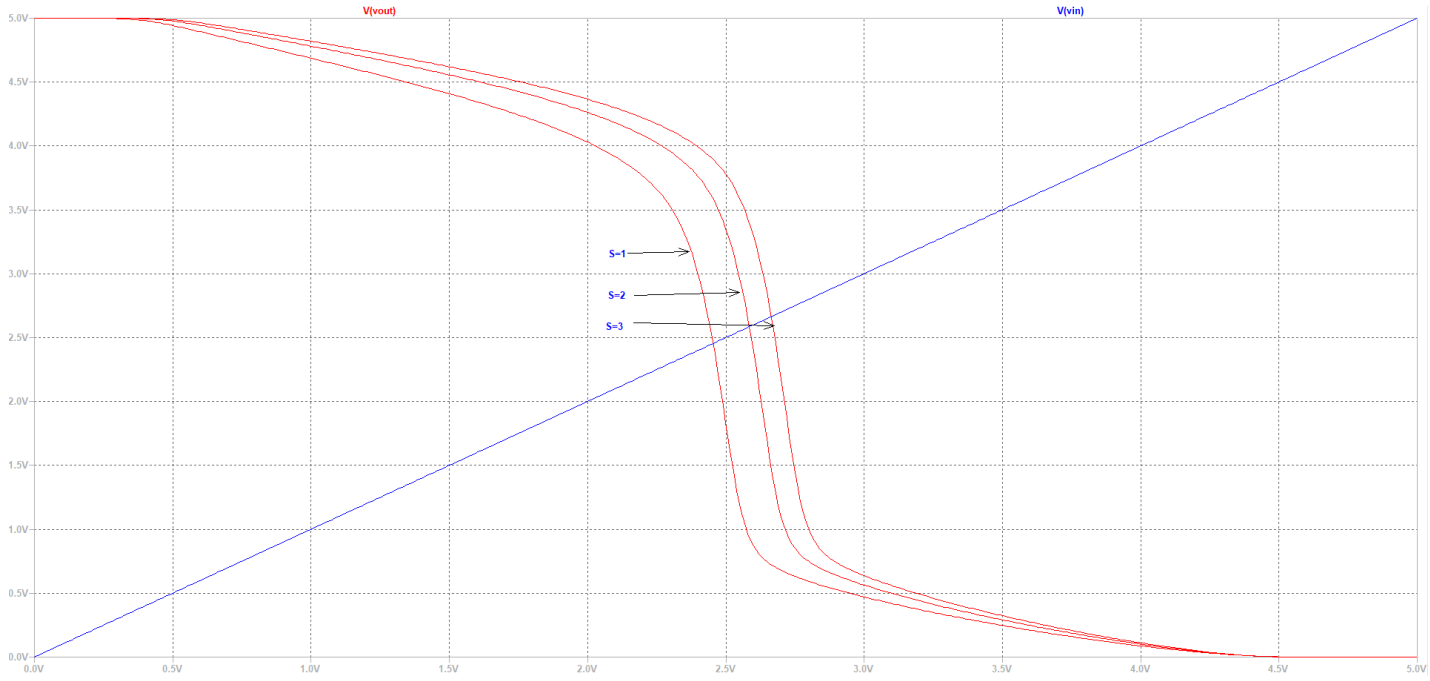
Noise immunity = min(NM_L, NM_H) = 1.32V

(Que) Also, simulate the static VTC of an inverter which is sized S times the minimum-sized inverter (both NMOS and PMOS are S times the size of the corresponding NMOS and PMOS of the minimum-sized inverter) for S = 1,2,4, and plot all VTCs in a single graph with clear legends indicating how the sizing affects the VTC.

Circuit:



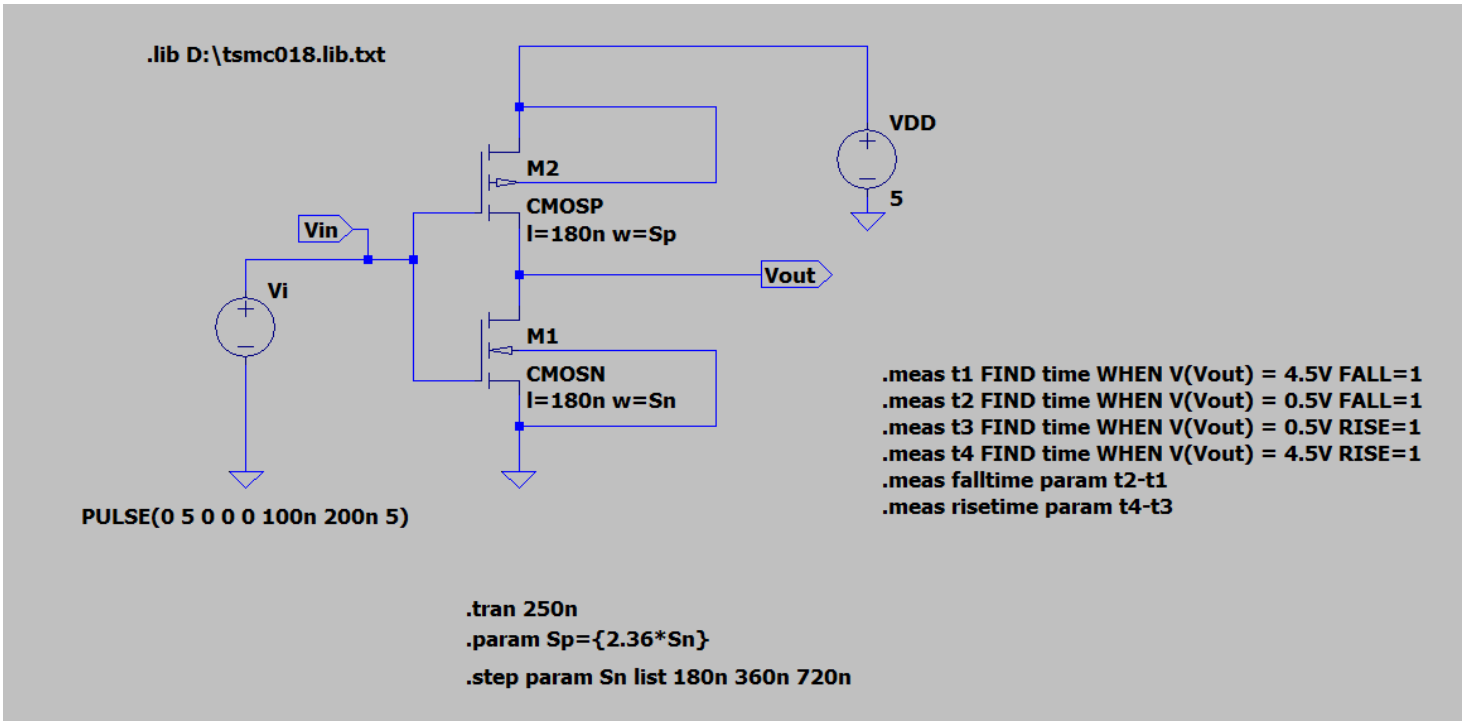
VTC:



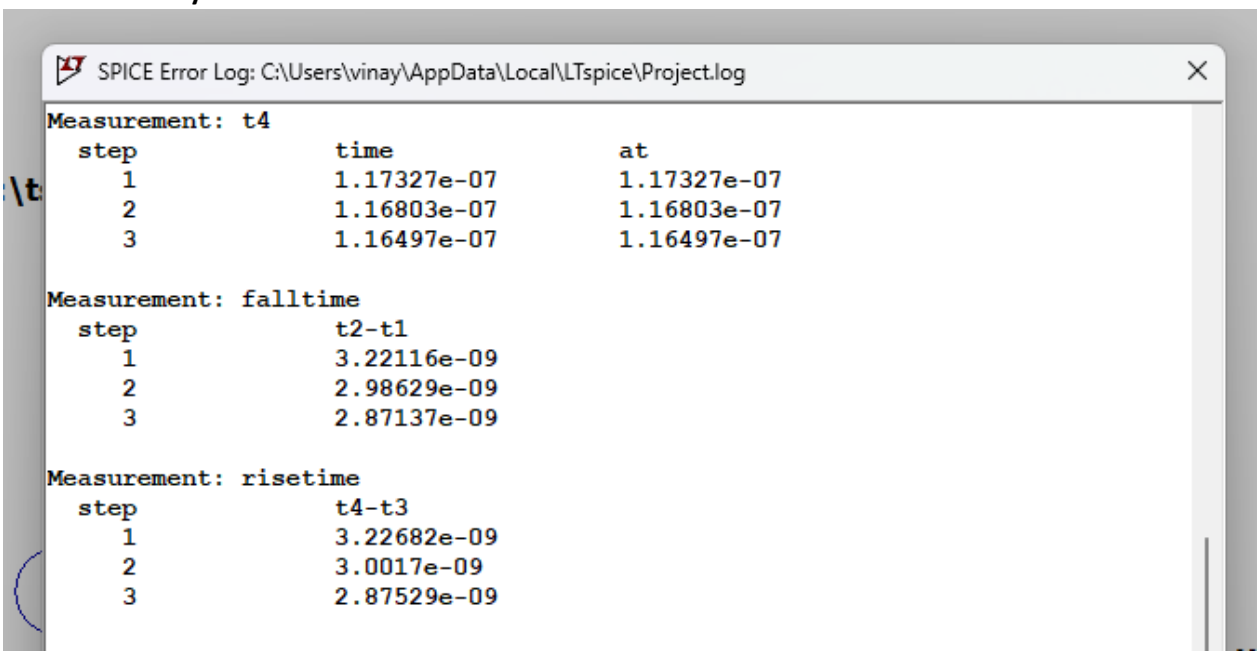
1.b. (Without adding external capacitor)

Carry out transient analysis to find out the rise time and fall time delays of a CMOS inverter sized S =1,2,4, when (i) no external capacitor is attached

(**Note:** Vin is taken as pulse input with **Von=5V**, **Ton=100nsec**, **Tperiod=200nsec**)



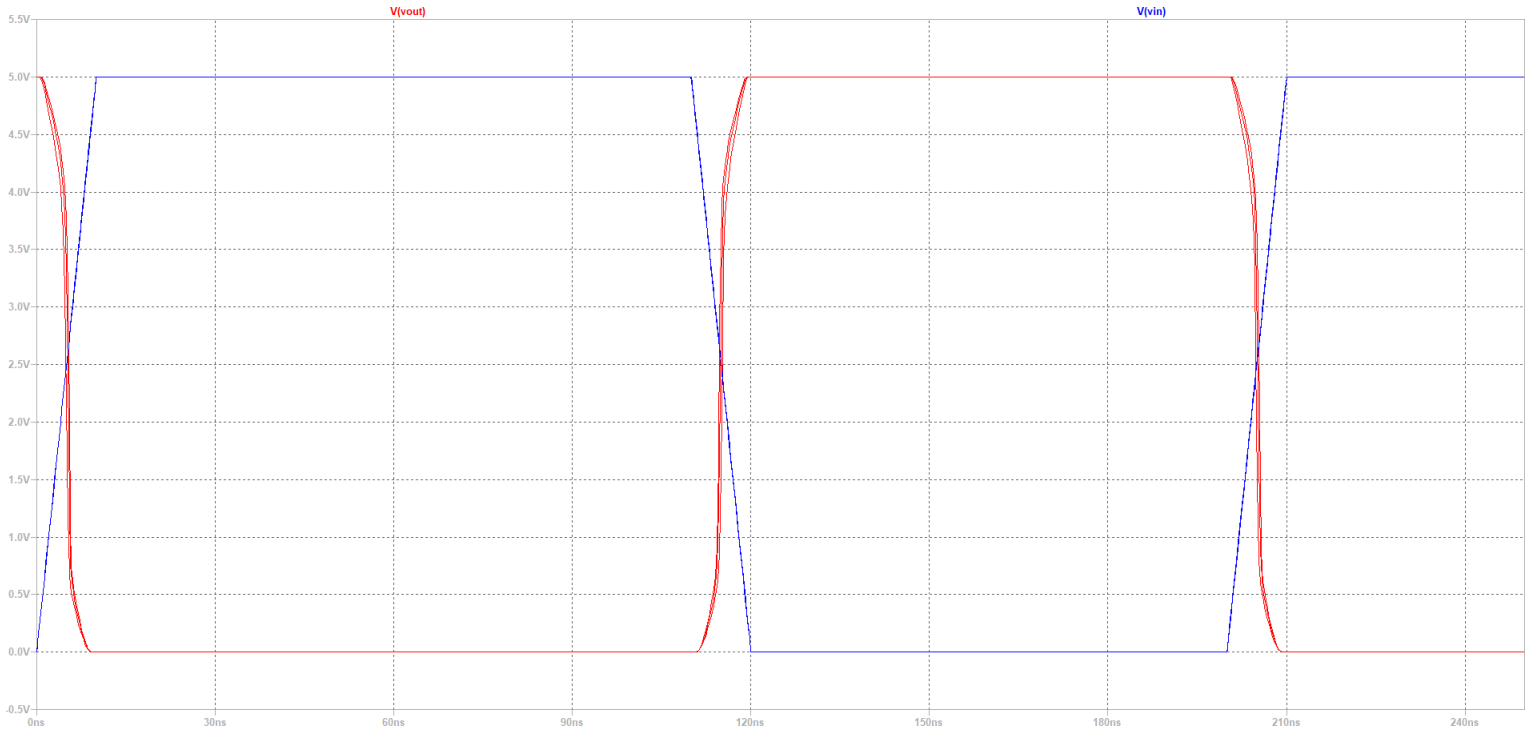
Rise & Fall Delays:



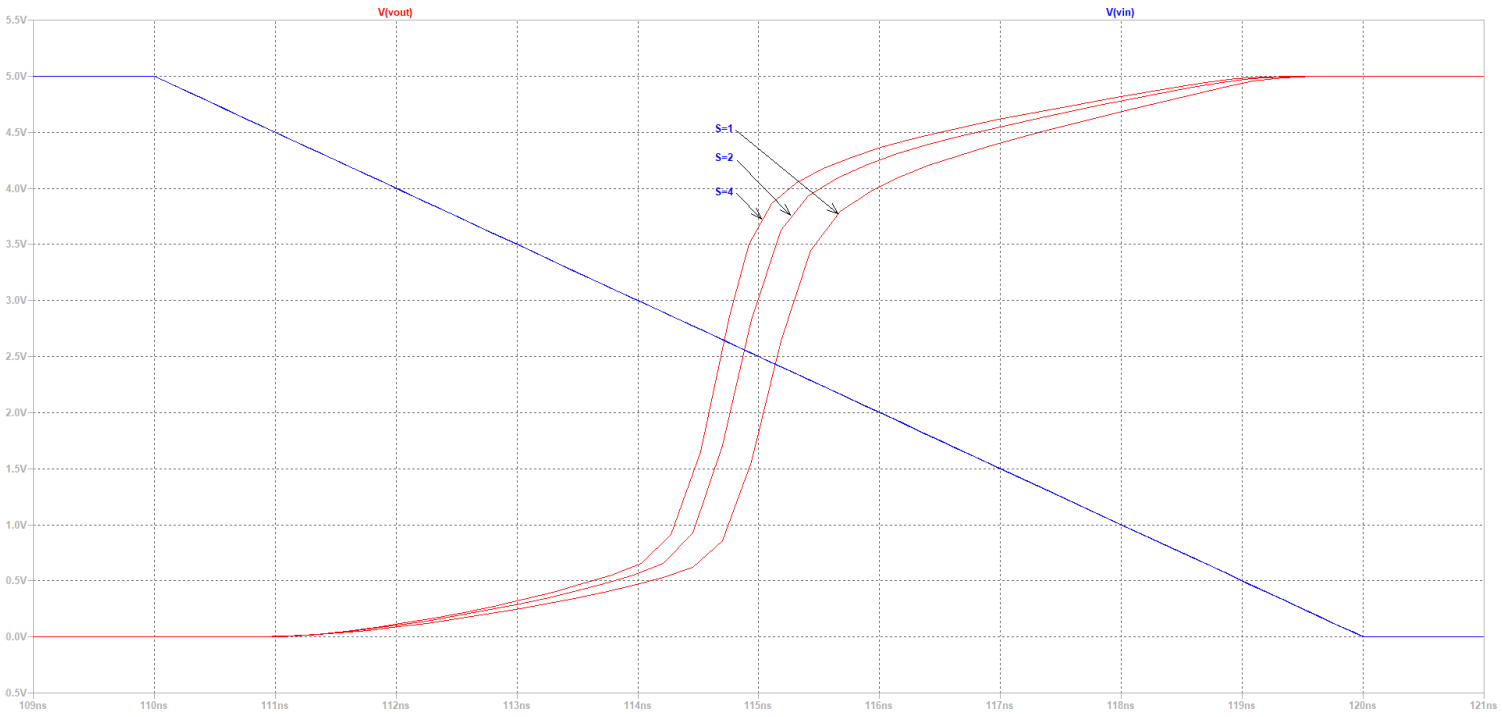
(Note: Delays are listed in order S=1, S=2 & S=4)

(Que) Plot the timing characteristics in a single graph with clearly labelled axes and legends for each value of S

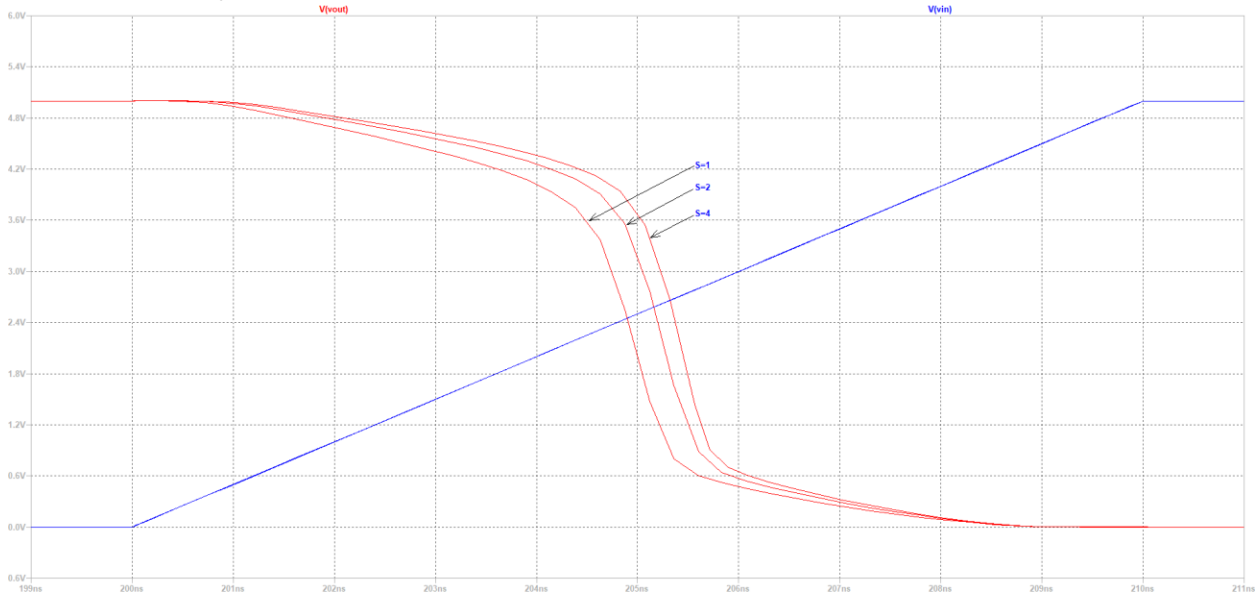
Timing Diagram (Legends for S=1,2 & 4 are shown in Rise time & Fall time figures separately):



Rise Times for S=1,2 & 4:

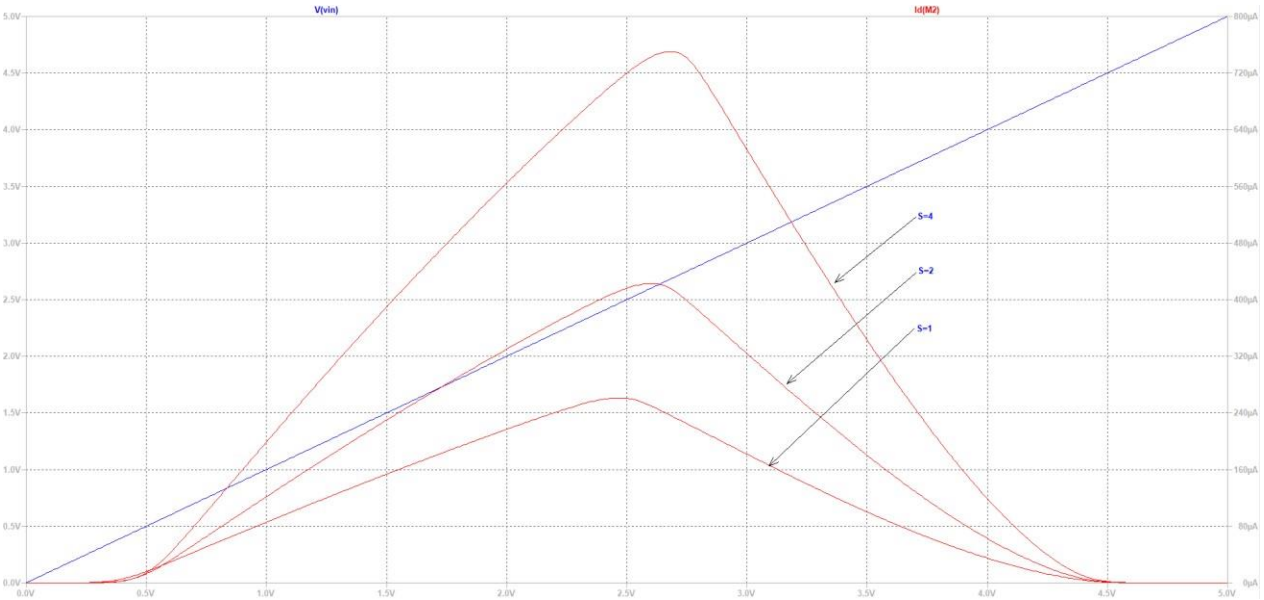


Fall Times for S=1,2 & 4:

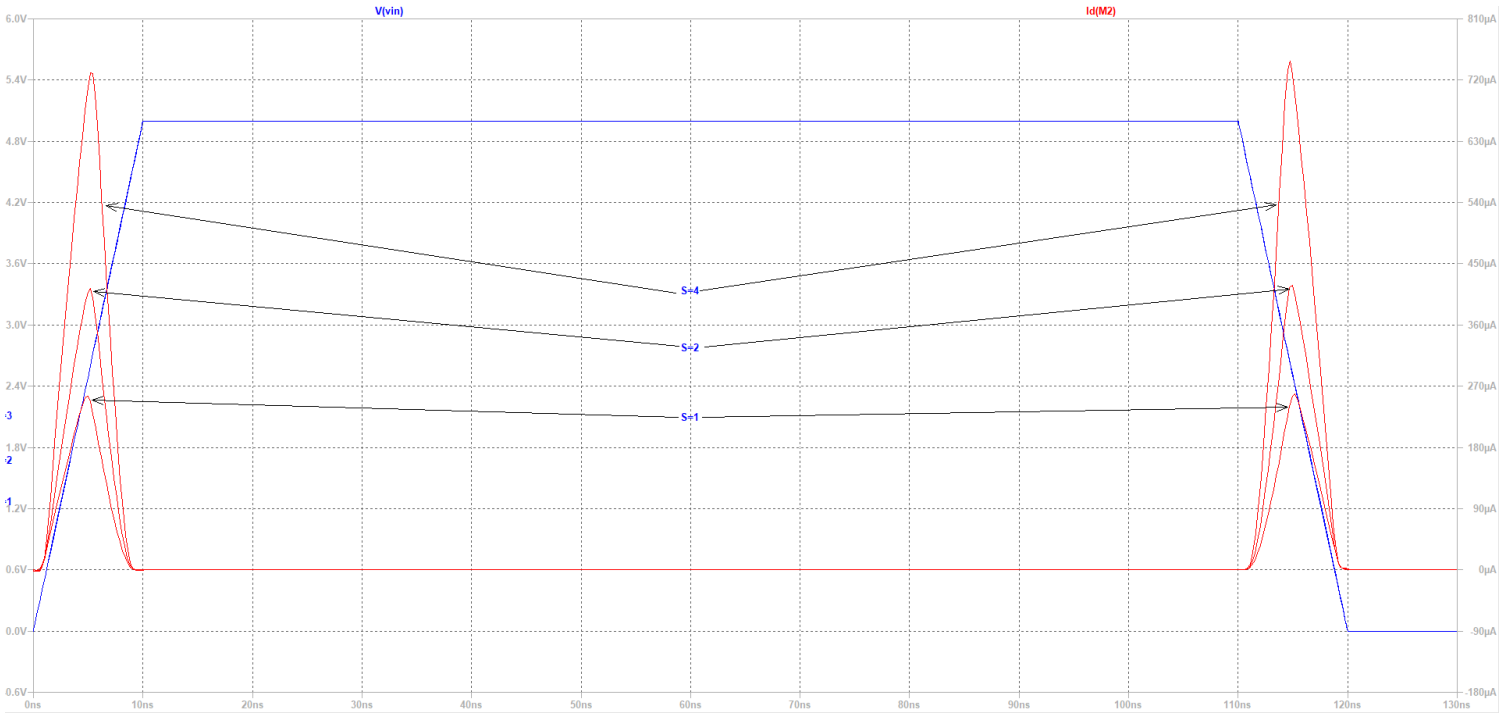


(Que) Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends for each value of S

Input voltage Vs Current (Input voltage Vin swept from 0V to 5V with 0.01V step):



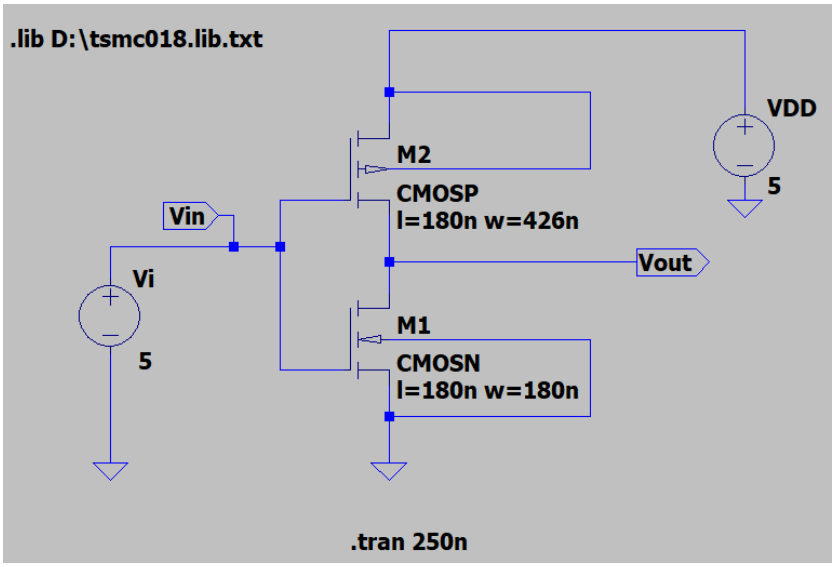
Current Vs Time:



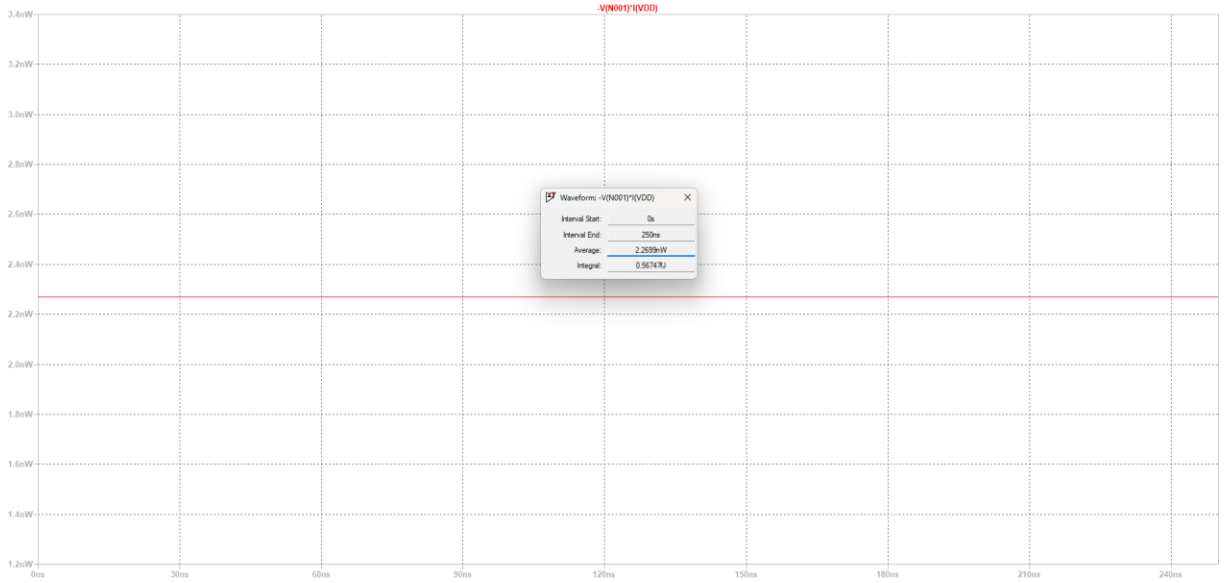
(Que) Calculate and tabulate the static and dynamic power dissipations in all cases, i.e., for each value of S and for part (i) and (ii).

Static Power: Static power is calculated as: Average powers are calculated for Vin = 0V & Vin = 5V by doing DC analysis. The results are then averaged.

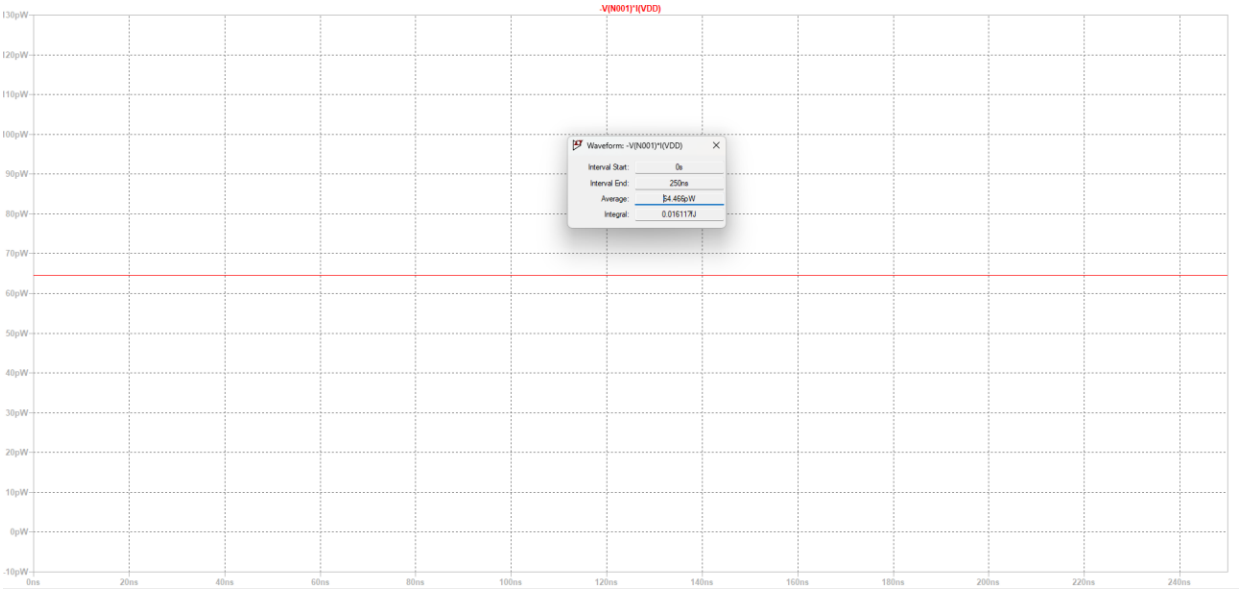
S=1:



Power @ Vin=0V: Power: 2.2699nW



Power @ Vin=5V: Power: 64.466pW



Static Power: (2.2699nW+64.466pW)/2=1.671nW

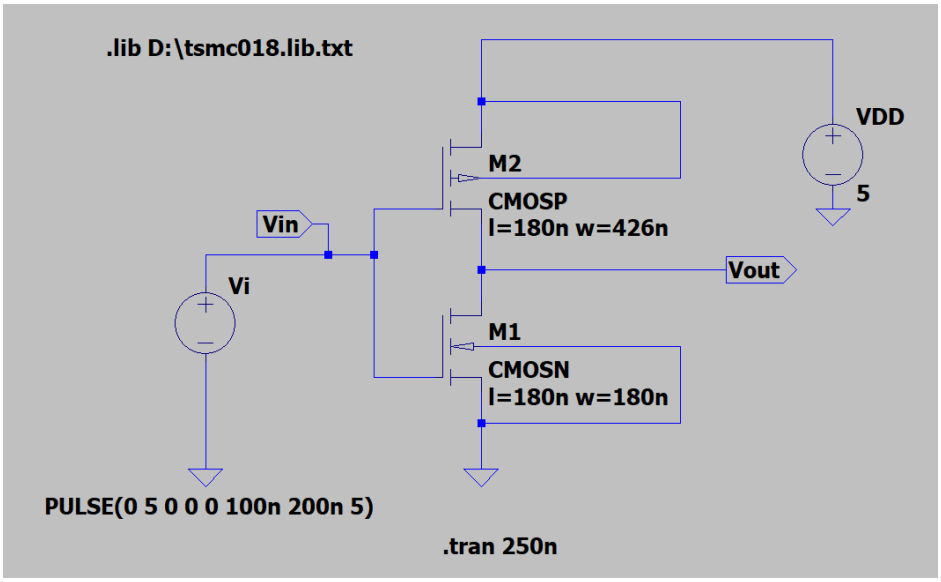
Similarly Static Power for S=1, S=2 & S=4 is calculated and tabulated as follows:

Sr. No.	S	Power @ Vin = 0V	Power @ Vin = 5V	Static Power
1	1	2.2699nW	64.466pW	1.167nW
2	2	561.35pW	67.019pW	0.314nW
3	4	381.32pW	86.055pW	0.233nW

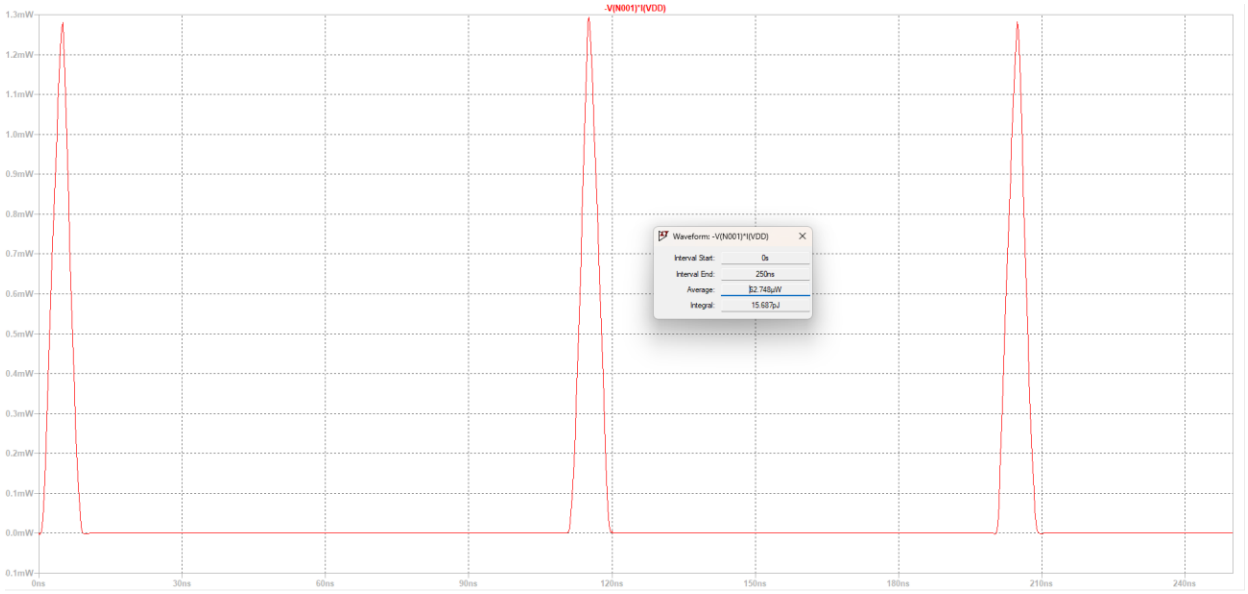
Dynamic Power: Dynamic power is calculated by pulsed input & calculating the power during output transition time.

S=1

Circuit:



Power: 62.748µW



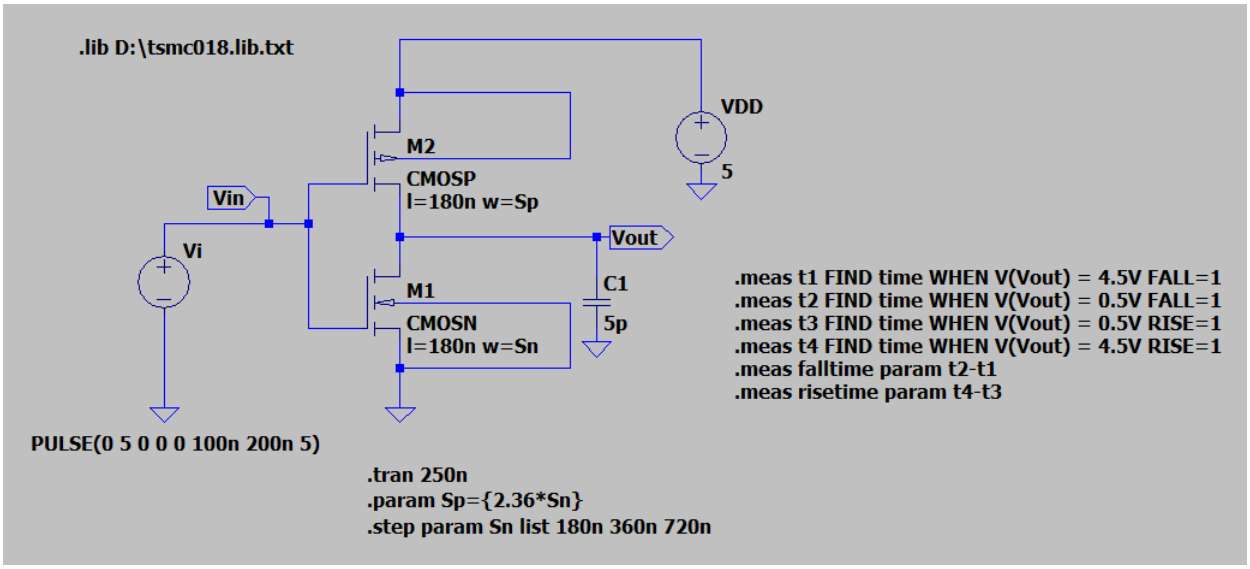
Similarly Dynamic Power for S=1, S=2 & S=4 is calculated and tabulated as follows:

Sr. No.	S	Dynamic Power
1	1	62.748µW
2	2	100.84µW
3	4	178.61µW

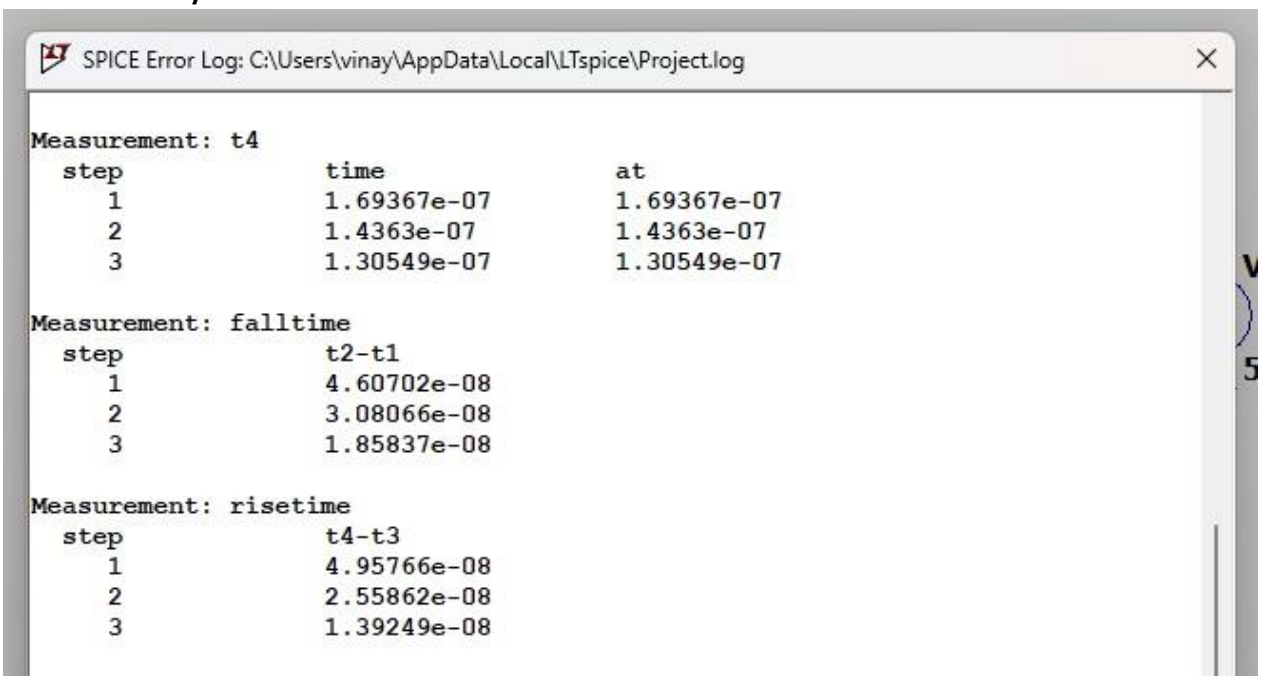
1.b. (With 5pF external capacitor)

Carry out transient analysis to find out the rise time and fall time delays of a CMOS inverter sized S =1,2,4, when (ii) an external capacitor of 5 pF is attached to the output node.

(**Note:** Vin is taken as pulse input with **Von=5V**, **Ton=100nsec**, **Tperiod=200nsec**)



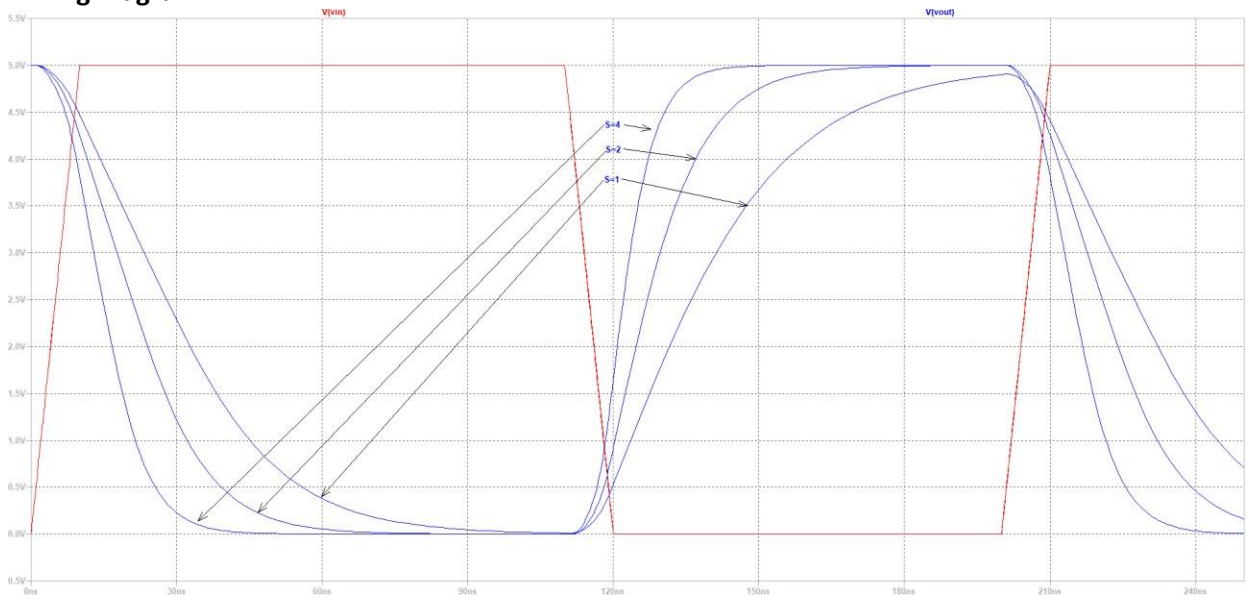
Rise & Fall Delays:



(Note: Delays are listed in order S=1, S=2 & S=4)

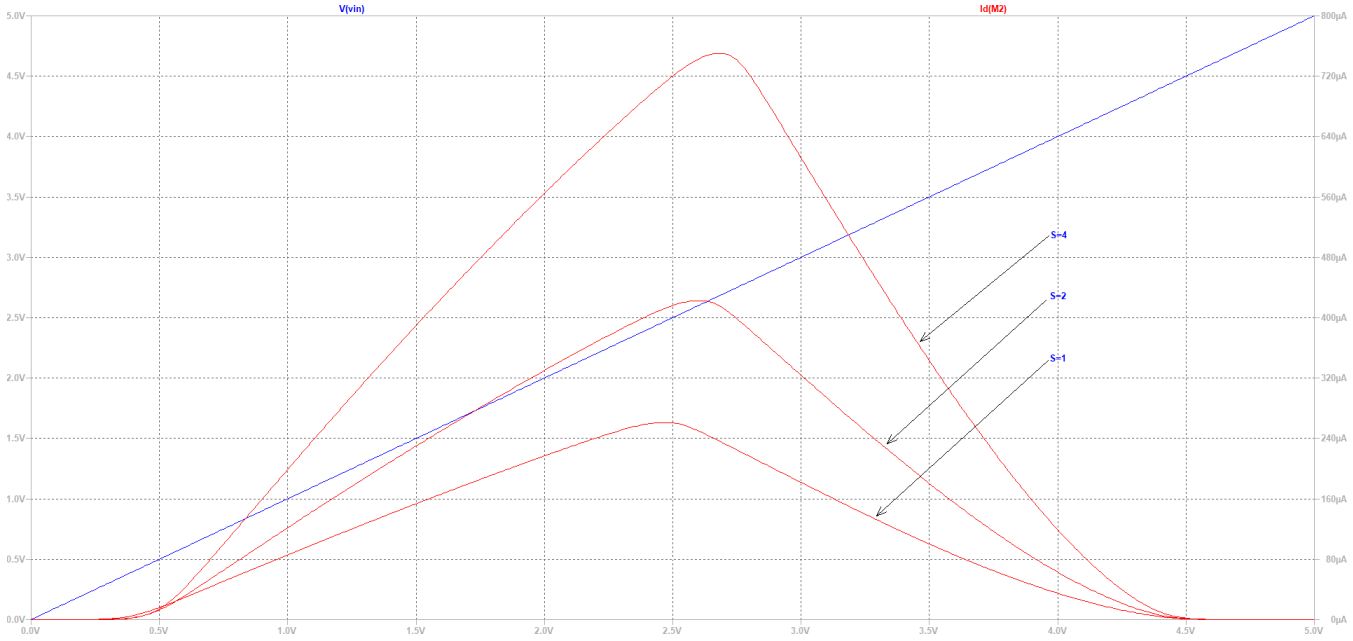
(Que) Plot the timing characteristics in a single graph with clearly labelled axes and legends for each value of S

Timing Diagram:

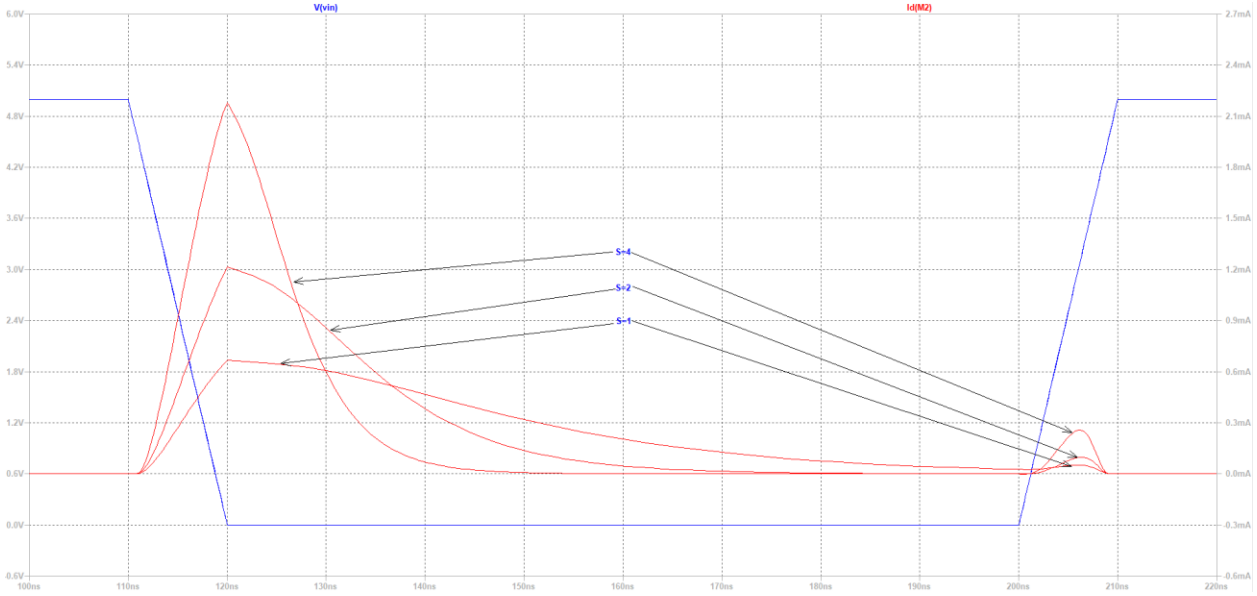


(Que) Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends for each value of S

Input voltage Vs Current (Input voltage Vin swept from 0V to 5V with 0.01V step):



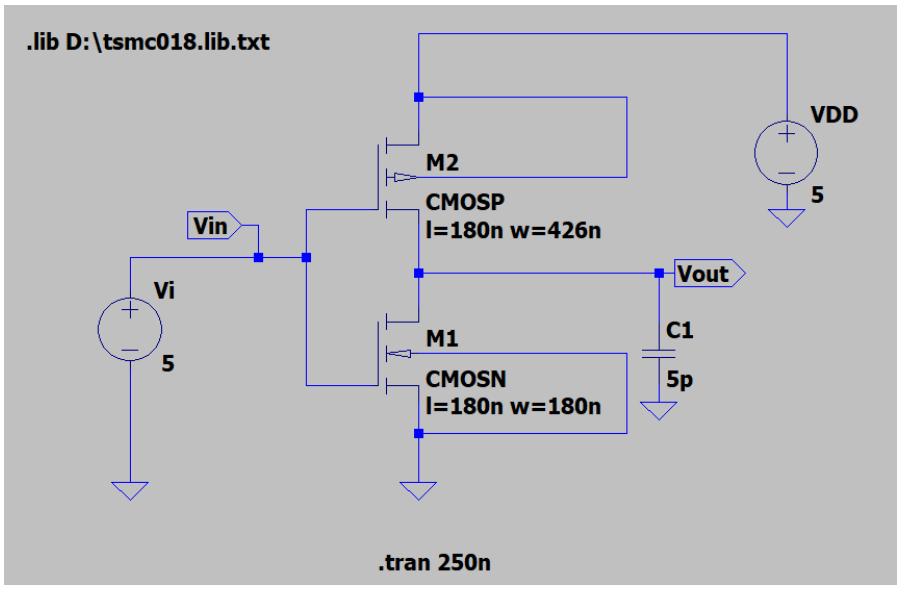
Current Vs Time:



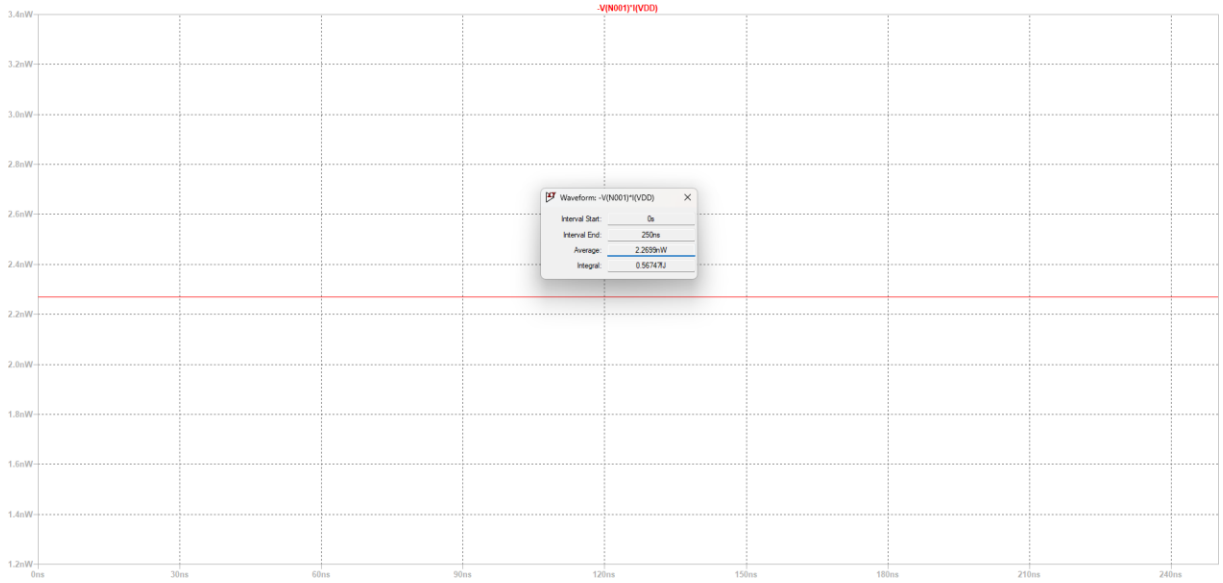
(Que) Calculate and tabulate the static and dynamic power dissipations in all cases, i.e., for each value of S and for part (i) and (ii).

Static Power: Static power is calculated as: Average powers are calculated for Vin = 0V & Vin = 5V by doing DC analysis. The results are then averaged.

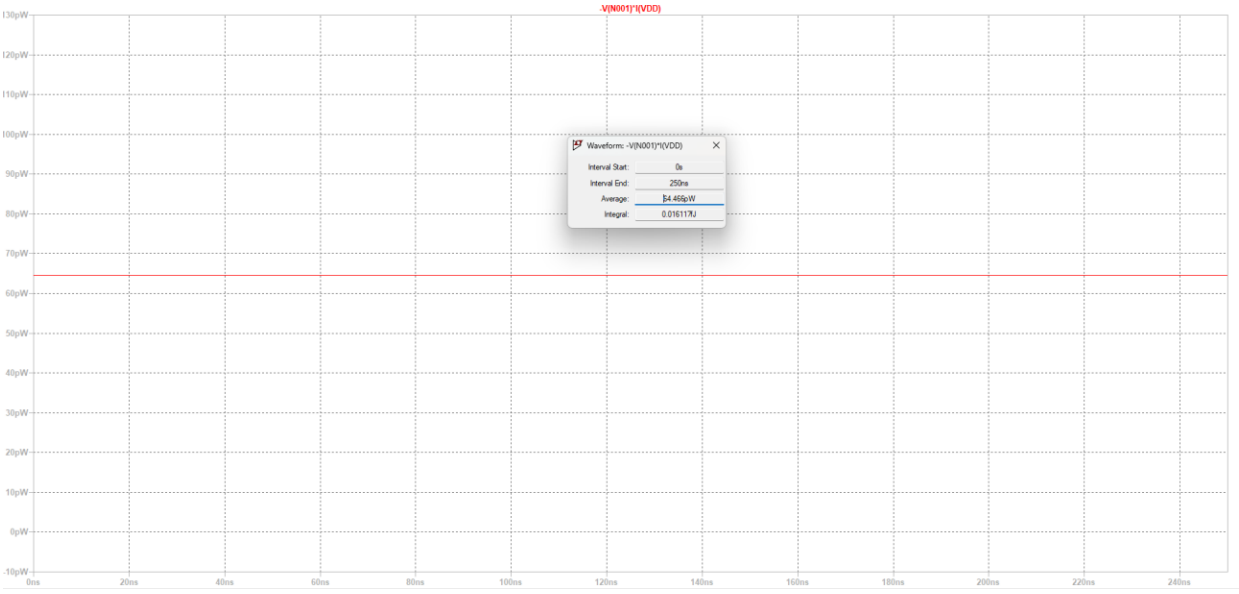
S=1:



Power @ Vin=0V: Power: 2.2699nW



Power @ Vin=5V: Power: 64.466pW



Static Power: (2.2699nW+64.466pW)/2=1.671nW

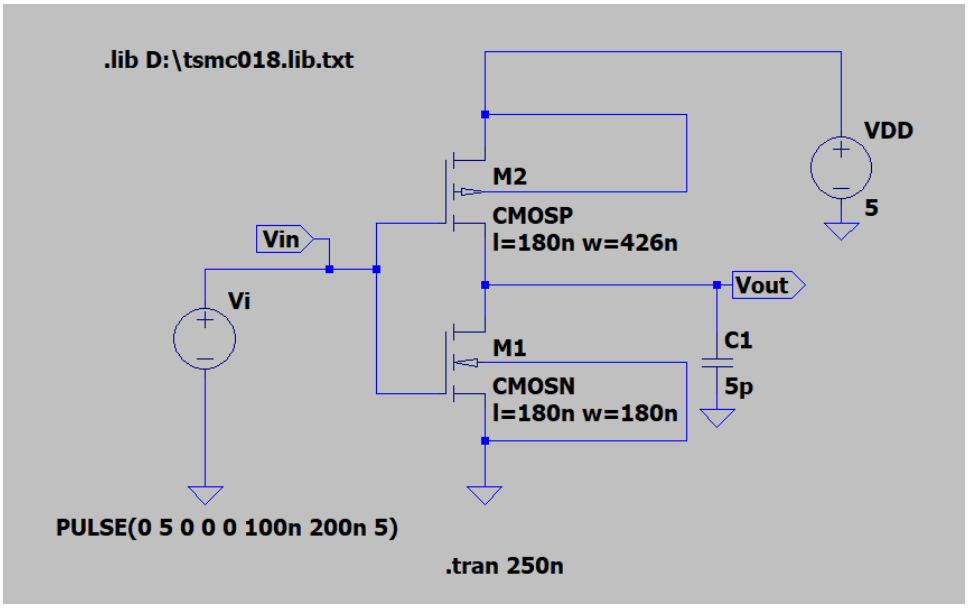
Similarly Static Power for S=1, S=2 & S=4 is calculated and tabulated as follows:

Sr. No.	S	Power @ Vin = 0V	Power @ Vin = 5V	Static Power
1	1	2.2699nW	64.466pW	1.167nW
2	2	561.35pW	67.019pW	1.168nW
3	4	381.32pW	86.055pW	1.177nW

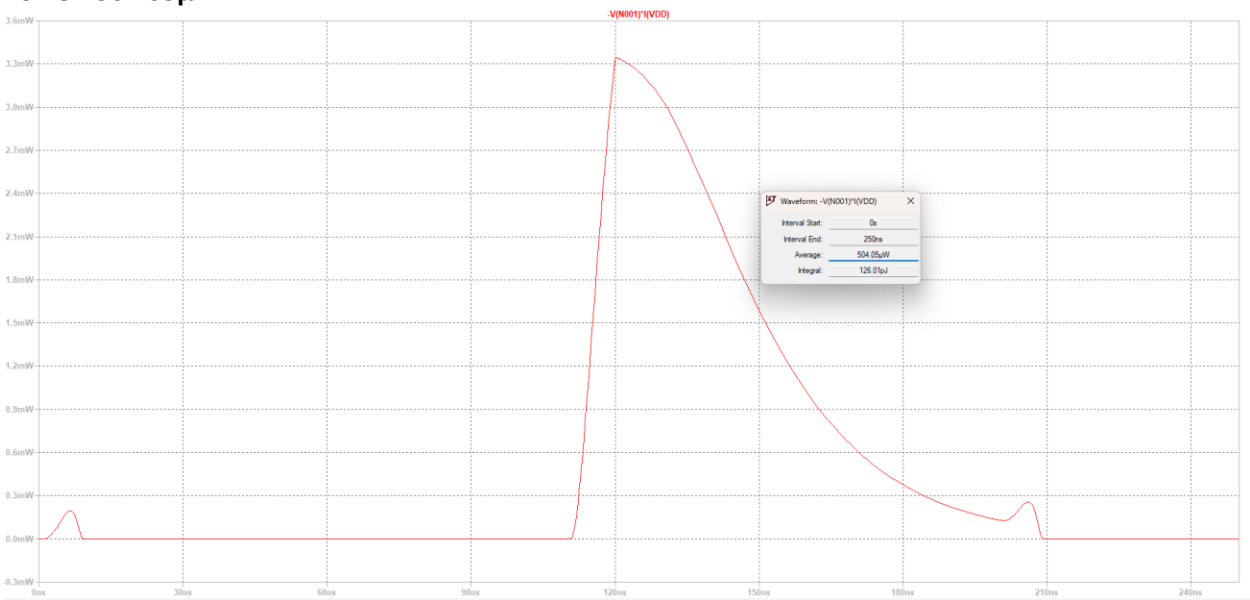
Dynamic Power: Dynamic power is calculated by pulsed input & calculating the power during output transition time.

S=1

Circuit:



Power: 504.05µW



Similarly Dynamic Power for S=1, S=2 & S=4 is calculated and tabulated as follows:

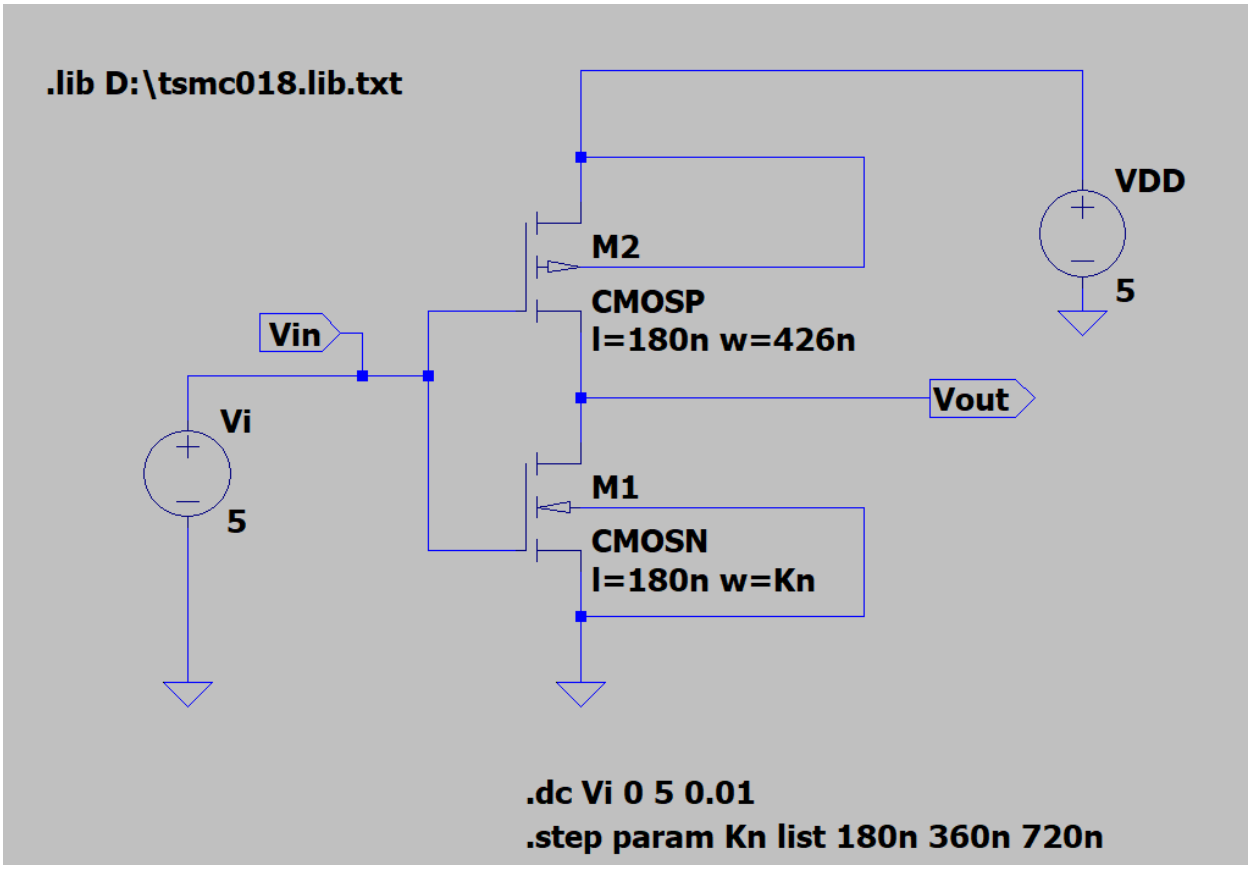
Sr. No.	S	Dynamic Power
1	1	504.05µW
2	2	526.77µW
3	4	568.11µW

1.c.

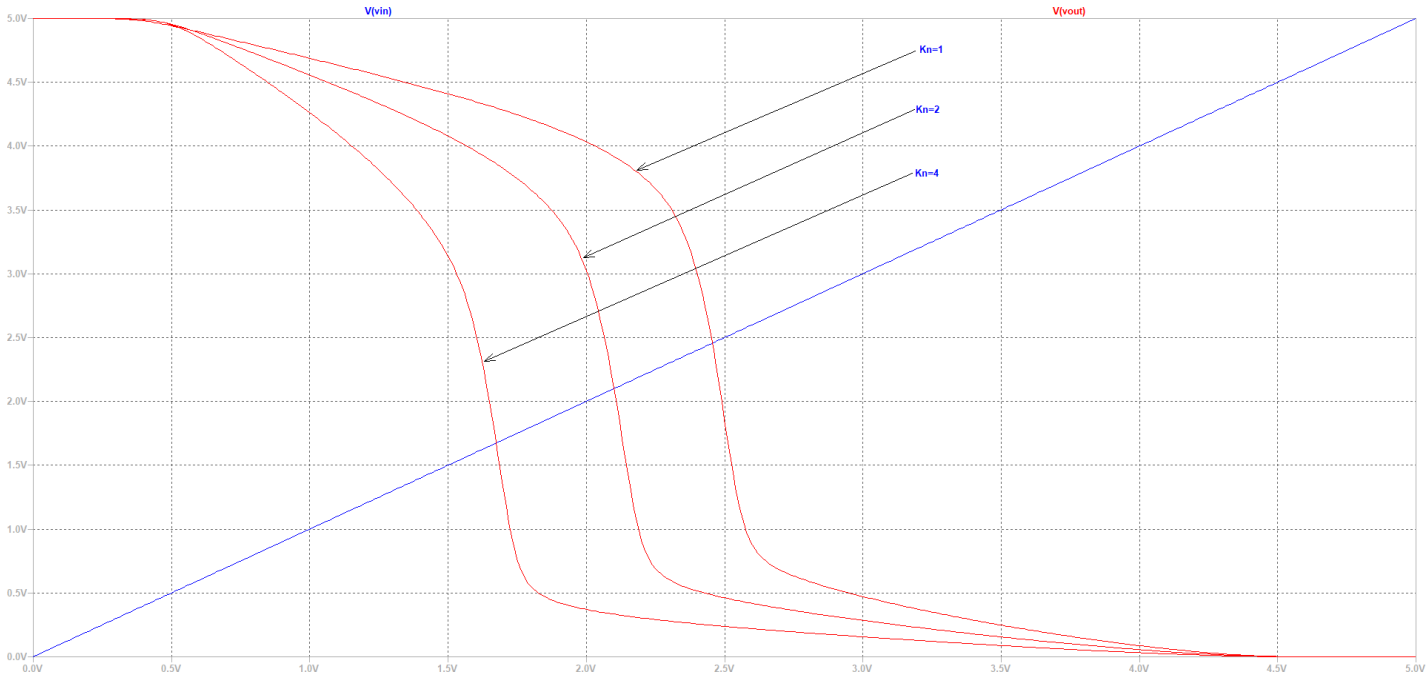
(Que) Simulate the static VTC of an inverter in which the NMOS is sized Kn times the size of the corresponding NMOS of the minimum-sized inverter for Kn = 1,2,4, keeping the size of the PMOS the same as that of the corresponding PMOS of the minimum-sized inverter.

Circuit:

(For Kn=1 - Wp=180nm, Kn=2 - Wp=360nm, Kn=4 - Wp=720nm)

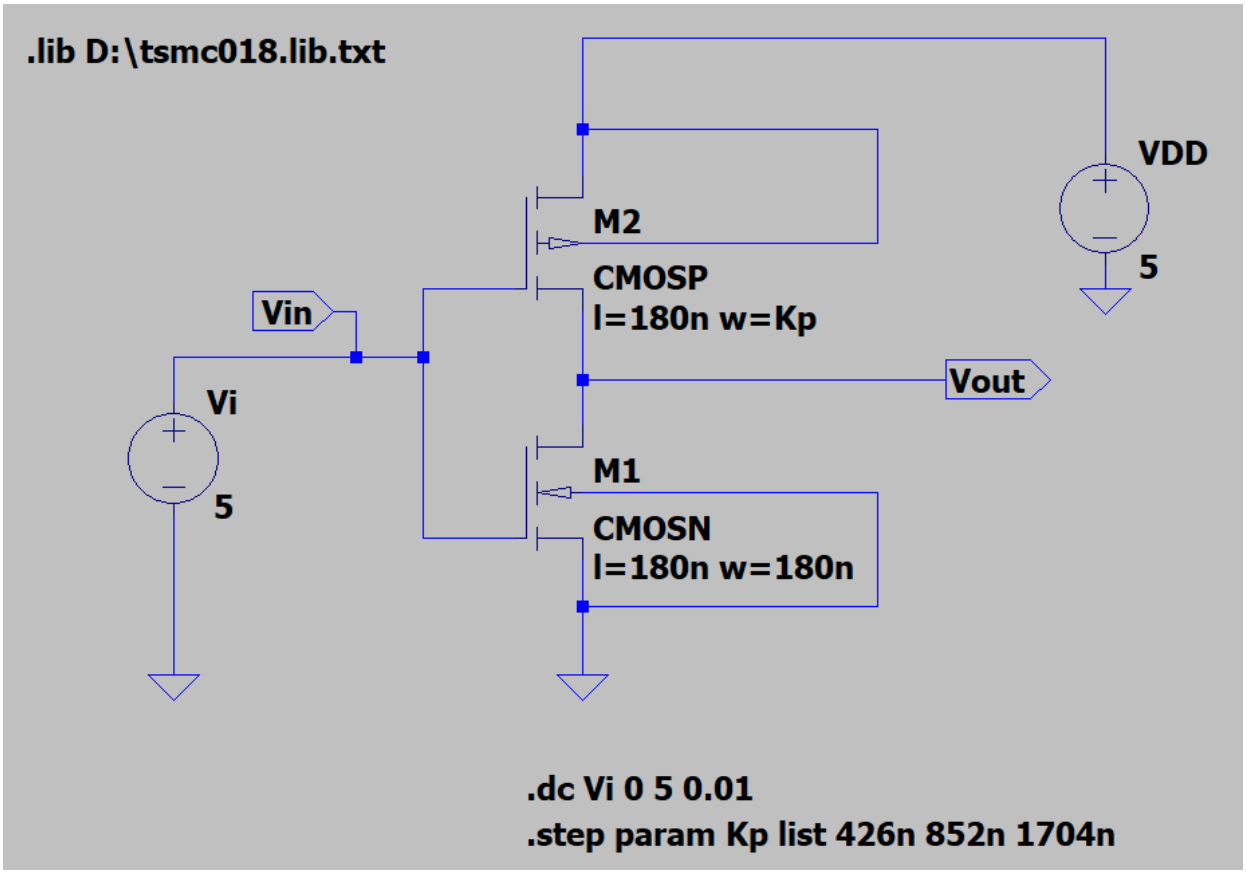


VTC:

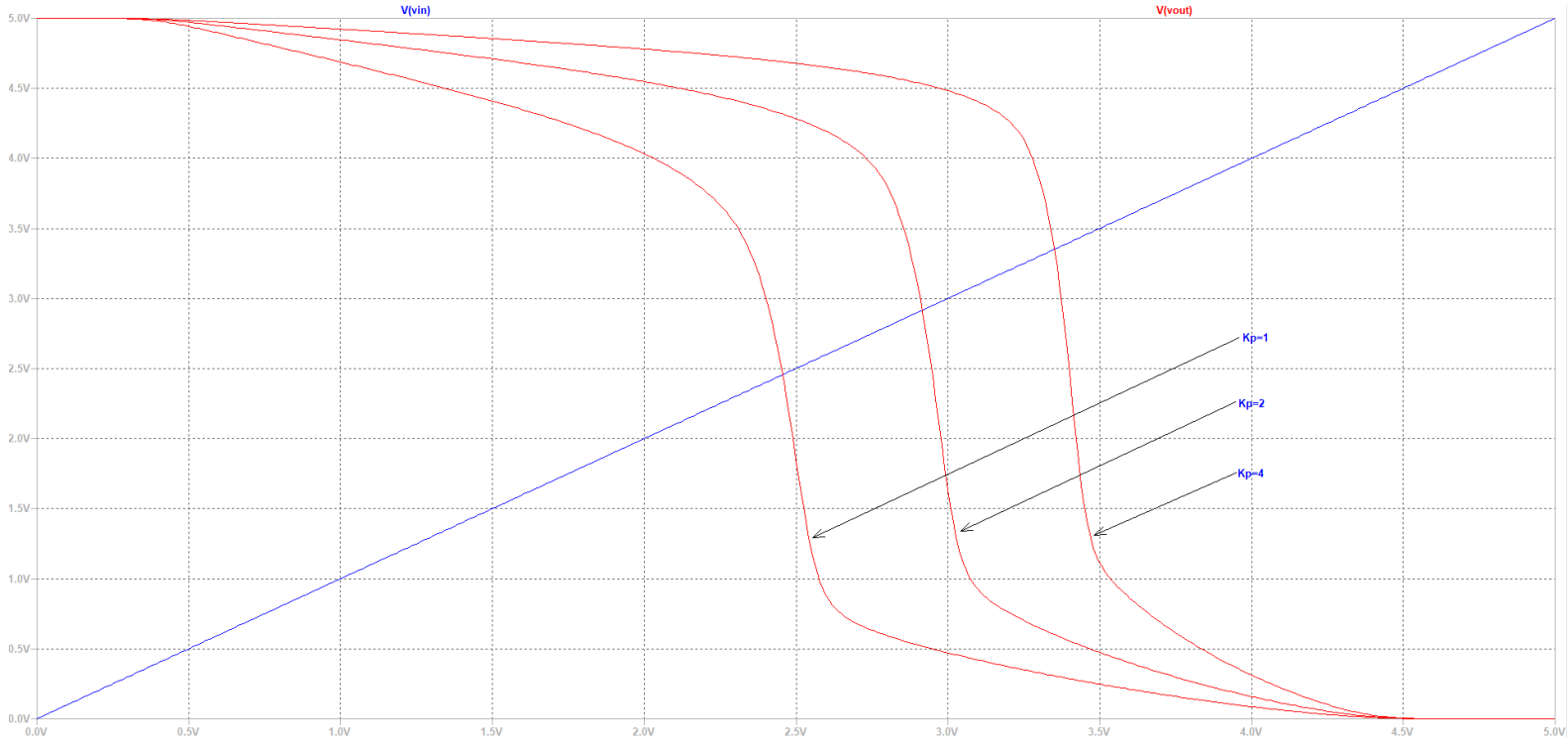

V(vin)
V(vout)
Kn=1
Kn=2
Kn=4
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V

(Que) Similarly, simulate the static VTC of an inverter in which the PMOS is sized Kp times the size of the corresponding PMOS of the minimum-sized inverter for Kp = 1,2,4, keeping the size of the NMOS the same as that of the corresponding NMOS of the minimum-sized inverter.

Circuit:
(For Kp=1 - Wp=426nm, Kp=2 - Wp=852nm, Kp=4 - Wp=1704nm)



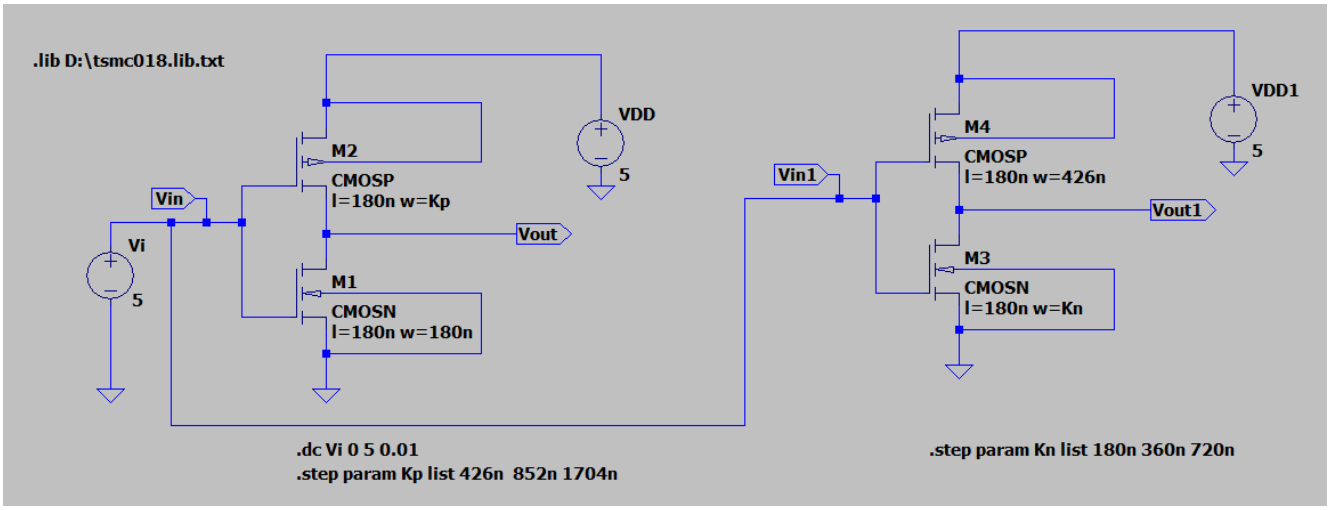
VTC:



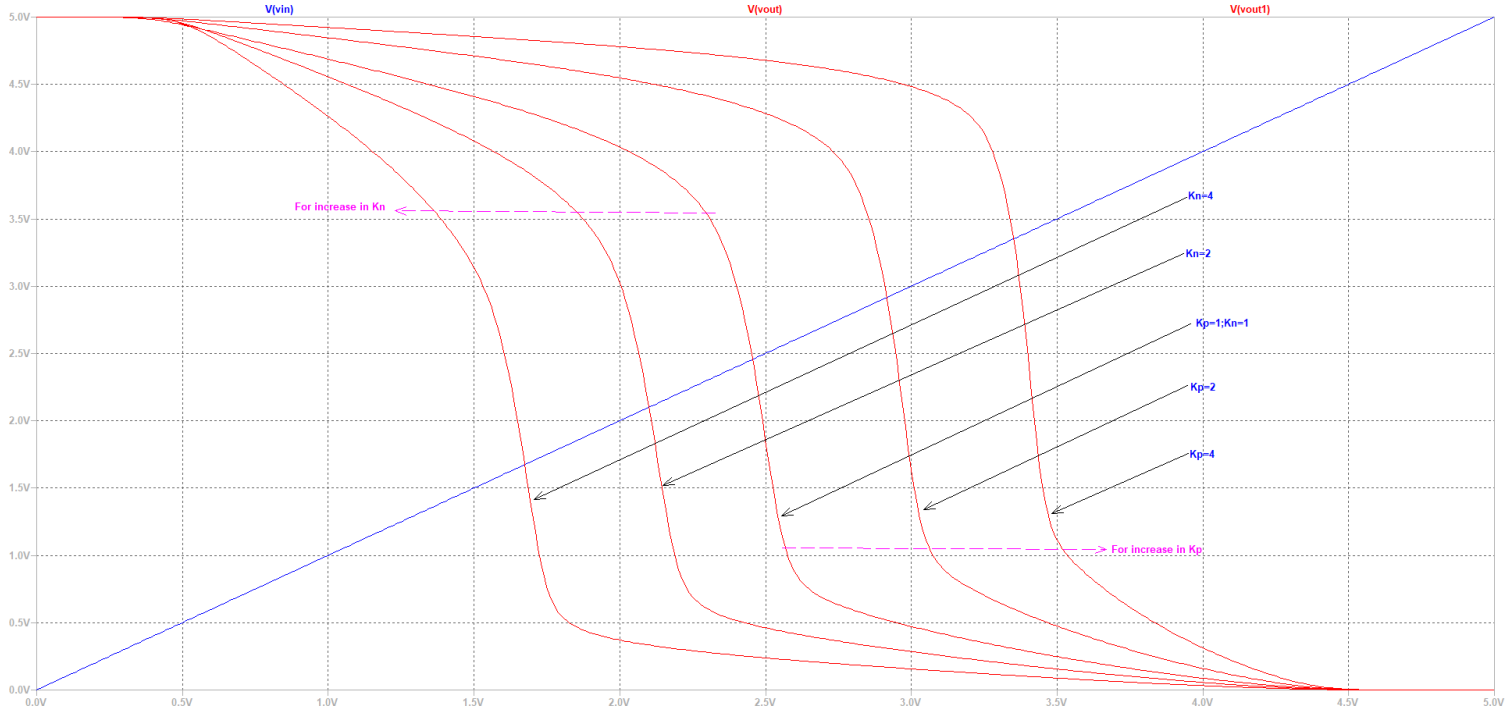
(Que) Plot all these VTCs in a single graph with clear legends indicating how sizing of skewed CMOS inverter affects the VTC.

To plot all VTCs together, CMOS inverter circuit is duplicated. In 1st circuit, Wn is kept constant that of minimum sized inverter (180nm) & Kp is varied. In 2nd circuit, Wp is kept constant that of minimum sized inverter (426nm) & Kn is varied.

Circuit:



VTC:



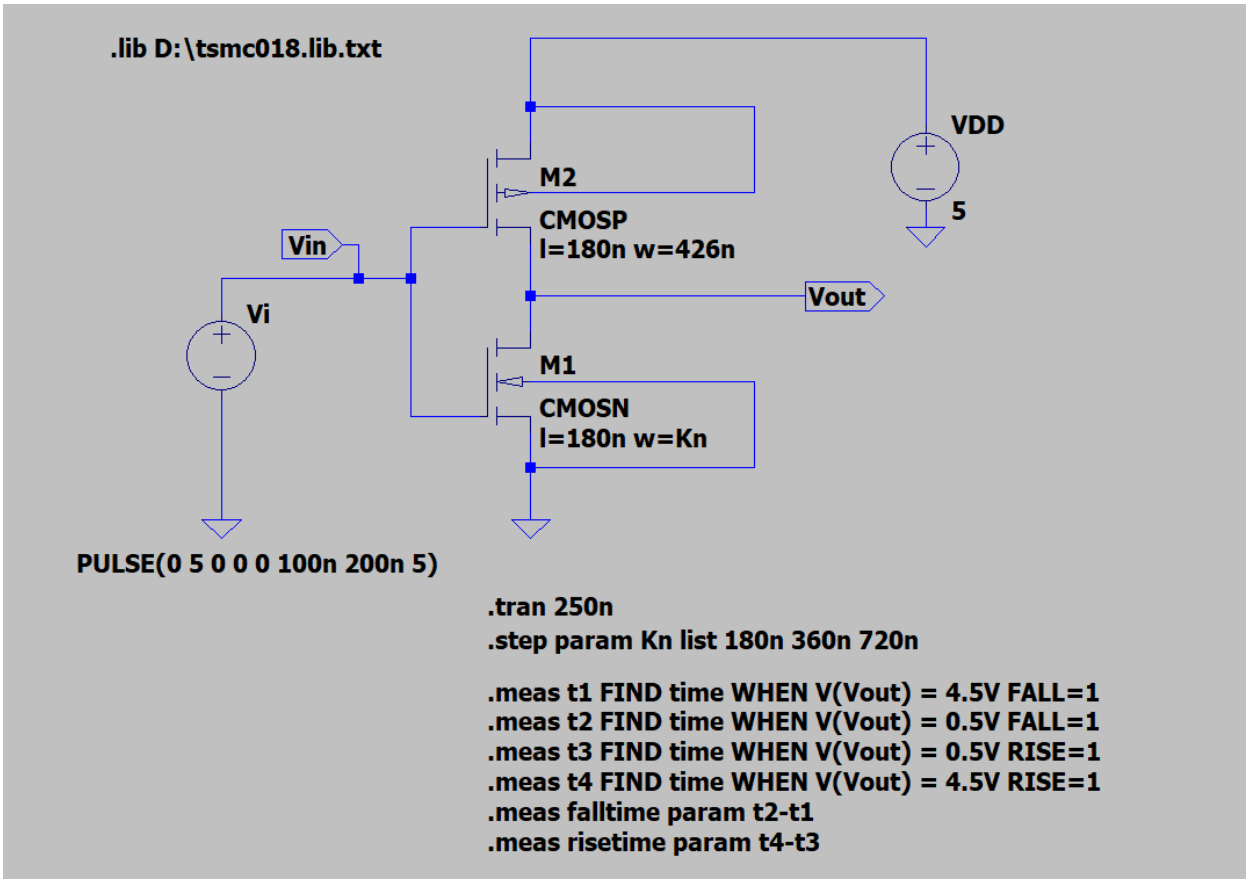
Observation: VTC shifts to left for increasing Kn values & shifts to right for increasing Kp values.

1.d.

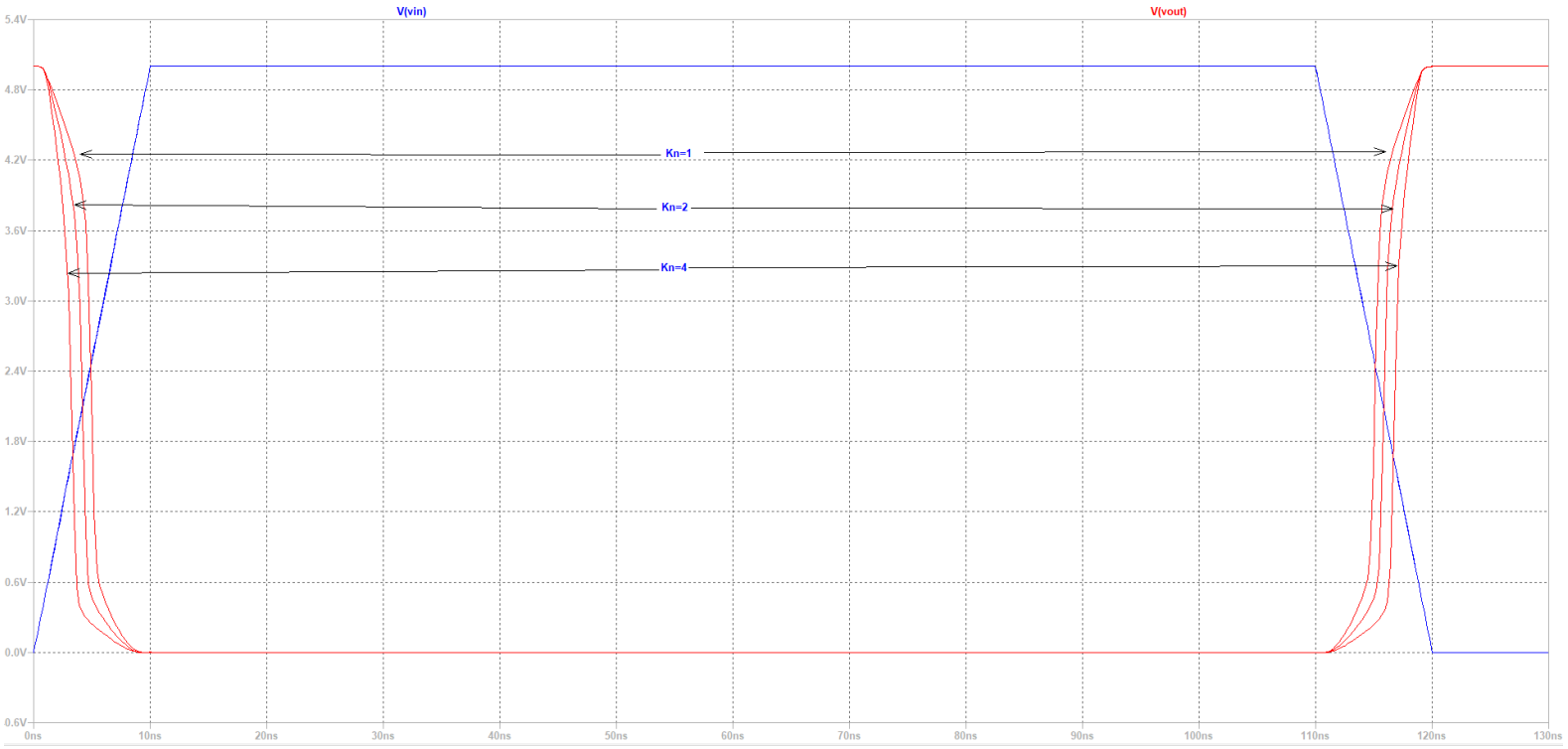
(Que) Carry out transient analysis to find out the rise time and fall time delays in each case when **Case (i) no external capacitor is attached**

Part(i) Kn is varied

Circuit:



Timing Diagram:



(Que) Tabulate the rise time and fall time delays obtained.

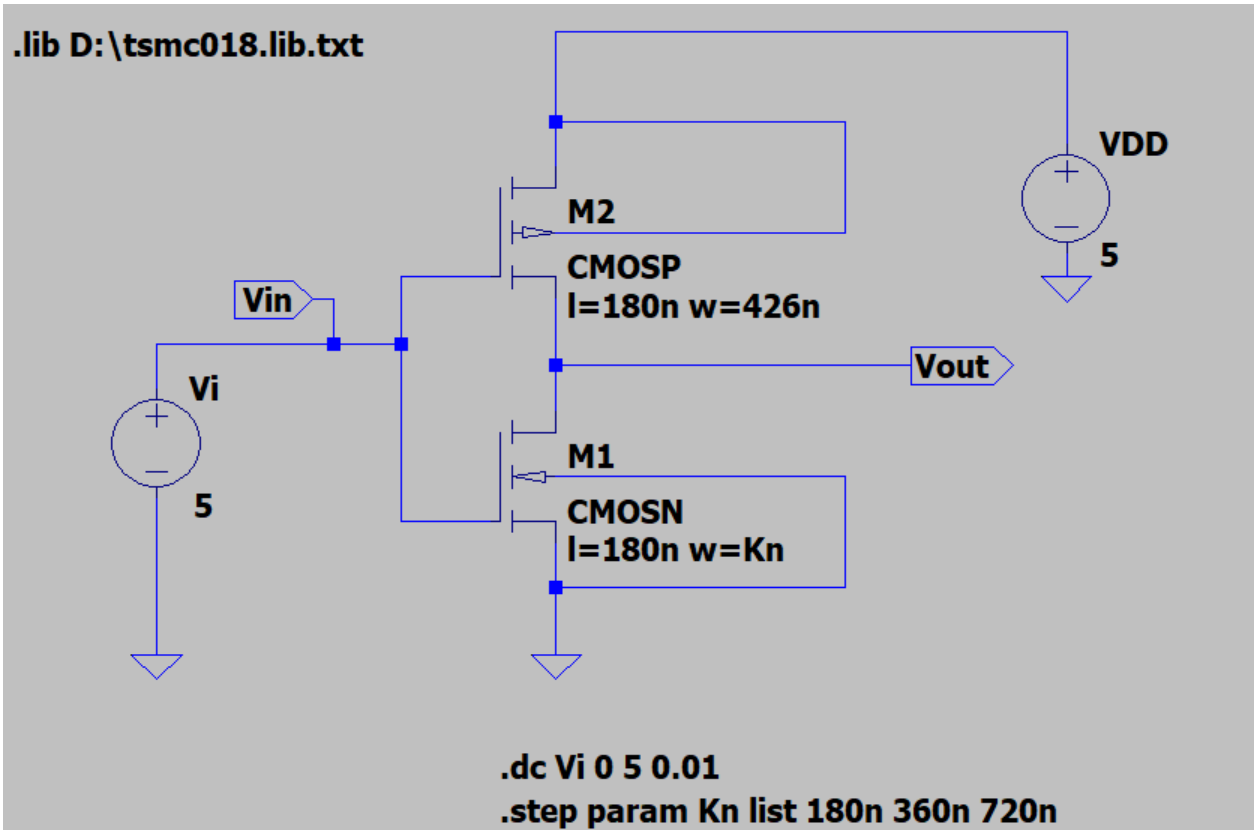
Rise & Fall Times: (For Kn=1, Kn=2, Kn=4)

SPICE Error Log: C:\Users\vinay\AppData\Local\LTspice\Project.log

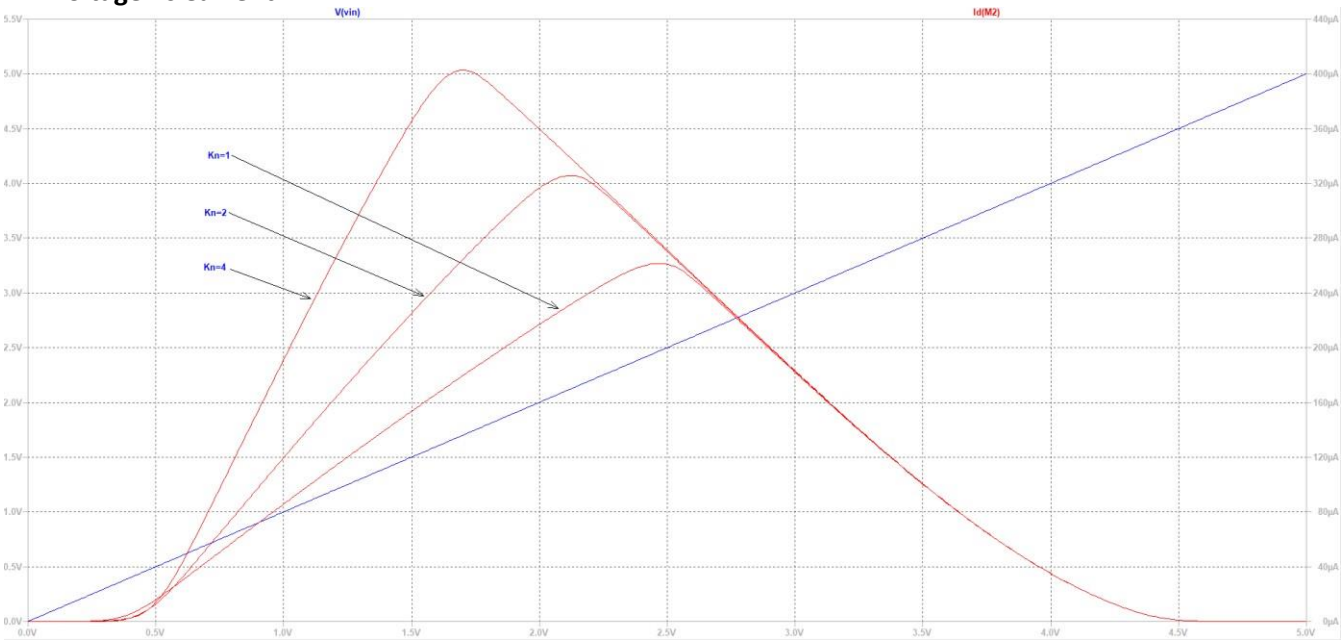
```
Measurement: t4
  step            time            at
     1            1.17322e-07     1.17322e-07
     2            1.17885e-07     1.17885e-07
     3            1.18318e-07     1.18318e-07

Measurement: falltime
  step            t2-t1
     1            3.22017e-09
     2            2.77454e-09
     3            2.0887e-09

Measurement: risetime
  step            t4-t3
     1            3.22665e-09
     2            2.77031e-09
     3            2.10259e-09
```

(Que) Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends.

Circuit: (Kn is varied)



Voltage Vs Current:



Static & Dynamic Power Tables:

(**Note:** Static & Dynamic powers are calculated using same process as that of question 1.b part)

Static Power:

Static Power for Kn=1, Kn=2 & Kn=4 is calculated and tabulated as follows:

Sr. No.	Kn	Power @ Vin = 0V	Power @ Vin = 5V	Static Power
1	1	2.2699nW	64.466pW	1.167nW
2	2	561.35pW	64.466pW	0.313nW
3	4	381.32pW	64.466pW	0.223nW

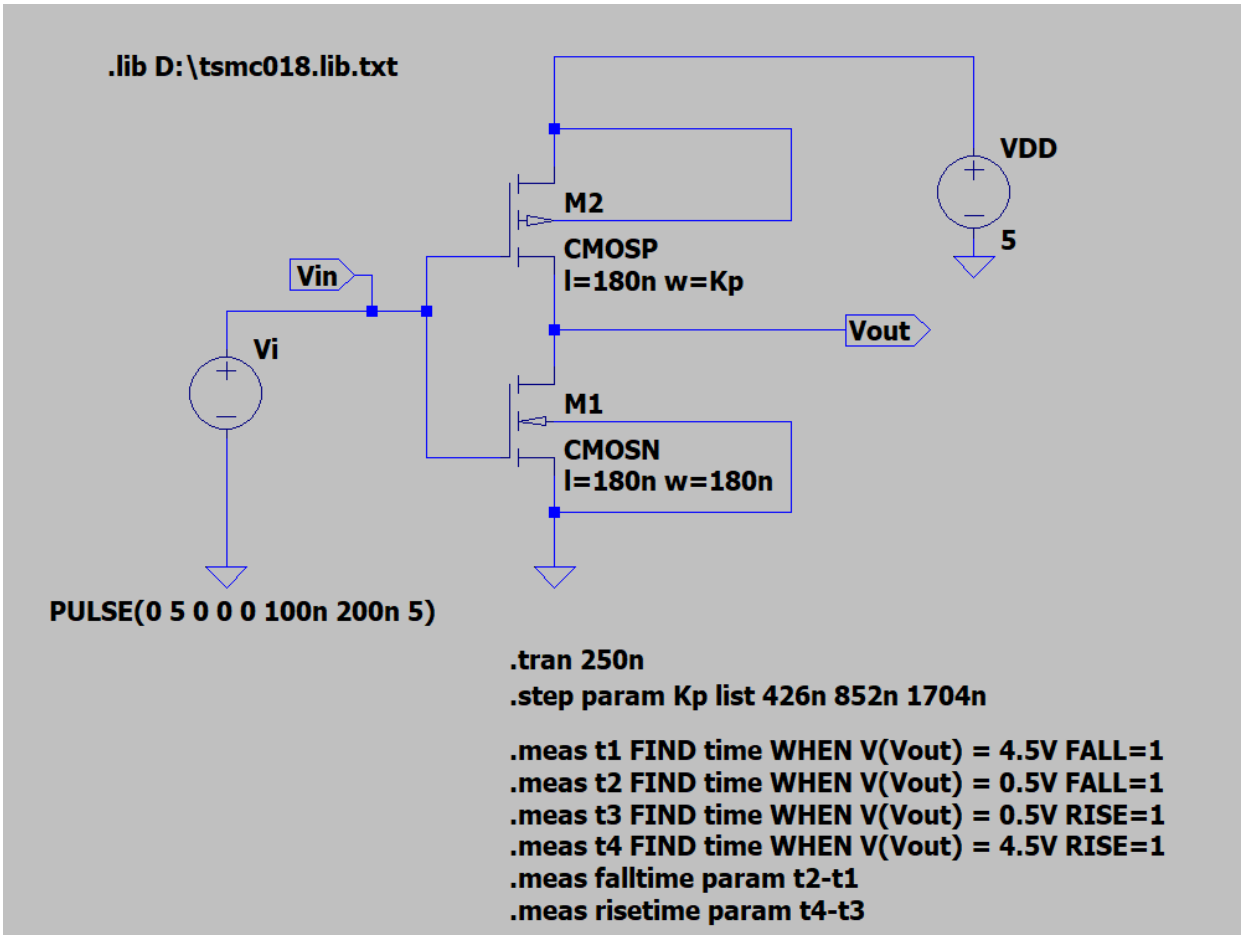
Dynamic Power:

Dynamic Power for Kn=1, Kn=2 & Kn=4 is calculated and tabulated as follows:

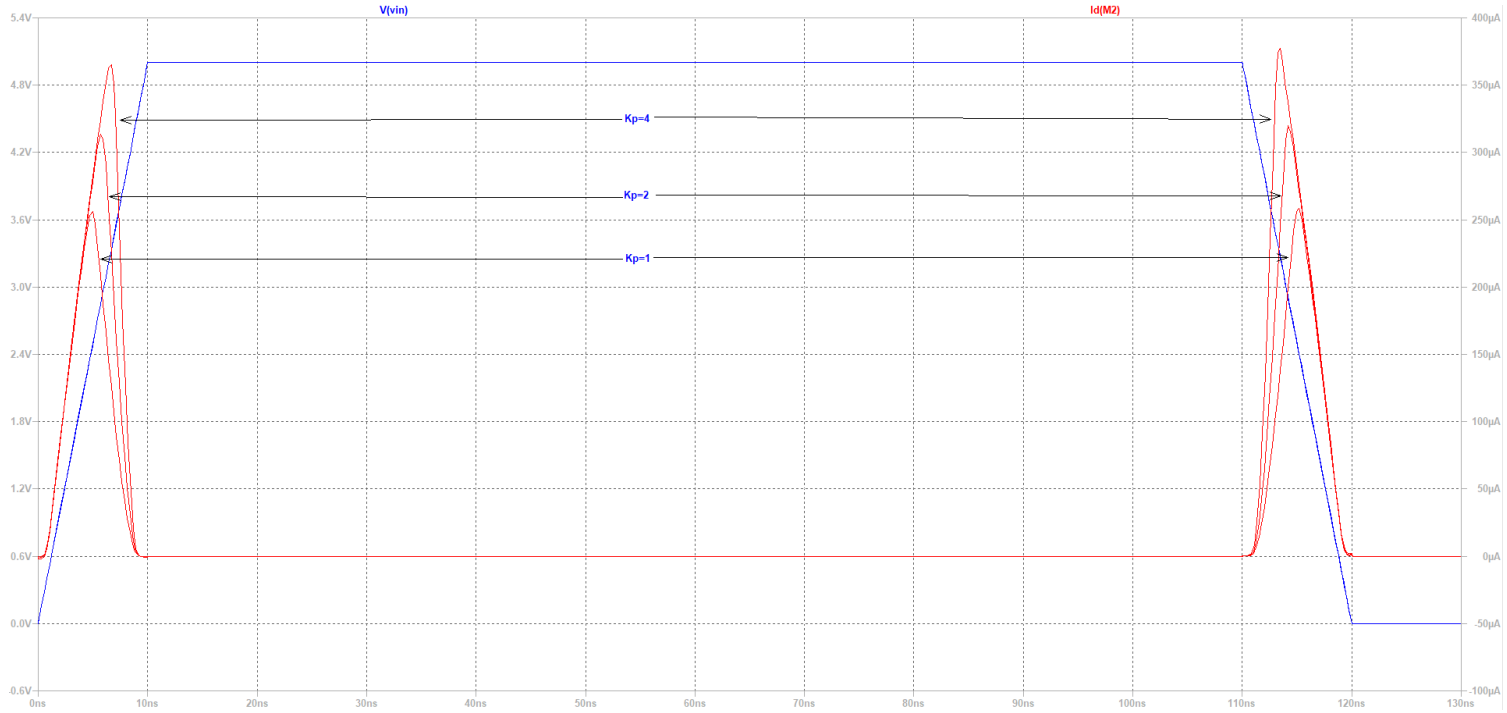
Sr. No.	Kn	Dynamic Power
1	1	62.748µW
2	2	75.891µW
3	4	91.733µW

Part(i) Kp is varied

Circuit:

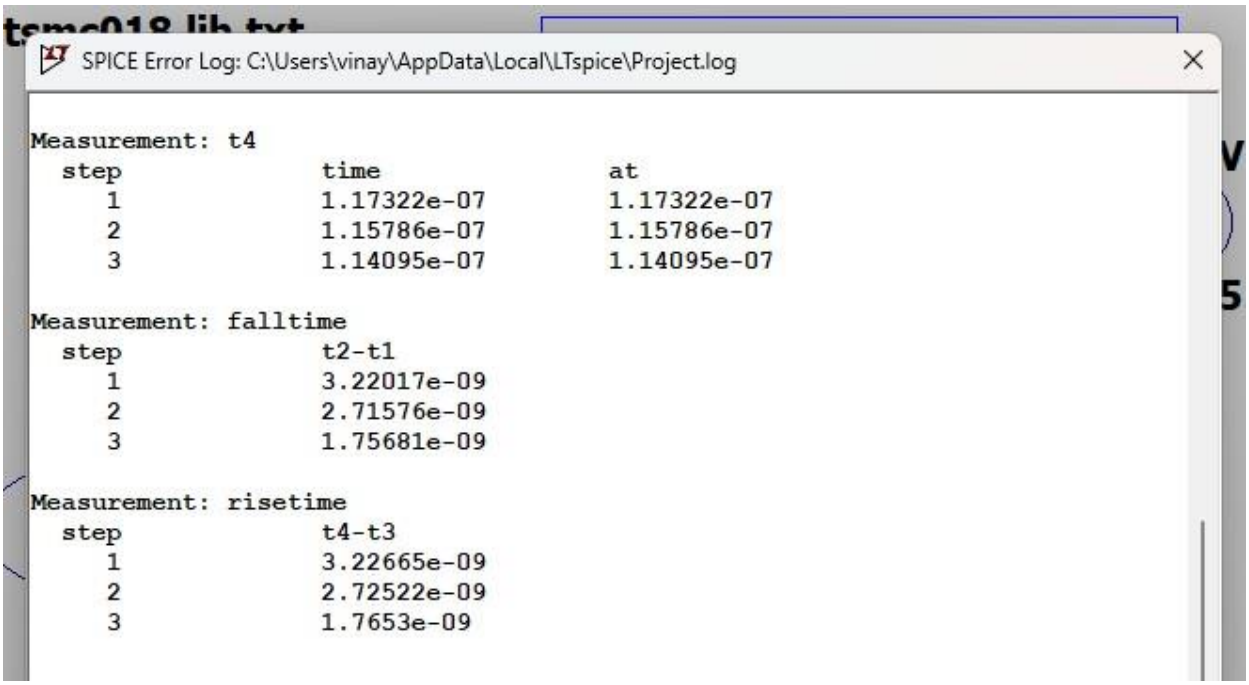


Timing Diagram:



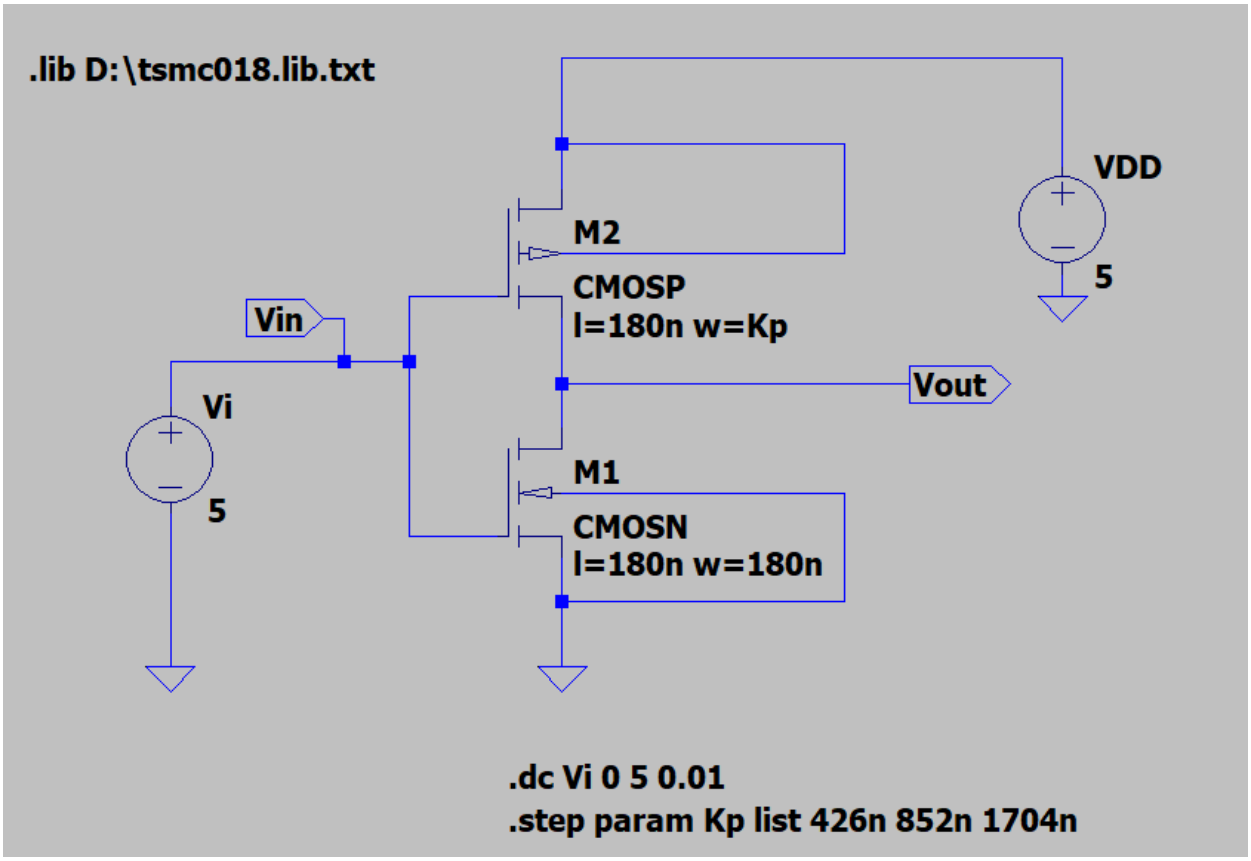
(Que) Tabulate the rise time and fall time delays obtained.

Rise & Fall Times: (For Kp=1, Kp=2, Kp=4)

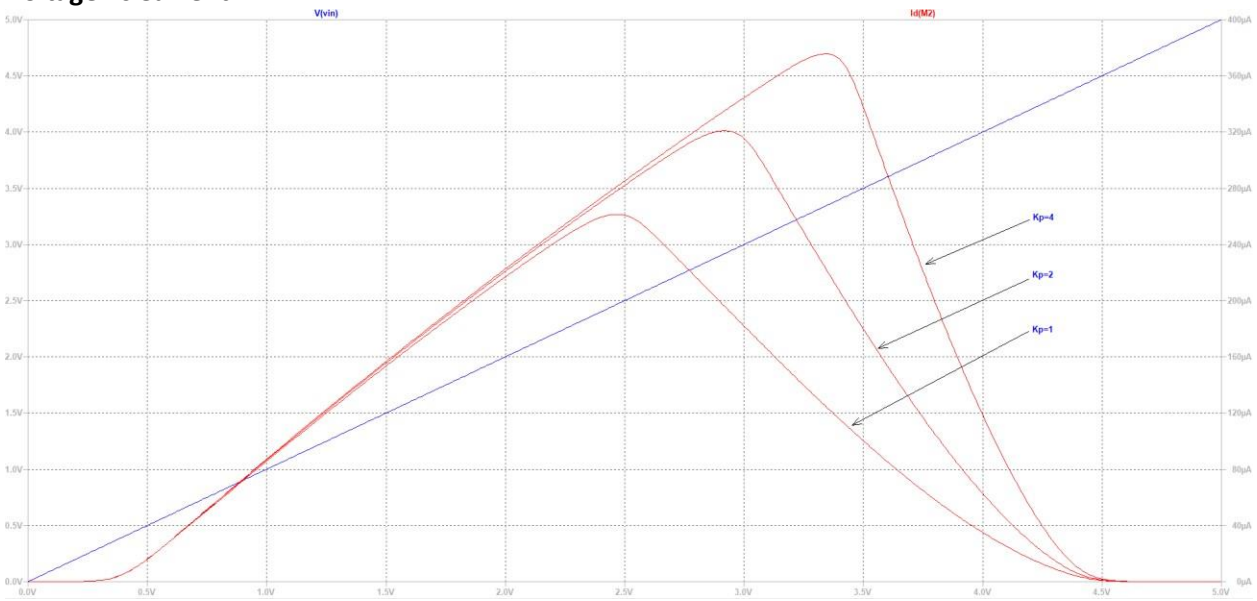


(Que) Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends.

Circuit: (Kp is varied)



Voltage Vs Current:



Static & Dynamic Power Tables:

(**Note:** Static & Dynamic powers are calculated using same process as that of question 1.b part)

Static Power:

Static Power for Kp=1, Kp=2 & Kp=4 is calculated and tabulated as follows:

Sr. No.	Kp	Power @ Vin = 0V	Power @ Vin = 5V	Static Power
1	1	2.2699nW	64.466pW	1.167nw
2	2	2.2699nW	67.019pW	1.168nW
3	4	2.2699nW	86.055pW	1.178nW

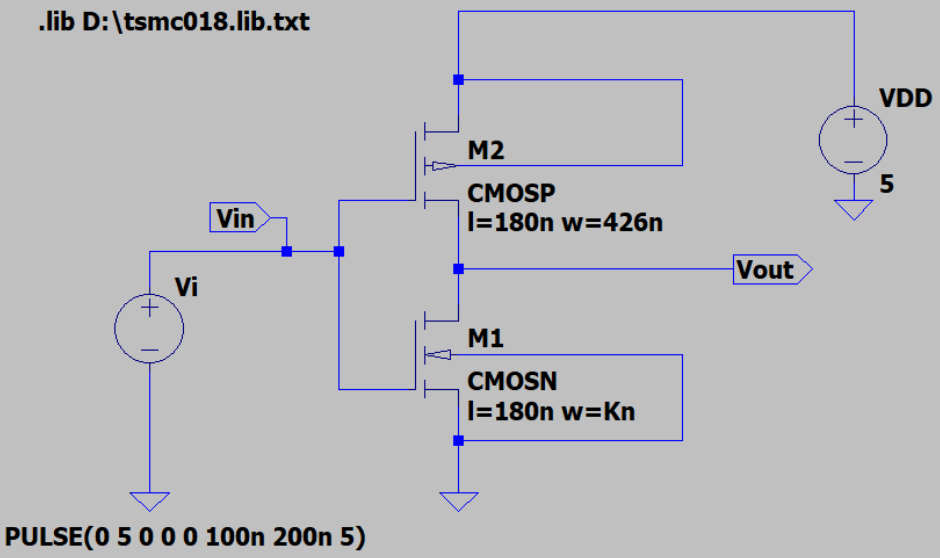
Dynamic Power:

Dynamic Power for Kp=1, Kp=2 & Kp=4 is calculated and tabulated as follows:

Sr. No.	Kp	Dynamic Power
1	1	62.748µW
2	2	78.705µW
3	4	93.802µW

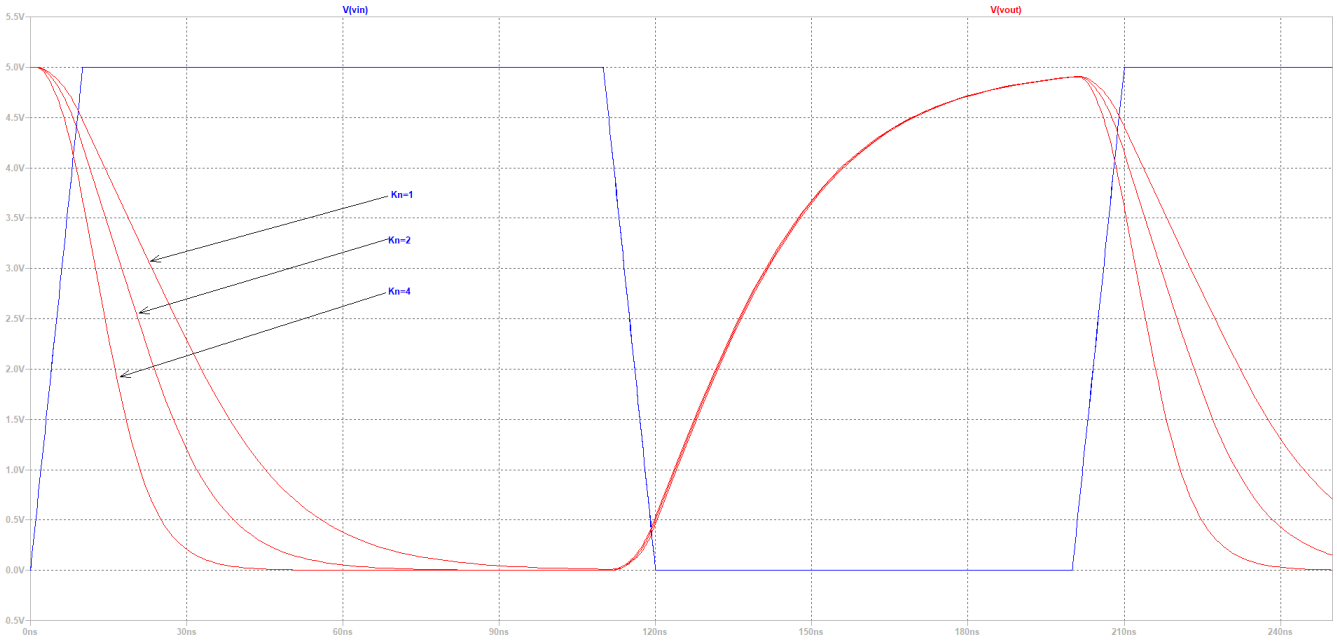
1.d.
Case (ii) 5pF external capacitor is attached

Part(i) Kn is varied
Circuit:




```
.tran 250n
.step param Kn list 180n 360n 720n

.meas t1 FIND time WHEN V(Vout) = 4.5V FALL=1
.meas t2 FIND time WHEN V(Vout) = 0.5V FALL=1
.meas t3 FIND time WHEN V(Vout) = 0.5V RISE=1
.meas t4 FIND time WHEN V(Vout) = 4.5V RISE=1
.meas falltime param t2-t1
.meas risetime param t4-t3
```

Timing Diagram:



(Que) Tabulate the rise time and fall time delays obtained.

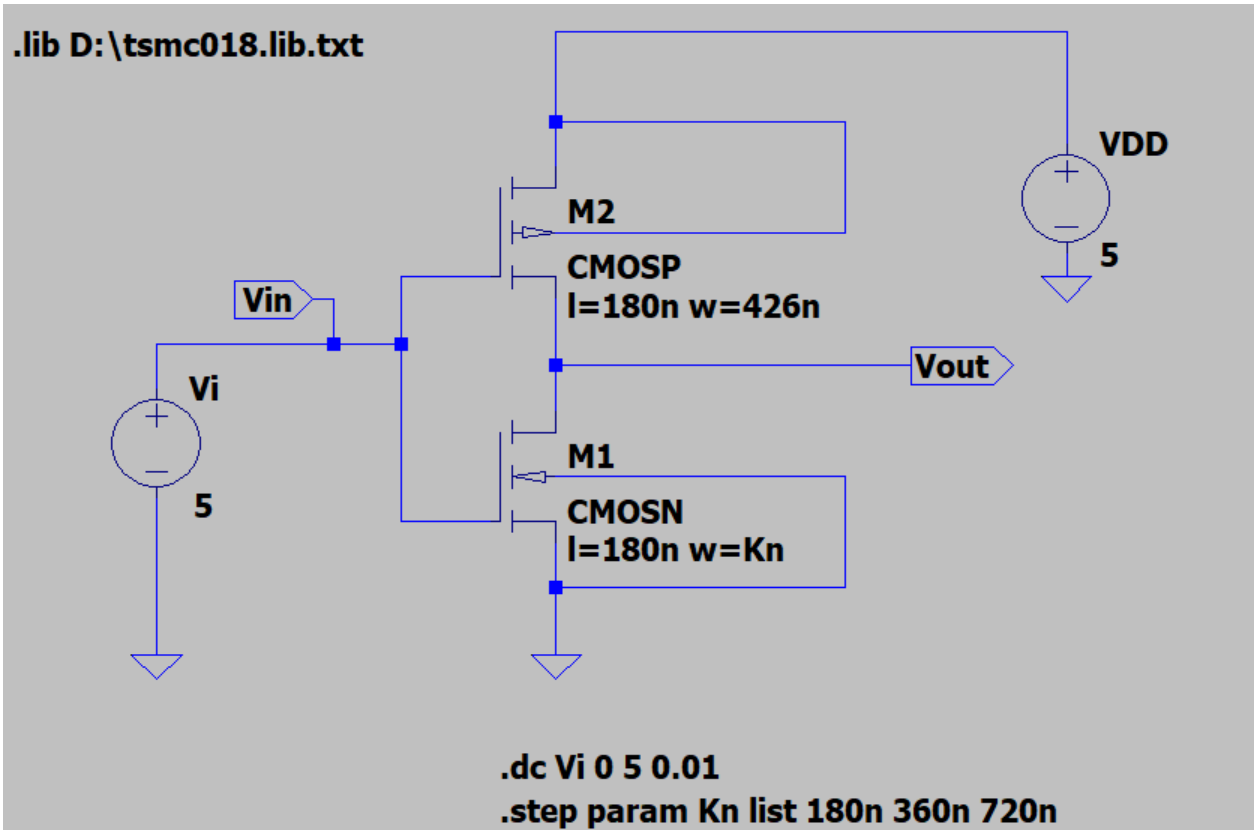
Rise & Fall Times: (For Kn=1, Kn=2, Kn=4)

SPICE Error Log: C:\Users\vinay\AppData\Local\LTspice\Project.log

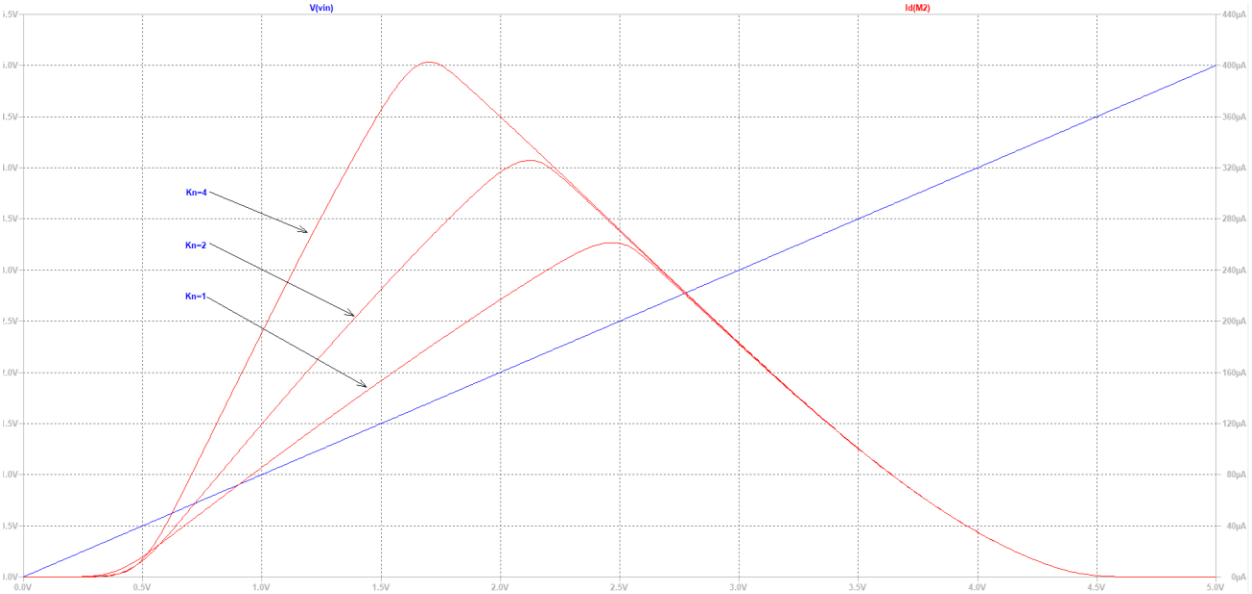
```
  step             time                at
     1             1.69217e-07         1.69217e-07
     2             1.69421e-07         1.69421e-07
     3             1.69711e-07         1.69711e-07

Measurement: falltime
  step             t2-t1
     1             4.60702e-08
     2             3.08452e-08
     3             1.87046e-08

Measurement: risetime
  step             t4-t3
     1             4.94349e-08
     2             4.94319e-08
     3             4.94336e-08
```

(Que) Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends.

Circuit: (Kn is varied)



Voltage Vs Current:



Static & Dynamic Power Tables:

(**Note:** Static & Dynamic powers are calculated using same process as that of question 1.b part)

Static Power:

Static Power for Kn=1, Kn=2 & Kn=4 is calculated and tabulated as follows:

Sr. No.	Kn	Power @ Vin = 0V	Power @ Vin = 5V	Static Power
1	1	2.2699nW	64.466pW	1.167nW
2	2	561.35pW	64.466pW	0.312nW
3	4	381.32pW	64.466pW	0.223nW

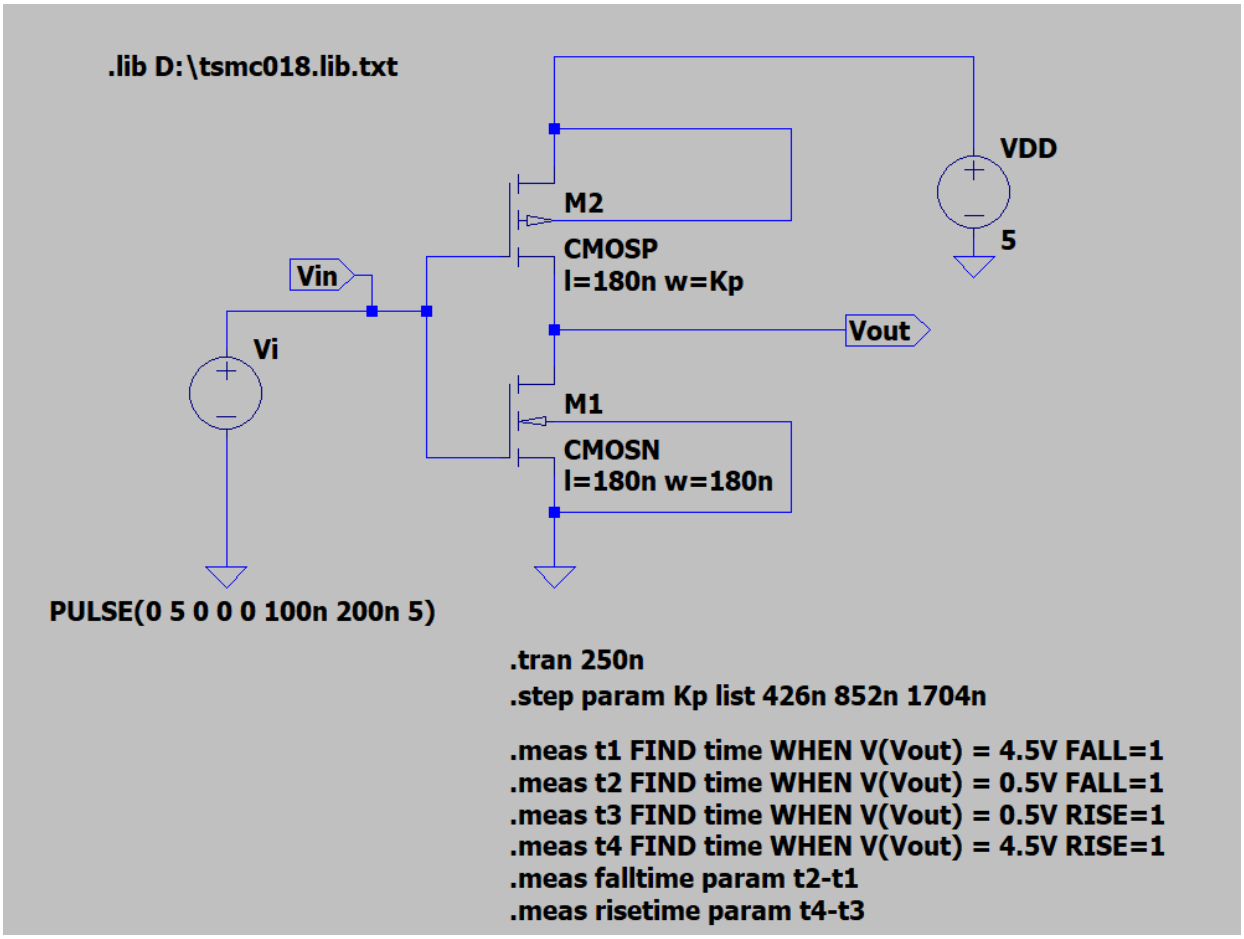
Dynamic Power:

Dynamic Power for Kn=1, Kn=2 & Kn=4 is calculated and tabulated as follows:

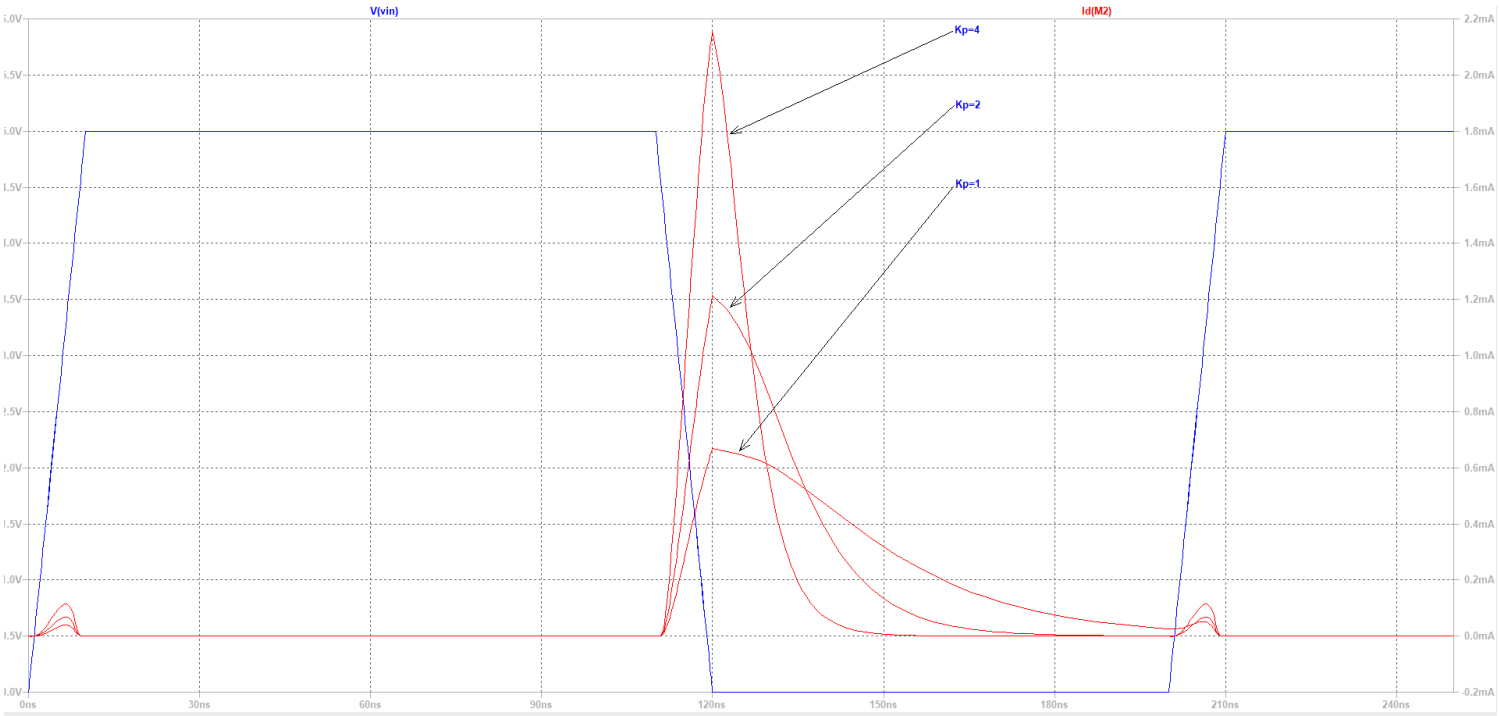
Sr. No.	Kn	Dynamic Power
1	1	504.05µW
2	2	509.07µW
3	4	516.98µW

Part(i) Kp is varied

Circuit:



Timing Diagram:



(Que) Tabulate the rise time and fall time delays obtained.

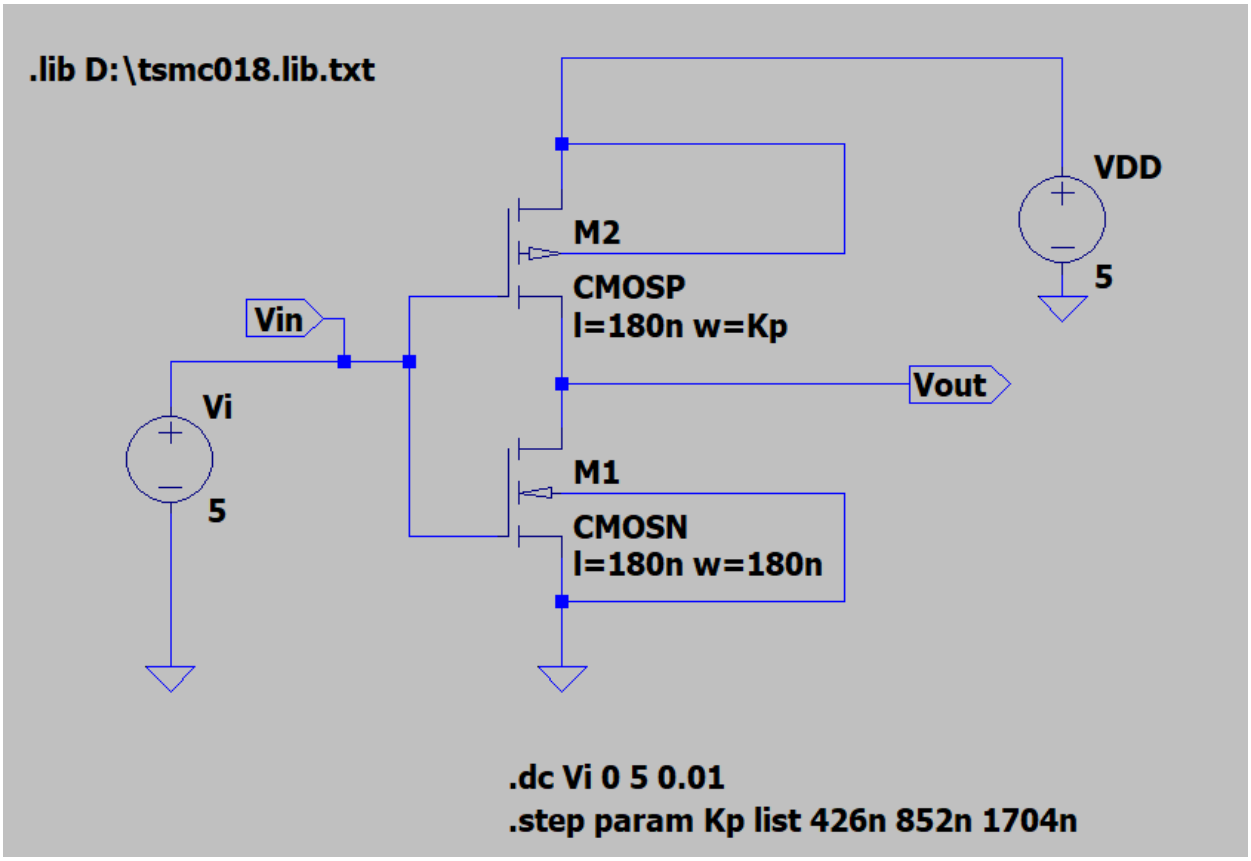
Rise & Fall Times: (For Kp=1, Kp=2, Kp=4)

SPICE Error Log: C:\Users\vinay\AppData\Local\LTspice\Project.log

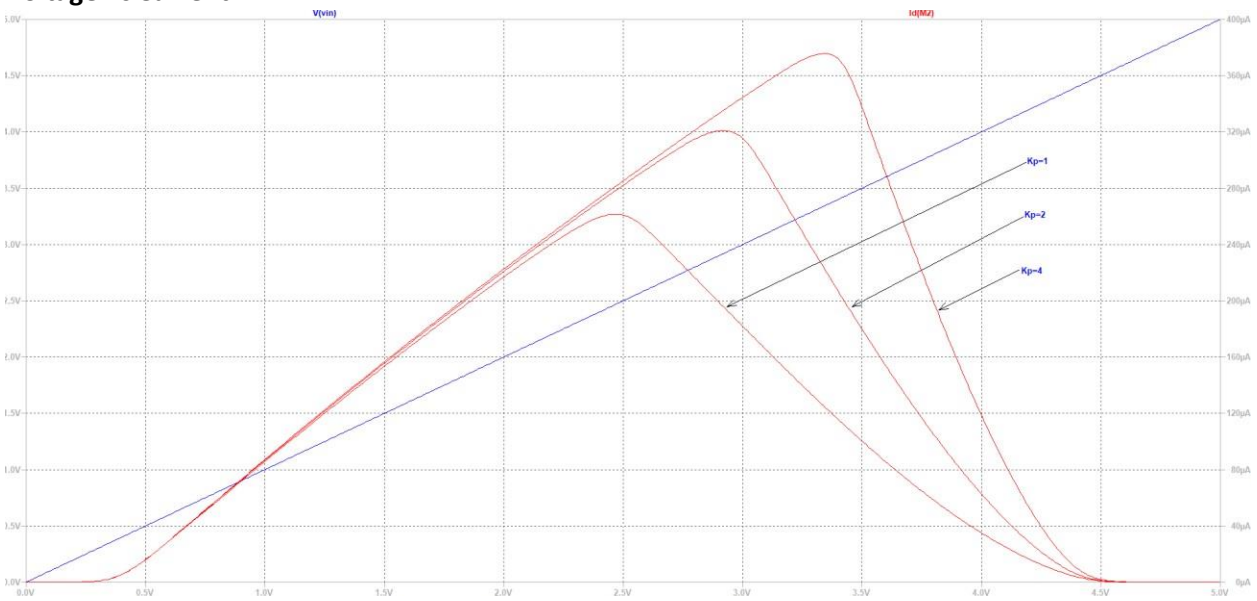
```
Measurement: t4
  step             time             at
     1             1.69217e-07      1.69217e-07
     2             1.43392e-07      1.43392e-07
     3             1.30162e-07      1.30162e-07

Measurement: falltime
  step             t2-t1
     1             4.60702e-08
     2             4.60692e-08
     3             4.60708e-08

Measurement: risetime
  step             t4-t3
     1             4.94349e-08
     2             2.55754e-08
     3             1.4014e-08
```

(Que) Find out the current drawn from the power supply in all cases as the input voltage is swept slowly w.r.t the output, and plot the current vs input voltage in a single graph with clear legends.

Circuit: (Kp is varied)



Voltage Vs Current:



Static & Dynamic Power Tables:

(**Note:** Static & Dynamic powers are calculated using same process as that of question 1.b part)

Static Power:

Static Power for Kp=1, Kp=2 & Kp=4 is calculated and tabulated as follows:

Sr. No.	Kp	Power @ Vin = 0V	Power @ Vin = 5V	Static Power
1	1	2.2699nW	64.466pW	1.167nW
2	2	2.2699nW	67.019pW	1.168nW
3	4	2.2699nW	86.055pW	1.178nW

Dynamic Power:

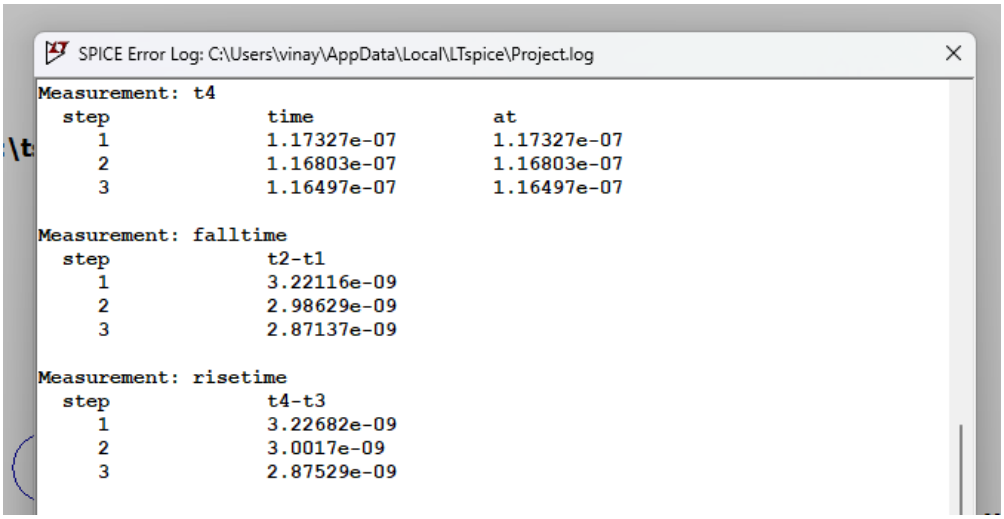
Dynamic Power for Kp=1, Kp=2 & Kp=4 is calculated and tabulated as follows:

Sr. No.	Kp	Dynamic Power
1	1	504.05µW
2	2	518.34µW
3	4	530.16µW

1.e.

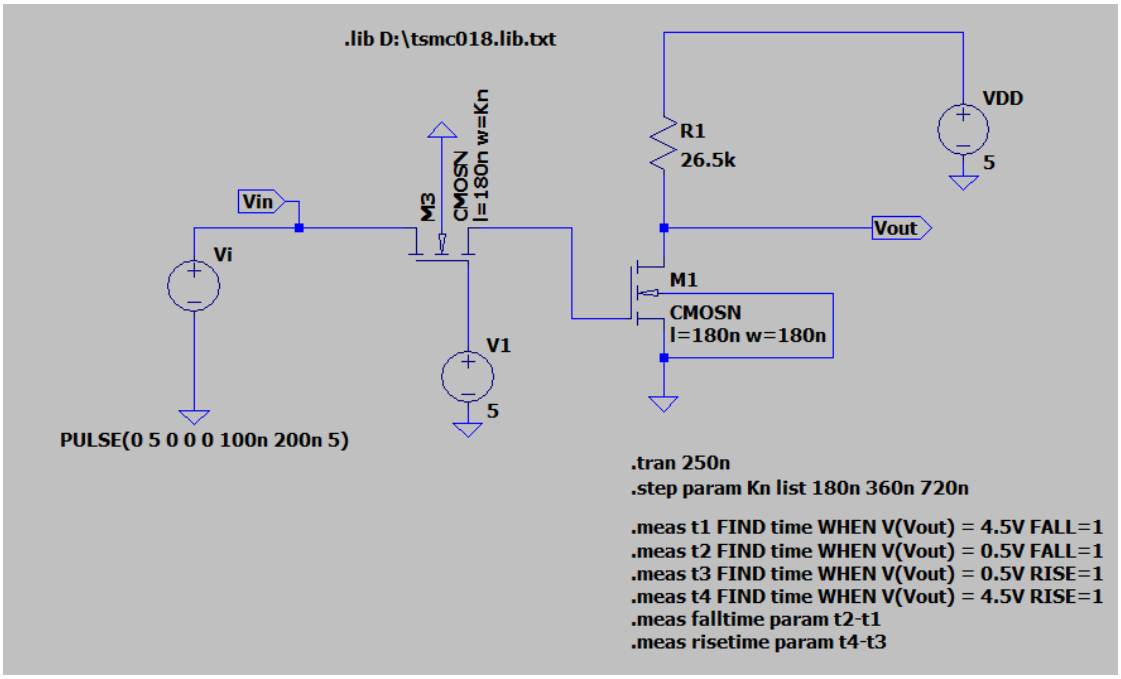
Create a circuit consisting of a NMOS pass transistor having size Kn=1,2,4, driving an NMOS inverter of minimum size connected to the source/drain of the NMOS pass transistor (choose the resistor value in the NMOS inverter to have equal rise and fall times which also should be equal to that of a minimum-sized symmetrical CMOS inverter).

From result 1.b. - Rise & Fall Delays for minimum sized CMOS inverter: (3.22nsec for S=1)



(Note: Delays are listed in order S=1, S=2 & S=4)

Now creating NMOS inverter with pass transistor for which rise & fall delays are matched with CMOS inverter:



Circuit:

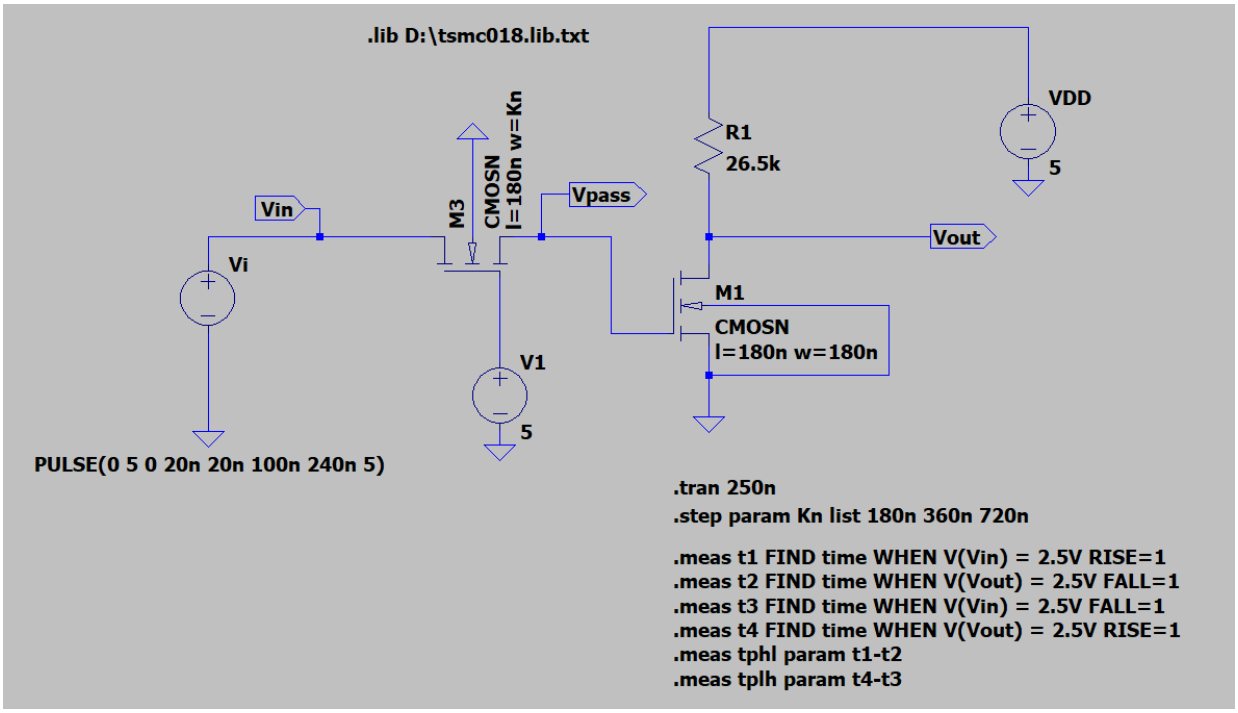
Rise & Fall Delays-

SPICE Error Log: C:\Users\vinay\AppData\Local\LTspice\Eproject.log

```
Measurement: t4
  step             time                at
     1             1.18955e-07         1.18955e-07
     2             1.18954e-07         1.18954e-07
     3             1.18954e-07         1.18954e-07

Measurement: falltime
  step             t2-t1
     1             3.18833e-09
     2             3.18848e-09
     3             3.18862e-09

Measurement: risetime
  step             t4-t3
     1             3.2106e-09
     2             3.21001e-09
     3             3.20956e-09
```

(Que) Apply an input signal to the source/drain of the NMOS pass transistor of which the gate is connected to VDD, and plot the voltage waveform at the input and output of the inverter and tabulate the delay at both the input and output of the inverter for all values of Kn, when the input signal varies slowly from (i) low to high, (ii) high to low.

Circuit:

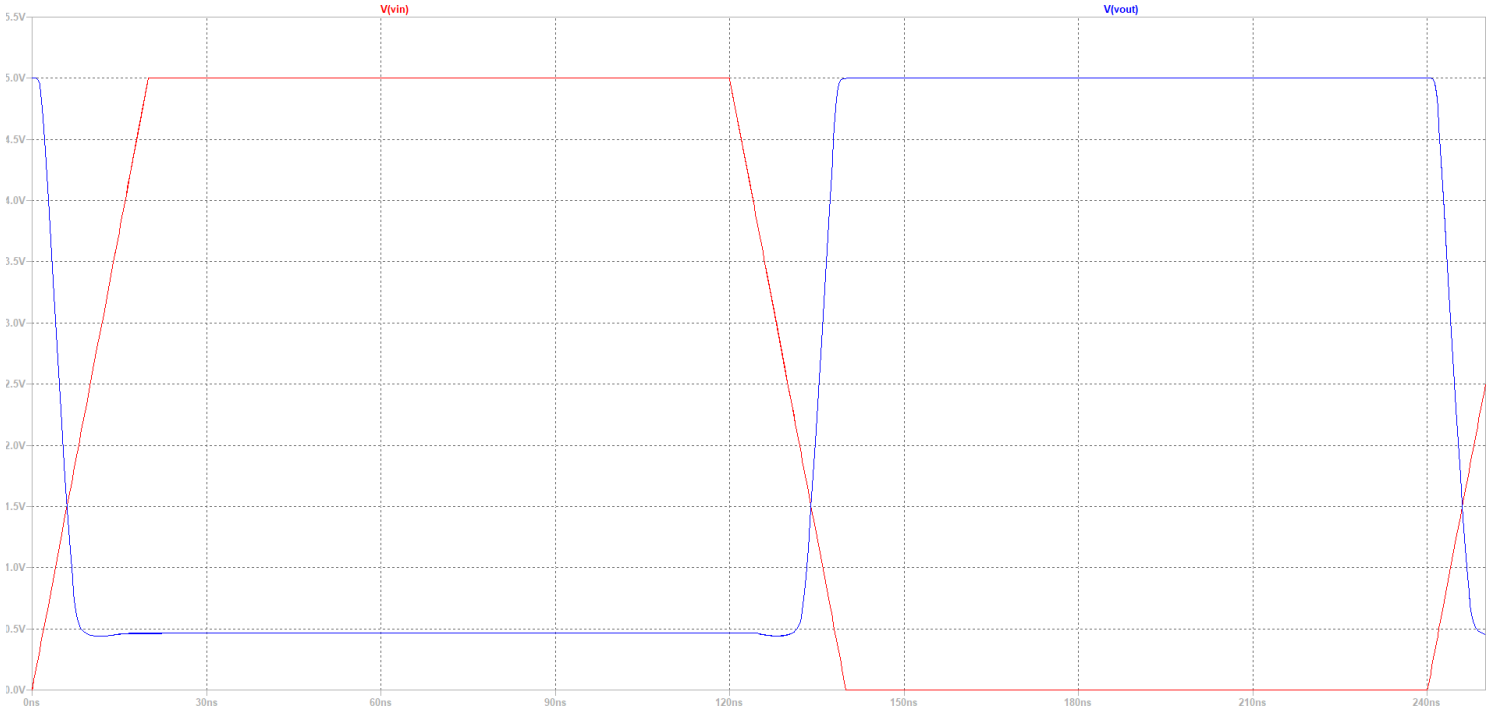


Propagation Delays (From Vin to Vout):

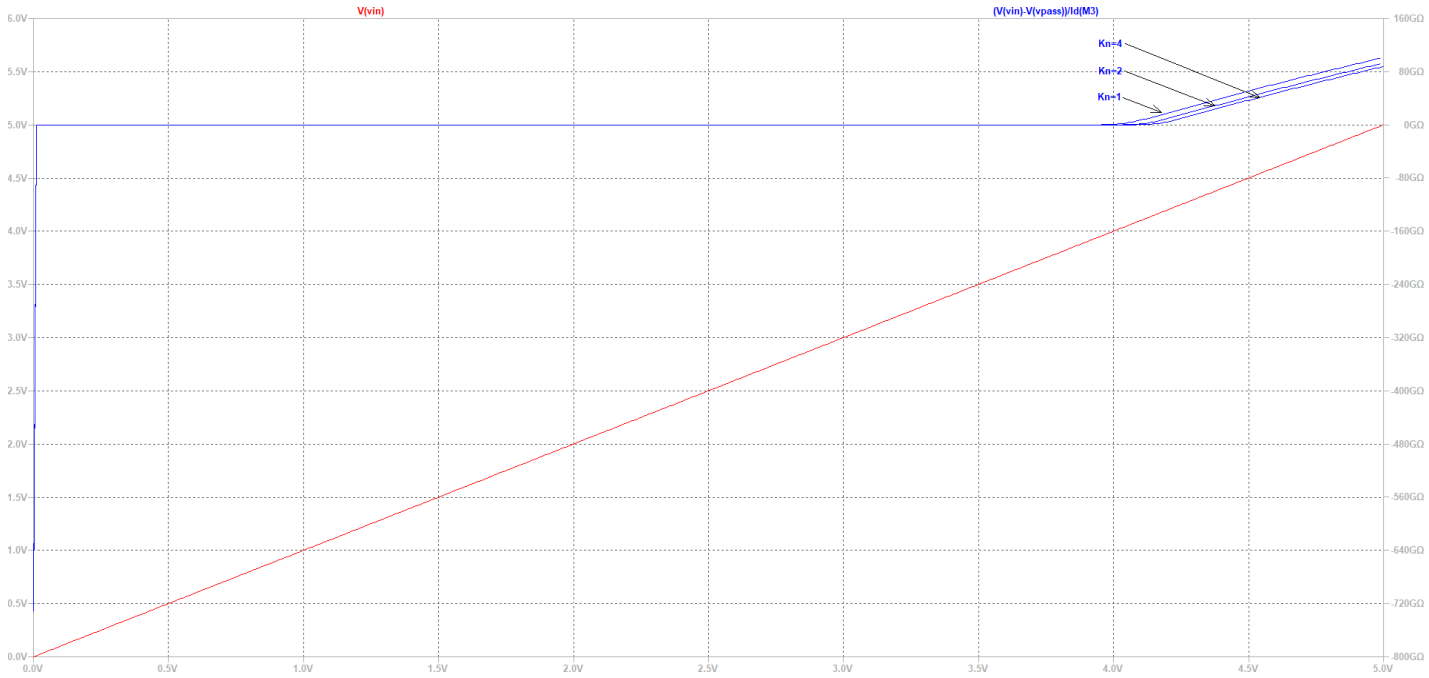
SPICE Error Log: C:\Users\vinay\AppData\Local\LTspice\Eproject.log

```
Measurement: tphl
  step              t1-t2
     1              5.32241e-09
     2              5.32304e-09
     3              5.32353e-09

Measurement: tplh
  step              t4-t3
     1              5.33575e-09
     2              5.33512e-09
     3              5.33462e-09
```

Timing Diagram:



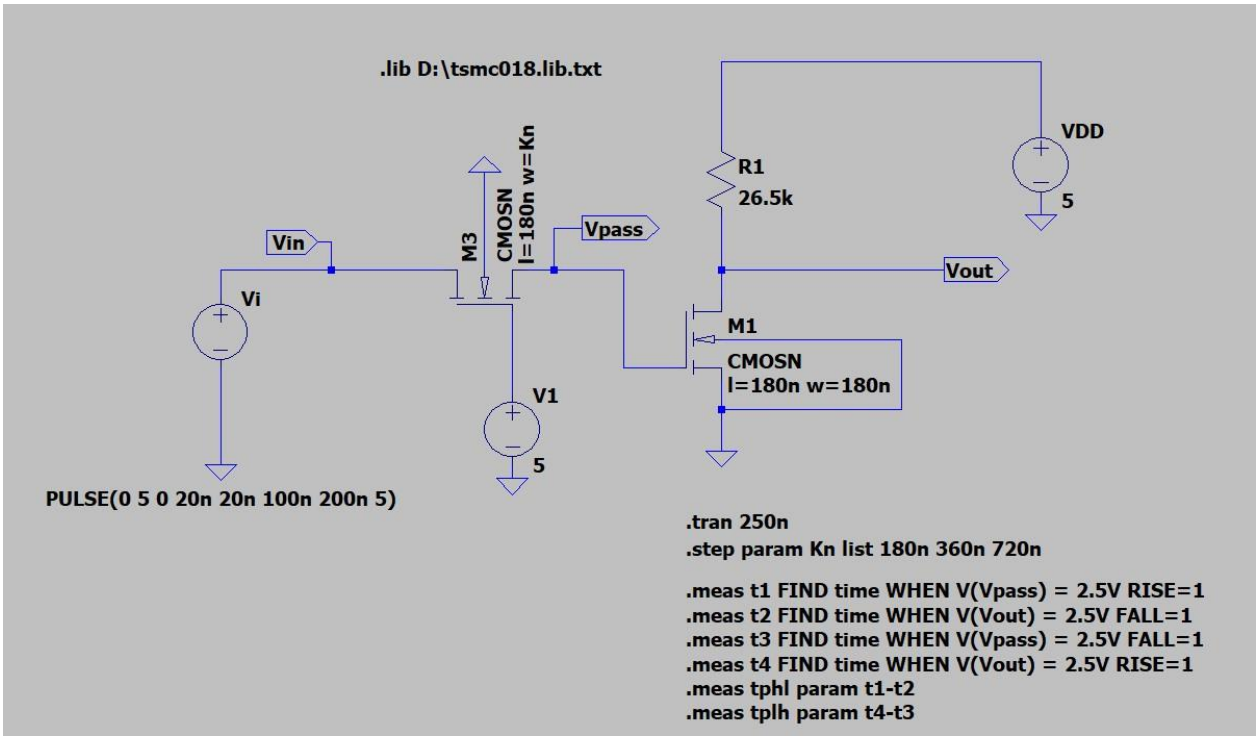
(Que) Plot the resistance of the pass transistor vs input voltage in a single graph with clearly labelled axes and legends for all values of Kn.



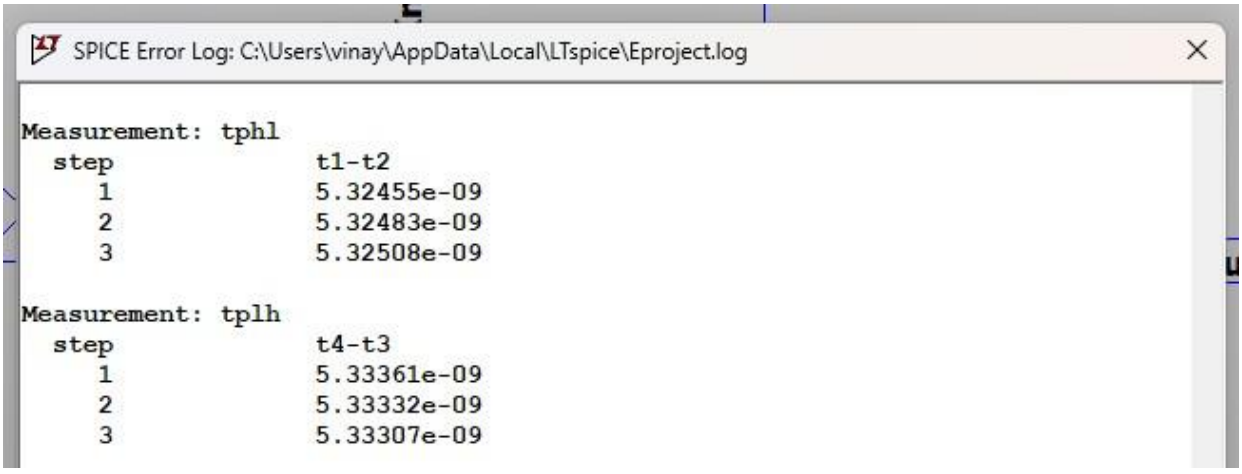
Observation: For increasing value of Kn, the resistance is decreasing.

(Que) Do another simulation to plot the voltage waveform at the input and output of the inverter and tabulate the delay at both the input and output of the inverter for all values of Kn, when the source/drain of the NMOS pass transistor is connected to VDD and the input signal which is applied to the gate of the NMOS pass transistor varies slowly from (i) low to high, (ii) high to low.

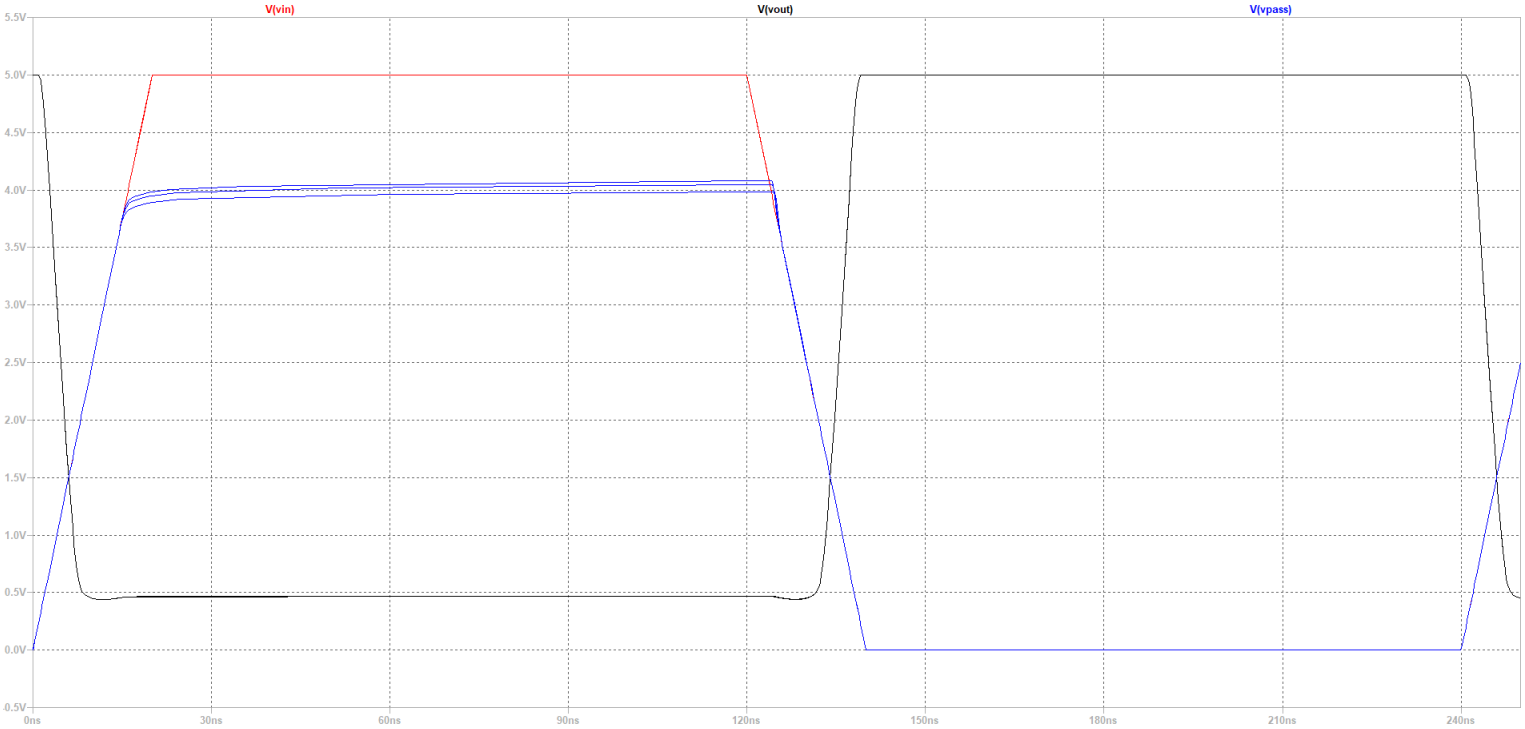
Circuit:



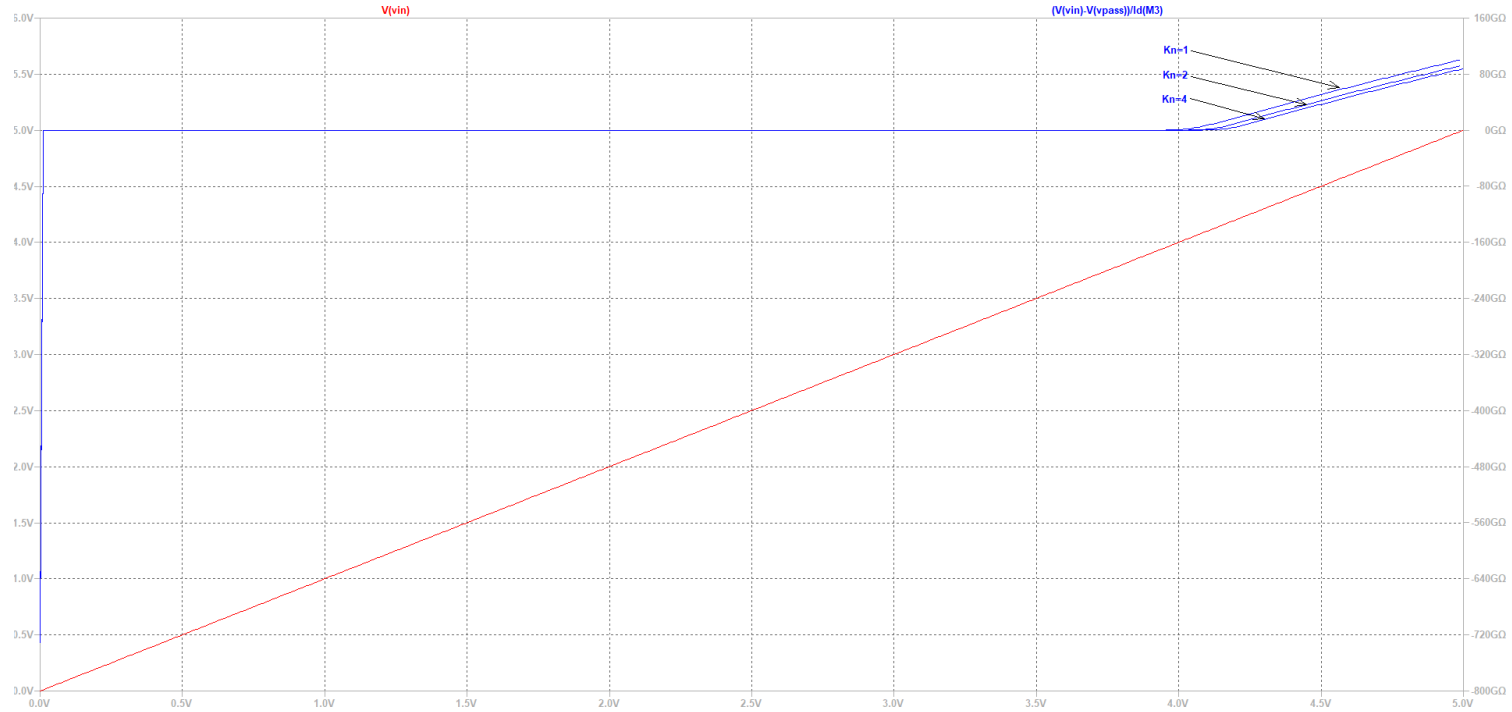
Propagation Delays (From Vpass to Vout):



Timing Diagram:



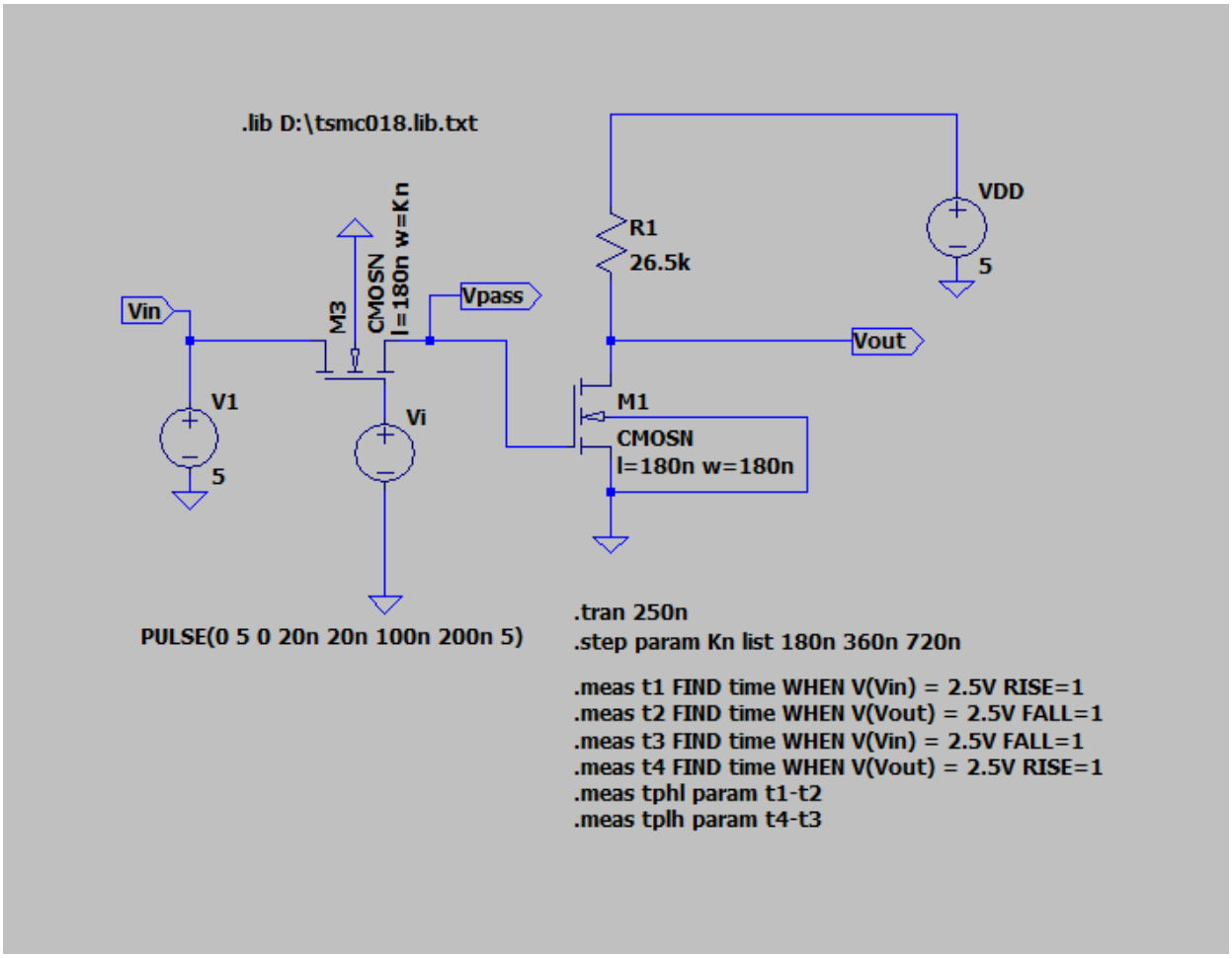
(Que) Plot the resistance of the pass transistor vs input voltage in a single graph with clearly labelled axes and legends for all values of Kn.



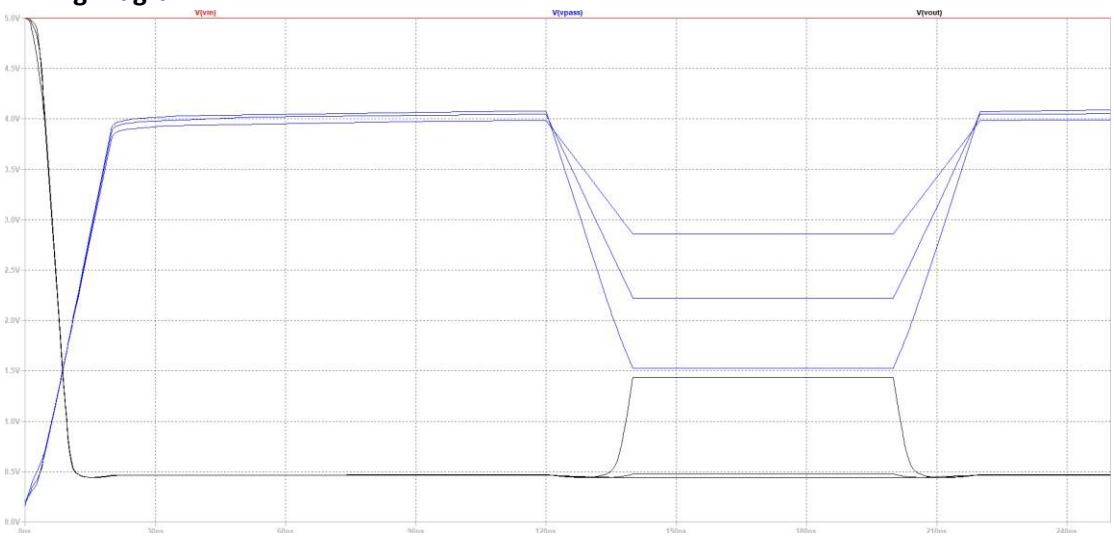
Observation: For increasing value of Kn, the resistance is decreasing.

If drain/source is connected to Vdd & input is connected to gate:

Circuit:



Timing Diagram:



Delays:

(Note: The pass transistor Source voltage does not reach to Vdd so delay calculation gives error)

SPICE Error Log: C:\Users\vinay\AppData\Local\LTspice\Eproject.log

```
Circuit: * C:\Users\vinay\AppData\Local\LTspice\Eproject.asc

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.
.step kn=1.8e-07
.step kn=3.6e-07
.step kn=7.2e-07


Measurement "t1" FAIL'ed

Measurement: t2
  step             time               at
     1             6.96049e-09        6.96049e-09
     2             7.01528e-09        7.01528e-09
     3             7.00107e-09        7.00107e-09

Measurement "t3" FAIL'ed

Measurement "t4" FAIL'ed

Measurement "tphl" FAIL'ed

Measurement "tplh" FAIL'ed
```

Resistance plots:

(Note: As Kn value increases, the resistance value drops.)