Project: Annual Handoff flow process at BlackChip Semiconductors (BCS)

Company Background:

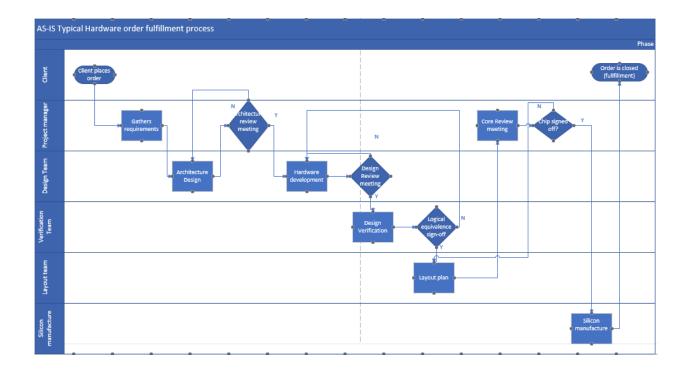
Blackchip is an upcoming semiconductor start-up specialized in developing low-cost hardware solutions for clients that are involved in Non-Profit activities. A typical project at BlackChip semiconductor starts with client placing a order and goes through several stages like sales, management, design, verification, layout planning, silicon manufacturing.

Process and Actors:

Once the client places an order, the sales inventory gets updated and a program manager gathers requirements to communicate to the designated Design Team. There are frequent architecture review meetings that are held until architecture is finalized. Once the architecture is finalized then the sales team performs projected cost benefit analysis and parallely Design development begins. For each design cycle, the verification team works on finding bugs within the design. If any breaks are found, then design is handed off to the design team to fix the issues. Once sign-off is clean, the layout engineer places the entire design on layout (A 3D platform) to simulate the actual chip before manufacturing. Once the layout process is finished, A core review meeting is held to take care of any last-minute hiccups before proceeding to silicon manufacturing.Once silicon manufacturing completes, the sales team performs actual cost benefit analysis and the order is fulfilled to the customer.

- Client Each client places orders based on their requirements. They can make multiple orders.
- Sales They handle the inventory updates. They also work on Actual and Projected cost benefit analysis, profit or loss estimation during the entire project life cycle.
- Project manager (Management) They receive the order and deliver the requirements to the appropriate design teams. They also conduct the review meetings across the teams. They are also part of signing-off of the project before delivering the order to silicon manufacturer
- Design & verification Team They design the chips, involve in hardware development and after the designing, they conduct various verifications on those chips.
- Layout team They perform chip planning on the designed and verified chips based.
- Silicon manufacture Post Layouting, silicon manufacturer manufactures the chips based on the order count.

Swimlane Diagram: AS-IS:



Issues with Current Process:

The current process has some minor issues.

- 1) The communication between the Design and Verification team. There is no necessity of frequent design meetings if the verification stage is failed. For example, if a chip "A" has met all goals of power, performance and area and signed off by the design team and if the verification team found bugs then entire design resources are wasted. So, it's not ideal for the verification team to wait until design review meetings take place. It's best to have a strategy.
- 2) Once the layout planning is done, there are no meetings happening internally within the team. These meetings are necessary for any team before the final core review meeting to make sure that everything is perfect.

Solution:

BCS has come up with the solutions for those two problems.

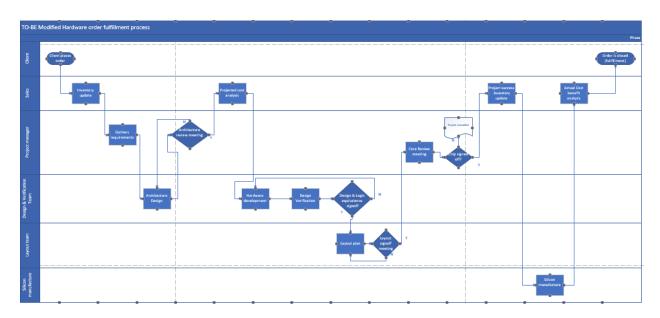
- \rightarrow For the first problem, combining the design and verification teams will resolve the dependencies among the two teams. Because they are interrelated, it's best practice to put them under the same actor.
- → As far as the second problem is concerned, BCS planned to add a layout signoff meeting before the final core-review meeting. This might add some delay in the process, but it's necessary to have this meeting, because this makes the process more efficient before handing chips to the client.

Enablers:

The changes suggested above contribute to modifying Workflow Design and Information systems.

- [Workflow Design] Added sales as a new actor and additional process restructuring in Layout, Design and Verification for making the process more streamlined.
- [Information systems] Addition of actor "Sales" would create additional data which can be used to cost benefit analysis..

Swimlane Diagram: TO-BE:

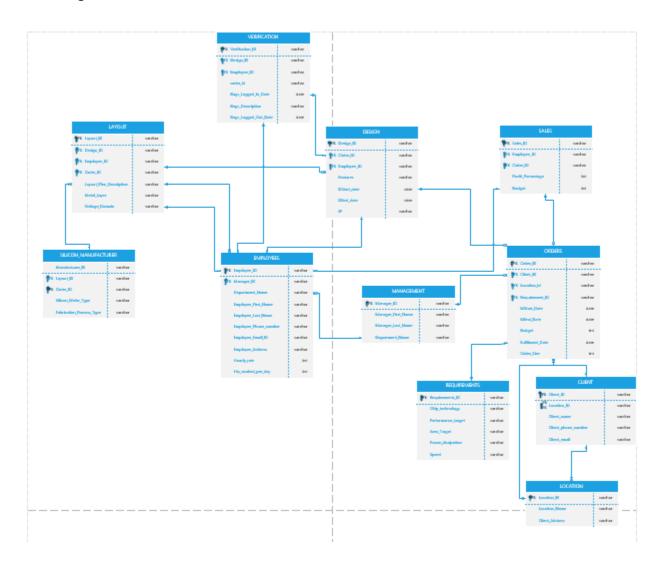


Detailed Description of the Business Rules and User Requirements:

- One order is placed by one and only one client, one client can place on or more orders.
- One client will be associated with one or more locations. Each location is associated with one client.
- One order will have one and only one requirement. Requirements will be for one or more orders.
- One order will be assigned to one and only one manager, Each manager may or maynot handle an order.
- One order will be assigned to one sales team, each sales team may or maynot handle an order
- Each order will be assigned to one and only one design team, design teams will work on zero or more orders.
- Each Design will be verified only once, verification is done on one or more designs.

- Each verified design will have one and only layout, multiple designs can have many layouts.
- Each layout-design is manufactured by one silicon manufacturer. Each silicon manufacturer can manufacture many layout-designs.
- Each team like sales, management, design, verification, layout have one or more employees. Each employee belongs to one and only one department team.

ERD Diagram:



Entity Description:

- 1. Client: Each client places an order. Each client is established in 1 or more locations. This entity contains the client's id, name, phone number, email id and location's id. Here client id and location id are the composite primary key. Location Id is the foreigh key.
- **2. Locations:** The entity locations have unique locations in which clients are present. This entity contains Location's ID, name and address. Here Location_id is the primary key.
- **3. Orders:** This entity gives information about the orders placed such as the id of the client who placed the order, the client's location, the requirement's id through which we can get the requirements of the order, order start date, order end date, order fulfillment date, order size and the budget assigned to this order.
- **4. Requirements:** This entity gives information about the requirements such as the chip technology to be used, target performance, target area, power dissipation and speed.
- **5. Employees:** This entity contains information of all employees such as their first name ,last name, phone number, email id, address, hourly rate, number of hours worked per day, department they belong to, and their manager' id.
- **6. Management:** This entity contains the id, first name, last name and department of the manager.
- **7. Design:** This entity gives design features, design start date, design end date, it's ip status for each order placed by the client.
- **8. Verification:** This entity gives description of the bugs detected along with the bugs log-in and log_out date for each design.
- **9.** Layout: This entity contains information about the layout's plan, metal layer and voltage domain for each design.
- **10. Silicon manufacturer:** This entity describes the materials and methodology type used for the manufacturing of chips
- **11. Sales:** This entity contains the budget and its respective profit percentage for each order along with the sales employees working for each order.

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Database	Attribute	Data type		Key type	Accepts null value	
	Client ID	VARCHAR		Primary key	N	Unique IDs for all the clients
	Location ID	VARCHAR	10	Primary key, Foreign Key	N	Unique IDs for all the locations
Clients	Client Name	VARCHAR	30		Υ	Full name of client
	Client phone number	VARCHAR	40		Υ	Phone number of client
	Client email	VARCHAR	50		Υ	Email of client
	Location ID	VARCHAR	10	Primary key	N	Unique IDs for all locations
Locations	Location Name	VARCHAR	30		Υ	Locations where client is established
Locations	Client Address	VARCHAR	255		Y	Location address where client is established
	Cilcit Address	VAICHAI	255			Eocation address where client is established
	0-410	WARCHAR	10	Data and Land		United the forest the control
	Order ID	VARCHAR		Primary key	N	Unique IDs for all the orders
	Client ID	VARCHAR		Foreign key	Υ	Unique IDs for all the clients
	Location ID	VARCHAR		Foreign key	Υ	Unique IDs for all the clients
	Requirement ID	VARCHAR	10	Foreign key	Υ	Unique IDs for all requirements imposed by customers
Orders	MStart date	DATE			N	Start date of the project
	MEnd date	DATE			N	End date of the project
	Budget	integer	20		N	Budget for the chip
	Fullfillment date	DATE			N	Due date for the chip completion
	Order size	integer	10		N	Number of chips required
	Requirements ID	VARCHAR	10	Primary key	N	Unique IDs for all requirements imposed by customers
Requirements	Chip technology	VARCHAR	15		Y	Chip technology is a number that specifies size of technology typically in nano meter
		VARCHAR	10		Y	Performance target is set per 100% to convey efficiency
	Performance target				*	
	Area target	VARCHAR	10		Y	Area target is a number in nn/mm size of chip
	Power dissipation	VARCHAR	10		Y	Power dissipation is an integer typically in milli watts
	Speed	VARCHAR	10		Υ	Describes the performance rate of the chip typically in GHz/ns
	Employee ID	VARCHAR		Primary key	N	Unique ID to identify all members of company
Employees	Manager_ID	VARCHAR	30	Foreign key	Υ	Unique ID to identify all members of company
	Department name	varChar	30		Υ	department ID to know which team he belongs
	Employee first name	varChar	30		N	Name of employee
	Employee Last name	varChar	50		N	Last name of employee
	Employee phone number	varChar	40		N	Phone number of employee
	Employee email ID	varChar	255		N	Email ID of employee
	Employee Address		255		Y	Address of employee
		varChar			N	
	Hourly rate	Integer	10			Hourly rate of the employee
	HRS_WORKED_PER_DAY	INTEGER	10		N	
	Manager_ID	VARCHAR	10	Primary key	N	Unique ID for a manager
					N Y	
Management	Manager first name	VARCHAR	40		Υ	first name of employee
Management	Manager first name Manager last name	VARCHAR VARCHAR	40 40		Y Y	first name of employee Last name of employee
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Design Verification	Manager first name Manager last name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Dusgs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Layout_plan description	VARCHAR	100 400 400 400 400 400 400 400 400 400	Primary key Foreign Key Foreign Key Foreign Key Primary key Foreign Key	Y Y N N N Y Y Y N N Y Y Y N N Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for all the orders Unique ID for all the orders Unique IDs for the designs Register to track the bugs that are found in design Register to track the bugs that are found in design Unique IDs for the designs Register to track closing dates of bugs that are found in design Unique IDs for the designs Register to track are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique ID for all the orders Unique ID for layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation
Design Verification	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Layout_ID Layout_ID Layout_ID Layout_ID and description Metal layer Voltage domain	VARCHAR	100 100 100 100 100 100 100 100 100 100	Primary key Foreign Key Foreign Key Primary key Foreign Key	Y Y N N N Y Y Y N N N Y Y N N N Y Y Y Y	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for all the orders Unique ID for all the orders Unique IDs for the designs Register to track the bugs that are found in design Register to track the bugs that are found in design Unique IDs for the designs Register to track closing dates of bugs that are found in design Unique IDs for the designs Register to track are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique ID for all the orders Unique ID for layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation
Design Verification	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Design_ID Design_ID Layout_ID Layout_ID Layout_ID Layout_ID Layout_ID Design_ID Design_ID Design_ID Layout_ID Layout_ID Layout_ID Design_ID Design_ID Layout_ID Layout_ID Layout_ID Layout_ID Layout_ID Design_ID Design_ID Design_ID Design_ID Layout_ID Resployee ID ORDER_ID Design_ID Design_ID Design_ID Layout_ID Resployee ID ORDER_ID Design_ID Design_ID Layout_ID Resployee ID ORDER_ID Design_ID Design_ID Layout_ID Resployee ID ORDER_ID Design_ID Design	VARCHAR	100 100 100 100 100 100 100 100 100 100	Primary key Foreign Key Foreign Key Primary key Primary key Foreign Key	Y Y N N N Y Y Y N N N Y Y Y N N Y Y Y Y	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for all the orders Unique ID for all the orders Unique IDs for all the orders Unique IDs for blues that are found in design Register to track the bugs that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique IDs for the layouts Unique ID for all the orders Unique IDs for all the orders Unique ID for layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation
Design Verification Layout	Manager first name Manager last name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Dusign_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout plan description Metal layer Voltage domain	VARCHAR	100 400 400 400 400 400 400 400 400 400	Primary key Foreign Key Foreign Key Primary key Foreign Key	Y Y Y N N N Y Y Y N N N Y Y N N N Y Y Y N N Y Y Y N N N Y Y Y N N N Y Y N N N Y Y N N N Y Y N N N N Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y N N N Y Y N N N N Y Y Y N N N N Y Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design IP status of the design Unique ID for a verification Unique ID for an employee working on verification Unique ID for an employee working on verification Unique IDs for all the orders Unique IDs for the designs Register to track the bugs that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique IDs for all the orders Unique IDs for the layouts Unique ID of employees working on identifying bugs Unique ID of layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation
Design Verification	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Employee ID ORDER_ID Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Order_ID	VARCHAR	100 100 100 100 100 100 100 100 100 100	Primary key Foreign Key Foreign Key Foreign Key Primary key Foreign Key	Y Y N N N Y Y Y Y N N N N Y Y Y Y N N N Y Y Y Y N N N N Y Y Y N N N N N N Y Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for a design Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for an employee working on verification Unique ID for all the orders Unique IDs for all the orders Unique IDs for the designs Register to track the bugs that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique ID for all the orders Unique ID for layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation
Design Verification Layout	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Layout_ID Layout_plan description Metal layer Voltage domain Manufacturer ID Layout_ID Layout_ID Layout_ID Order ID Order ID Silicon wafer type	VARCHAR	100 400 400 400 400 400 400 400 400 400	Primary key Foreign Key Foreign Key Primary key Foreign Key	Y Y N N N Y Y Y N N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N N Y Y Y N N Y Y Y N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y N N N Y Y N N N N Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design IP status of the design IP status of the design Unique ID for a verification Unique ID for a employee working on verification Unique ID for all the orders Unique ID for all the orders Unique IDs for all the orders Unique IDs for bugs that are found in design Description of bugs that are identified Register to track the bugs that are found in design Unique IDs for the design that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for all the orders Unique ID of employees working on identifying bugs Unique ID of or playout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation Unique ID for a layout Unique ID for a layout Unique ID for a layout
Design Verification Layout	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Employee ID ORDER_ID Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Order_ID	VARCHAR	100 100 100 100 100 100 100 100 100 100	Primary key Foreign Key Foreign Key Primary key Foreign Key	Y Y N N N Y Y Y Y N N N N Y Y Y Y N N N Y Y Y Y N N N N Y Y Y N N N N N N Y Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for a design Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for an employee working on verification Unique ID for all the orders Unique IDs for all the orders Unique IDs for the designs Register to track the bugs that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique ID for all the orders Unique ID for layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation
Design Verification Layout	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Layout_ID Layout_plan description Metal layer Voltage domain Manufacturer ID Layout_ID Layout_ID Layout_ID Order ID Order ID Silicon wafer type	VARCHAR	100 400 400 400 400 400 400 400 400 400	Primary key Foreign Key	Y Y N N N Y Y Y N N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N N Y Y Y N N Y Y Y N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y N N N Y Y N N N N Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design IP status of the design IP status of the design Unique ID for a verification Unique ID for a employee working on verification Unique ID for all the orders Unique ID for all the orders Unique IDs for all the orders Unique IDs for bugs that are found in design Description of bugs that are identified Register to track the bugs that are found in design Unique IDs for the design that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for all the orders Unique ID of employees working on identifying bugs Unique ID of or playout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation Unique ID for a layout Unique ID for a layout Unique ID for a layout
Design Verification Layout	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout_ID Layout_ID Layout_plan description Metal layer Voltage domain Manufacturer ID Layout_ID Layout_ID Layout_ID Order ID Order ID Silicon wafer type	VARCHAR	100 400 400 400 400 400 400 400 400 400	Primary key Foreign Key Foreign Key Primary key Foreign Key	Y Y N N N Y Y Y N N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N N Y Y Y N N Y Y Y N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y N N N Y Y N N N N Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design IP status of the design IP status of the design Unique ID for a verification Unique ID for a employee working on verification Unique ID for all the orders Unique ID for all the orders Unique IDs for all the orders Unique IDs for bugs that are found in design Description of bugs that are identified Register to track the bugs that are found in design Unique IDs for the design that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for all the orders Unique ID of employees working on identifying bugs Unique ID of or playout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation Unique ID for a layout Unique ID for a layout Unique ID for a layout
Design Verification Layout	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Layout plan description Manufacturer ID Layout iD Order ID Layout ID Order ID Layout ID Order ID Layout ID Order ID Silicon wafer type Fabrication process type	VARCHAR	100 100 100 100 100 100 100 100 100 100	Primary key Foreign Key	Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y N N N Y Y Y N N N Y Y Y Y N N N Y Y Y Y N N N Y Y Y Y Y N N N Y	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design IP status of the design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for an employee working on verification Unique ID for althe orders Unique IDs for althe orders Unique IDs for the designs Register to track the bugs that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique ID for althe orders Unique ID for layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation Unique ID for a layout Unique ID for a layout Unique ID for an order Description of the material type used for silicon manufacturing process Description of methodology type
Design Verification Layout	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Design_ID Usign_ID U	VARCHAR VARCHA	100 100 100 100 100 100 100 100 100 100	Primary key Foreign Key	Y Y Y N N N Y Y Y N N N Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y N N Y Y N N N Y Y Y N N N N Y Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for all the orders Unique ID for all the orders Unique ID for all the orders Unique ID for bugs that are found in design Description of bugs that are identified Register to track the bugs that are found in design Unique ID of employees working on identifying bugs Unique ID of employees working on identifying bugs Unique ID of employees working on identifying bugs Unique ID of or all the orders Unique ID of rol ayout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation Unique ID for a layout Unique ID for a layout Unique ID for a norder Description of the material type used for silicon manufacturing process Description of the material type used for silicon manufacturing process Description of the material type used for silicon manufacturing process
Design Verification Layout Silicon manufacturer	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Design_ID Layout_ID Employee ID ORDER_ID Design_ID Silicon wafer type Fabrication process type Fabrication process type Sales ID Employee ID Order ID	VARCHAR VARCHA	100 400 400 400 400 400 400 400 400 400	Primary key Foreign Key Foreign Key Foreign Key Primary key Foreign Key	Y Y N N N Y Y Y N N N Y Y Y N N Y Y Y N N Y Y N N Y Y N N Y Y N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y N N N Y Y Y Y N N N Y Y Y Y Y N N N Y Y Y Y Y N N N Y Y Y Y Y N N Y Y Y Y Y Y N N Y Y Y Y Y Y N N Y Y Y Y Y Y N N Y Y Y Y Y Y N N Y	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design IP status of the design IP status of the design Unique ID for a verification Unique ID for an employee working on verification Unique ID for all the orders Unique ID for all the orders Unique ID for all the orders Unique ID for blugs that are found in design Description of bugs that are identified Register to track the bugs that are found in design Unique ID for all the orders Unique ID for all the orders Unique ID for all the orders Unique ID for the design Register to track the design that are found in design Description of all the orders Unique ID for all the orders Unique ID for all the orders Unique ID for layout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation Unique ID for a layout Unique ID for a layout Unique ID for a layout Unique ID for an order Description of the material type used for silicon manufacturing process Description of methodology type Unique IDs for the sales Unique IDs for the sales Unique IDs for all the employees Unique IDs for all the employees Unique IDs for all the employees
Design Verification Layout Silicon manufacturer	Manager first name Manager last name Department name Department name Design_ID Order ID Employee ID Features DStart date DEnd date IP Verification_ID Employee ID ORDER_ID Design_ID Bugs logged-in-date Bugs description Bugs logged-out-date Layout_ID Employee ID ORDER_ID Design_ID Design_ID Usign_ID U	VARCHAR VARCHA	100 100 100 100 100 100 100 100 100 100	Primary key Foreign Key	Y Y N N N Y Y Y Y N N N N Y Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y Y N N Y Y Y N N Y Y Y Y N N Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y Y N N Y Y N N Y Y N N Y Y Y N N Y Y N N Y Y Y N N Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y Y N N Y Y Y N N Y Y N N Y Y Y N N Y Y N N Y Y N N Y Y N N Y Y Y N N N Y Y N N Y Y N N N Y Y N N N Y Y N N N Y Y N	first name of employee Last name of employee department name Unique ID for a design Unique ID for orders Unique ID for a employee working on design Description of design features Start date of design End date of design IP status of the design Unique ID for a verification Unique ID for a verification Unique ID for an employee working on verification Unique ID for an employee working on verification Unique ID for all the orders Unique IDs for the designs Register to track the bugs that are found in design Description of bugs that are identified Register to track closing dates of bugs that are found in design Unique IDs for the layouts Unique IDs for the layouts Unique IDs for the layouts Unique ID for all the orders Unique ID for all yout team to track the design they are layouting Description of chip planning like shape of chip etc. Metal layer describes type of mental used in chip layout simulation Domain simulates type of power domain used for layour simulation Unique ID for a layout Unique ID for a layout Unique ID for a layout Unique ID for methodology type Unique IDs for the sales Unique IDs for the sales Unique IDs for the sales