Instruction Set Architecture

Category	Opcode (Binary)	Mnemonic	Format	Operation	ALU Action
ARITHMETIC	0000	ADD Rd, Rs1, Rs2	R	Rd = Rs1 + Rs2	A + B
	0001	SUB Rd, Rs1, Rs2	R	Rd = Rs1 - Rs2	A - B
	0010	MUL Rd, Rs1, Rs2	R	Rd = Lower(Rs1 * Rs2)	A * B
	0011	DIV Rd, Rs1, Rs2	R	Rd = Rs1 / Rs2	A / B
LOGIC	0100	AND Rd, Rs1, Rs2	R	Rd = Rs1 & Rs2	A & B
	0101	OR Rd, Rs1, Rs2	R	Rd = Rs1 | Rs2	A | B
	0110	XOR Rd, Rs1, Rs2	R	Rd = Rs1 ^ Rs2	A ^ B
DATA MOVEMENT	0111	MOV Rd, Rs1	R	Rd = Rs1	Passthrough (A + 0)
	1000	LDI Rd, Imm	I	Rd = Immediate	Passthrough (0 + Imm)
	1001	LD Rd, [Rs]	I	Rd = Mem[Rs]	A + 0 (Calc Address)
	1010	ST Rs, [Rd]	I	Mem[Rd] = Rs	A + 0 (Calc Address)
CONTROL FLOW	1011	CMP Rs1, Rs2	R	Flags = Rs1 - Rs2	SUB (Don't save result)

	1100	JMP Addr	J	PC = Addr	Idle
	1101	BZ Addr	J	if (Z==1) PC = Addr	Idle (CU checks Flag)
	1110	BNZ Addr	J	if (Z==0) PC = Addr	Idle
	1111	HALT	-	Stop Clock	Idle