**Interface**

The inputs contain a 32-bit register from the Data Memory module (mem\_read\_data) and ALU (mem\_alu\_result); and a 1-bit select mode (memtoreg). The MUX would output a 32-bit data (wb\_data) to the Instruction Decode stage register.

**Implementation**

We just instantiated the MUX3 from Execute again since this only needs one MUX. The only difference is that mem\_alu\_result and mem\_read\_data are placed in reverse when inputting “a” and “b” since “a” had 1 while “b” was 0 in the Execute stage. The Write Back stage would have “a” as 0 and “b” as 1.