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DA+BMAC: Distance-Aware Bidirectional Medium Access Control for Mesh Wireless Network-on-Chip

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ABSTRACT Medium access control (MAC) protocol and routing strategy significantly influence Wireless Network-on-Chip (WiNoC) performance and energy characteristics. Conventional WiNoC MAC typically utilizes a daisy-chained ring topology, which limits wireless channel performance due to maximum waiting times when a radio hub misses the token before packet arrival. Additionally, due to limited wireless channel bandwidth compared to aggregate wired interconnect capacity, radio hubs become susceptible to congestion when multiple processing cores simultaneously request wireless access. The lack of intelligent traffic control leads to indiscriminate wireless transmission even when efficient wired paths are available. This paper proposes DA+BMAC, a Distance-Aware (DA) Bidirectional Medium Access Control (BMAC) scheme for mesh WiNoC architecture. BMAC employs bidirectional links allowing token reversal when it overshoots an idle radio hub, reducing worst-case token wait time. DA+BMAC implements distance-aware routing to reserve single-hop wireless transmission exclusively for source-destination pairs beyond a specific distance threshold, while dedicating wired interconnects with higher aggregate bandwidth to short-range communication. Comprehensive validation using a cycle-accurate Noxim simulator on an 8 × 8 mesh with 16 radio hubs demonstrates up to 11.49× throughput improvement and 15% energy savings compared to a baseline token-ring WiNoC. Scalability analysis confirms performance benefits extend to larger networks (256 and 1024 cores), making DA+BMAC suitable for future many-core systems. The proposed approach has been validated using both synthetic traffic distributions (random, shuffle, transpose, and hotspot) and real-application traces (Barnes and Fluidanimate) from PARSEC and SPLASH-2 benchmark suites, confirming its effectiveness across diverse workloads.

INDEX TERMS Bidirectional medium access control, distance-aware routing, mesh topology, network-on-chip, on-chip interconnects, packet switching, token passing, wireless network-on-chip.

I. INTRODUCTION

In the era of chip multiprocessors (CMP), modern processors contain an ever-increasing number of integrated

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processing cores, and network-on-chip (NoC) architectures are widely recognized as robust solutions for future on-chip interconnects [1], [2], [3]. NoC adapts networking theory based on packet switching and comprises multiple interconnected routers built using point-to-point channels coordinated to form specific topological structures. Currently, NoC is

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the preferred choice for chip multiprocessor interconnect networks because it provides substantial enhancements to on-chip interconnect scalability, fault tolerance, and modularity with appropriate routing scheme design or control flow mechanism revisions [4], [5], [6].

In general, the scaling of parallel applications increases the ratio of communication to computation as computation is distributed across numerous processing cores [7]. The increase in processing core density implicates a broader selection of possible destinations, making the traffic more dynamic with a higher degree of traffic heterogeneity due to increased communication [8], [9]. With the expansion of processing core numbers, the performance benefit of conventional NoC is restricted by high latency and higher power dissipation due to long-distance multiple-hop communication. One of the critical challenges of the growing number of processing cores is the average packet traversal distance, which affects the time and energy required for data movement across the chip die. This calls for innovative alternative architectures that can offer shorter connection paths between distant processing cores.

As integration levels continue to rise, these NoC interconnects face serious scalability constraints, inspiring research into emerging interconnect technologies such as optical NoC (oNoC) [10], [11], [12], three-dimensional (3D) NoC [13], [14], [15], RF-interconnection (RF-I) [16], [17], [18], and Wireless NoC (WiNoC) [19], [20], [21]. Each of these on-chip interconnect alternatives has unique features with distinct advantages and disadvantages [19], [22], [23]. Among these, WiNoC communication has garnered interest in recent research due to several compelling capabilities [19], [20], [21]. First, this interconnect is Complementary Metal-Oxide Semiconductor (CMOS) compatible [24] and can transmit data across the chip via a one-hop wireless link with low energy while providing high bandwidth with low latency. Furthermore, because wireless transmission does not require wireline metal interconnects or waveguides, the WiNoC platform provides architectural flexibility, reducing area overhead and chip design complexity.

WiNoC refers to an innovative NoC architecture that combines wired and wireless interconnects to address the issue of extended latency in wired planar communication by incorporating dedicated long-range wireless channels [19], [21], [24], [25], [26]. Advances in integrated transceivers [27], [28] and millimeter-wave antennas [29], [30] have motivated the development of WiNoC as a possible complement to conventional NoC [31]. A set of processing cores are integrated with antennas and transceivers that can modulate and transmit data packets for wireless on-chip transmission. With WiNoC, long-distance cores can communicate with one-hop low latency. Additionally, beyond a certain sourceto-destination distance, the performance enhancement using the WiNoC wireless channel is greater because the wireless channel consumes less energy compared to multi-hop traditional metal wires [32], [33], [34].

The design of low-area-overhead and efficient MAC protocols represents a fundamental challenge for WiNoC technology [34], [56], [57]. Existing MAC approaches predominantly employ daisy-chained ring topologies with token-passing mechanisms due to their simplicity and collision-free operation [34], [46], [58], [59], [60], [61]. However, these approaches suffer from significant performance limitations: unidirectional token circulation creates worst-case waiting times proportional to ring size, while indiscriminate wireless channel usage leads to congestion even when efficient wired paths are available. Besides, due to limited wireless channel bandwidth compared to aggregate wired interconnect capacity, radio hubs become susceptible to congestion when multiple processing cores simultaneously request wireless access [60], [68], [69], [70], [71], [72], [73]. This creates network contention that affects the high-speed advantages of wireless links [67], [68], [69], [74]. The challenge is compounded by the lack of intelligent traffic driving mechanisms that can dynamically balance load between wired and wireless communication planes.

This paper proposes DA+BMAC, a Distance-Aware Bidirectional Medium Access Control scheme for mesh WiNoC architecture. DA+BMAC addresses two key limitations in conventional WiNoC designs: (1) the inefficient token distribution in daisy-chained token rings that causes long waiting times, and (2) the unbalanced utilization of wireless and wired resources that leads to network congestion. Our approach consists of two complementary techniques:

- 1) Bidirectional MAC (BMAC): Introduces bidirectional links in the token ring, allowing the token to reverse direction when it overshoots an idle radio hub. This reduces worst-case token waiting time by up to 48%.
- 2) Distance-Aware (DA) routing: Implements distance-based traffic steering that reserves wireless transmission exclusively for source-destination pairs beyond a specific distance threshold (empirically determined to be 5 hops in our 8×8 mesh), while dedicating wired communication for shorter distances.

The contributions of this paper are as follows:

- 1) We introduce BMAC, a bidirectional token-based MAC protocol that significantly improves token distribution efficiency with minimal hardware overhead.
- 2) We present a systematic methodology for determining the optimal distance threshold for traffic steering between wired and wireless networks.
- 3) We integrate BMAC with Distance-Aware routing to create DA+BMAC, a comprehensive solution that balances the network load between wired and wireless planes.
- 4) We validate our approach through extensive simulations using both synthetic traffic patterns and real application traces, demonstrating substantial improvements in throughput (up to $11.49 \times$) and energy efficiency (up to 15%).
- 5) We demonstrate the scalability of our approach with larger network configurations (256 and 1024 cores), confirming its suitability for future many-core systems.



The remainder of this paper is organized as follows. Section II provides an overview of related works. Section III describes the proposed DA+BMAC scheme in detail. Section IV presents performance evaluation and experimental results. Finally, Section V concludes the paper and discusses future work.

II. RELATED WORKS

Token-passing ring is a type of channel coordinate access protocol that time-slices access to wireless channels fairly among radio hubs [35]. In the token-passing method, hub nodes in a WiNoC are organized into a logical ring. A special packet called a token circulates through the ring to determine which hub node has the right to send data packets through the wireless channel. Many works in the literature have adopted the token-based approach as the preferred MAC protocol [21], [24], [26], [36], [37], [38], [39], [40].

The first research effort employing a token-based MAC protocol for WiNoC was from DiTomaso et al. [21], which presented inter-router wireless scalable express channel (iWISE) as a proposed WiNoC architectural structure. This architecture is equipped with a scalable wireless inter-router express link for WiNoC capable of enhancing system performance by minimizing the average hop count for communication. Additionally, power dissipation is reduced through the proposed hybrid wireless communication link while area overhead is lowered by utilizing smaller buffers and routers. In [24], the same authors presented a token-sharing protocol with an adaptable algorithm to effectively use wireless bandwidth for the Adaptive WiNoC (A-WiNoC) architecture. A-WiNoC is a scalable architecture that dynamically reassigns links in response to bandwidth demand from various processing cores. The token is passed among router nodes and enables transmission on a particular wireless link. This scheme was chosen because the token can be immediately passed among routers with minimal waiting time for data transmission. The experimental results showed 21% energy enhancement with 37% throughput improvement [24].

Token-passing MAC arbitration was also proposed in [26] and [33] for hierarchical CMOS-compatible small-world architecture operated in the mm-wave frequency spectrum. This architecture utilizes the long-range single-hop high-bandwidth wireless expressway to alleviate multi-hop wired interconnect in conventional NoC. The token-based passing scheme bypasses the demand for synchronization and a centralized control mechanism. In this protocol, the particular wireless hub node that possesses the token is allowed to forward dedicated flits via the wireless medium at a similar frequency band. Once flits are wholly transmitted, the token is released to the next wireless hub. This proposed work demonstrated better performance compared to NoC with metal interconnect in terms of energy efficiency and achievable bandwidth.

Palesi et al. [41] proposed a radio access control mechanism called RACM that improves both the energy and

performance of WiNoC. For each radio channel, the proposed RACM arbitrates access to the radio medium using a token-based mechanism. A token is circulated through radio hubs in a ring-like fashion and allows the radio hub holding the token to utilize radio communication for a certain number of clock cycles.

The token ring concept can be extended to support multiple subnets. A WiNoC architecture inspired by honeycomb topology also employing token-passing as a medium access protocol was proposed by Afsharmazayejani et al. [37]. The proposed hybrid reconfigurable WiNoC architecture, named honeycomb-based wireless NoC (HoneyWin), utilizes a wireline network at the base layer, equipped with a five-port conventional router connected to the processing core. At the upper layer, wireless interconnection is formed by a set of wireless routers. Simulation results demonstrated that this proposed work improves network throughput by 10% and conserves 10% of energy consumption [37].

Random-access protocols, also known as contention or best-effort approaches, are alternatives to token-based methods. In these techniques, every radio hub has access to the shared wireless channel without being dominated by any other radio hub. In WiNoC, several works have adopted this protocol [42], [43]. Piro et al. [42] presented two baseline MAC protocols based on carrier-sense multiple access (CSMA) [44] and ALOHA [45] schemes for a wired and wireless hybrid Graphene-based Wireless-NoC (GWNoC) network architecture. In this system, every processing core is integrated with a graphene antenna operating in the terahertz frequency range. Their work verified that the CSMA-based approach outperformed the ALOHA-based protocol by better exploiting the wireless link [42].

Mestres et al. [43] proposed the Broadcast, Reliability, and Sensing MAC protocol (BRS-MAC) which uses WiNoC context particularities to meet strict requirements. BRS-MAC is a protocol between CSMA/CD and CSMA/CA that utilizes the chip environment's sensing capabilities. This protocol employs a contention detection and notification strategy that scales with the number of receivers, making it compatible with broadcast communications. The main design features are a scalable negative acknowledgment (NACK) mechanism and preamble-based collision detection. The work was validated with performance modeling and proved this protocol could achieve 27% improvement in peak throughput compared to traditional CSMA [43].

Hybrid MAC approaches combine various MAC protocols. For instance, hybrid channelization approaches, such as combining FDMA and TDMA, have been proposed in [46] and [47]. Additionally, hybrid MAC protocols integrating carrier sensing and token-based methods are presented in [48] and [49].

Ganguly et al. [46] leveraged 24 different frequencies [50] of continuous-wave laser sources for CNT-based antennas in small-world WiNoC infrastructure. On top of the FDMA technique, the number of different channels can be increased by utilizing a simple TDMA approach. For signal interference



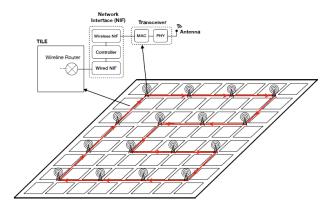


FIGURE 1. A conceptual illustration of top-level perspective of 8×8 (64) cores mesh-WiNoC architecture with 4×4 (16) radio hub. Note that the unidirectional daisy-chained token ring link is represented by the bold red arrows.

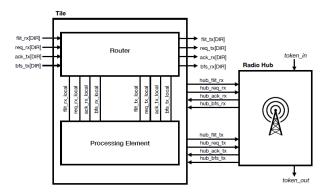


FIGURE 2. Functional block diagram for microarchitectural components of Tile-Radio Hub. Note that there are unidi- rectional links (token_in and token_out) at the Radio Hub component.

avoidance, these frequencies are designated to multiple wireless channels so that single-frequency links are used only once. Their proposed work exceeded the wireline counterpart in terms of transmission delay and network throughput while improving energy consumption [46]. Similarly, Bahrami et al. also employed a combination of TDMA and FDMA techniques as a MAC protocol in their proposed hierarchical WiNoC structure based on an analytic hierarchy process [47]. The suggested architecture uses fewer radio hubs, allowing communication within the subnet to be accomplished with fewer wireline links. Simulation results showed this approach could help WiNoC interconnects operate better.

Mansoor et al. [48] proposed a dynamic MAC that sets wireless links based on traffic conditions. Their work is based on an adaptive policy that switches between token passing and CSMA protocol based on the degree of contention. This dynamic MAC has dual-functional modes (token passing and CSMA) depending on the wireless utilization of radio hubs. When radio hub utilization is low, the dynamic MAC runs in CSMA mode. When wireless utilization is high, the

WiNoC switches to token passing mode. This interconnection system integrating wireless links to an NoC fabric adapts to address non-uniformity in traffic distribution demanded in large multicore chips. Furthermore, Fernando et al. presented an ad–aptive MAC technique combining CSMA and token based approaches in their proposed WiNoC architecture known as Replica [49]. Replica's MAC approach adapts between CSMA and token passing based on workload application characteristics. For instance, CSMA is adopted for applications with sparse transmission, while token-based is used for bursty workload applications.

Our proposed DA+BMAC differs from these approaches in two key aspects. First, while existing works such as iWISE [21], A-WiNoC [24], and RACM [41] employ unidirectional token circulation, DA+BMAC introduces bidirectional token movement that reduces significant worst-case token waiting time. Unlike these approaches where tokens must complete full ring traversals, our bidirectional mechanism allows immediate service to adjacent radio hubs with pending requests, significantly improving token distribution efficiency. Second, compared to conventional CSMA-based approaches [42], [43] that suffer from collisions and exponential backoff delays at high injection rates, DA+BMAC maintains collision-free operation while achieving 45% higher throughput than adaptive CSMA and 68% higher than ALOHA-based protocols. Our deterministic token-based approach eliminates the unpredictable delays inherent in contention-based schemes.

Next, while the static TDMA/FDMA schemes [46], [47] provide deterministic channel access, they lack adaptability to dynamic traffic patterns and often result in channel underutilization. DA+BMAC achieves higher throughput than the current static TDMA/FDMA schemes [46], [47] through intelligent traffic steering that adapts to communication distance patterns, ensuring optimal utilization of both wireless and wired resources. Finally, our proposed DA+BMAC provides consistent performance through its integrated bidirectional token management and distance-aware routing, compared to complex adaptive schemes that switch between CSMA and token-passing based on network conditions. This comprehensive approach addresses both the MAC and routing layers, leading to superior performance across diverse traffic patterns.

III. THE PROPOSED DA+BMAC

A. TOP-DOWN PERSPECTIVE OF 8 × 8 MESH WINOC

This section lays out an abstraction hierarchy for the topological structure implemented in this work. Figure 1 depicts a schematic diagram representing the top-level perspective of the 8×8 (64) processing core mesh-WiNoC with 4×4 (16) radio hubs. In this research, 16 radio hubs are used at the upper layer of architecture to provide all tiles with access to wireline and wireless interconnection. The daisy-chained token ring links are constructed edge-to-edge between these

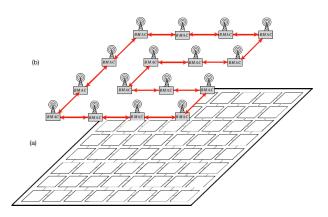


FIGURE 3. The two-tier mesh-WiNoC architecture with the proposed joint scheme of DA+BMAC (a) The proposed architecture is at the lower layer of the wireline plane (b) The proposed BMAC is employed at the upper-layer of the mesh-WiNoC with its neighbour-aware mechanism and the bidirectional links to allow the token to serve the previous adjacent radio hub for utilising the wireless channel for data packet transmission.

radio hub nodes, as represented by the bold red arrows in Figure 1.

At the bottom-level perspective, Figure 2 shows the functional block diagram (FBD) with interconnection details between the NoC tile modules and radio hub modules. As can be seen, the *token_in* and *token_out* links are unidirectional. This architecture is adopted as the baseline token-based MAC design in this work.

B. BIDIRECTIONAL MAC (BMAC) PROTOCOL

This section proposes an improved MAC protocol called Bidirectional MAC (BMAC) at the upper layer of the mesh-WiNoC architecture hierarchy. The MAC protocol defines how a radio hub can reliably access the wireless channel for data packet transmission. This procedure is critical to ensure successful wireless transmission by avoiding two or more simultaneous accesses to the same wireless link. As illustrated in Figure 3, mesh-WiNoC can be represented by two-tier planes: the wireless plane at the upper layer and the wireline plane at the lower layer.

BMAC addresses the upper layer of mesh-WiNoC as depicted in Figure 3. Daisy-chained token-based MAC remains the choice for WiNoC MAC due to its simplicity and collision-free protocol [21], [24], [26], [36], [37], [38], [39], [40]. However, the worst-case maximum token waiting time can be reduced by allowing the token to return to its immediately passed radio hub. With the neighbor-aware token controller mechanism, BMAC uses bidirectional links to grant the token the ability to turn to the previous adjacent radio hub, preventing the full- round maximal waiting time for token discovery in the next token cycle.

1) RF TRANSCEIVER SPECIFICATIONS AND PARAMETERS

The radio hub architecture integrates a specialized RF transceiver operating in the millimeter-wave frequency band. For our implementation, we utilize a 60 GHz

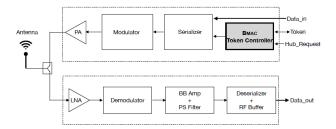


FIGURE 4. Enhanced radio hub architecture with BMAC token controller and bidirectional link.

TABLE 1. Rf specifications in the proposed DA+BMAC architecture.

Parameter	Value	Unit	
Carrier Frequency	60	GHz	
Channel Bandwidth	16	GHz	
Modulation Scheme	OOK (On-Off Keying)	-	
Data Rate	16	Gbps	
Antenna Type	On-chip zigzag dipole	-	
Antenna Gain	3	dBi	
Power Amplifier Output	0.5	mW	
Power Amplifier Efficiency	15	%	
Receiver Sensitivity	-55	dBm	
Bit Error Rate (BER)	10-12	-	

carrier frequency, which offers an optimal balance between bandwidth availability and propagation characteristics within the chip's silicon substrate. This frequency selection aligns with recent advancements in on-chip mm-wave technologies [33], [52] while ensuring compatibility with CMOS fabrication processes. Table I details the RF specifications used in our BMAC implementation.

The transceiver design employs On-Off Keying (OOK) modulation for its simplicity and energy efficiency, crucial factors in the WiNoC context. While more complex modulation schemes could provide higher spectral efficiency, OOK offers the best power-performance tradeoff for our implementation [52]. The zigzag dipole antenna structure was selected for its compact footprint $(120\mu m \times 60\mu m)$ and quasi-omnidirectional radiation pattern, which ensures signal reception across the entire chip with minimal path loss variation.

Our power analysis incorporates the RF front-end energy consumption based on the ORION-RF model [53], which accounts for the transceiver's active, idle, and sleep power states. The power amplifier output of 0.5mW with 15% efficiency represents a realistic compromise between transmission range and energy consumption in current CMOS processes. These parameters directly inform our energy calculations in Section IV, providing a more accurate representation than generic energy models.

2) BMAC CONTROLLER ARCHITECTURE

The BMAC token controller, as depicted in Figure 4, consists of three primary components:

6) Direction Control Logic: Monitors token flow and determines when direction reversal is beneficial



- 7) Token State Machine: Manages token possession, transmission, and release
- Neighbor Awareness Module: Tracks activity at adjacent radio hubs

The direction control logic requires approximately 150 gates additional hardware beyond the baseline token controller, representing a minimal 3% area overhead per radio hub. The basic architecture of a radio hub transceiver consists of two main components: the transmitter and the receiver, which both share a common antenna through an RF switch, as depicted in Figure 4. At the transmitter end, the main function is to adapt a baseband digital signal to the wireless channel medium. The bidirectional MAC token controller grants access and ensures the wireless medium is not occupied during transmission. In cases where the previous immediate neighbour radio hub misses the token, the BMAC token controller allows a backward turn with its bidirectional link.

When the wireless channel is available for transmission, the incoming data flits are converted in a serial manner by the serializer. The modulator then converts the data flit into a higher frequency signal delivered to the on-chip antenna through the power amplifier. At a given frequency, these radio wireless signals propagate within the chip and can be received by any other antenna within the radio hub range. The internal structure of the receiver end is the opposite of the transmitter end. The wireless signal is converted into a baseband stream of data by the demodulator. The deserializer then reconverts the serial data stream into a flit for transmission to its destination core.

The BMAC protocol is formally described in Algorithm 1, with enhanced clarity and precise operational details. The implementation prioritizes low latency token handling with a worst-case decision time of 2 clock cycles, ensuring that the direction control logic does not introduce critical path delays in the token circulation.

The BMAC token control algorithm implements an efficient bidirectional token management system. The main procedure (lines 1-14) first identifies the previous and *next_hub_ID*s in the token ring. It then checks if the previous hub has a pending wireless transmission request while the next hub does not. If this condition is true, the token direction is reversed to serve the waiting previous hub, optimizing token distribution and reducing waiting time. Otherwise, the token continues its normal forward circulation.

The token reversal procedure (lines 15-22) handles the mechanics of sending the token backward, with special consideration for the edge case of the first hub (hub 0), which must send the token to the last hub in the ring. The normal token circulation procedure (lines 23-26) simply passes the token to the next sequential hub in the ring. This bidirectional approach significantly reduces worst-case token waiting time compared to traditional unidirectional token rings, as radio hubs can immediately serve their adjacent neighbors rather than waiting for a complete ring traversal.

C. DISTANCE-AWARE ROUTING WITH BIDIRECTIONAL-MAC PROTOCOL (DA+BMAC)

Due to the fact that wireless channel bandwidth is much less than the aggregate bandwidth of wireline, WiNoC can easily become a bottleneck when wireless resources are excessively used. When all tiles connected to radio hubs transmit through them, high network contention occurs as wireless resources are limited. WiNoC performance can be improved when the interplay between wireline and wireless planes is appropriately selected to control optimal workload transmission.

Algorithm 1 Proposed Pseudocode for BMAC Protocol

// Main routine for token direction decision

1: **procedure** BMAC_TOKEN_CONTROL (current_hub_id)

- 2: // Check if previous adjacent hub has pending request
- 3: prev_hub_id ← (current_hub_id 1) % TOTAL_HUBS
- 4: next_hub_id ←(current_hub_id +1) % TOTAL_HUBS
- 6: if HAS PENDING REQUEST (prev hub id) AND
- 7: NOT HAS PENDING REQUEST (next hub_id) then
- 8: // Activate bidirectional mode
- 9: REVERSE TOKEN DIRECTION()

10. else

- 11: // Continue with baseline token circulation
- 12: MAINTAIN TOKEN DIRECTION()
- 13: end if
- 14: end procedure

//Reverse token direction to serve previous hub

- 15: procedure REVERSE TOKEN DIRECTION()
- 16: **if** $current_hub_id = 0$ **then**
- 17: // Special case: first hub in ring
- 18: SEND_TOKEN(TOTAL_HUBS 1) // Send to last hub
- 19: **else**
- 20: SEND_TOKEN (current_hub_id 1)
- 21: end if
- 22: end procedure

// Continue with normal token circulation

- 23: procedure MAINTAIN_TOKEN_DIRECTION()
- 24: $next_hub_id \leftarrow (current_hub_id+1) \% TOTAL_HUBS$
- 25: SEND TOKEN (next hub id)
- 26: end procedure

The proposed DA+BMAC enhances the routing approach for WiNoC architecture by optimally balancing the network workload between upper and lower layers, as shown in Figure 3. The DA mechanism is proposed at the underlying wired mesh-WiNoC as a way to complement the BMAC protocol at the upper layer for balancing the load between wireline and wireless planes. For this purpose, short-range communication is conducted through the wireline metal planar that has much higher aggregate bandwidth, while long-range far-apart communication can be established through a wireless channel. In particular, for source and destination tiles beyond a certain distance threshold, DA+BMAC applies a



distance-aware routing strategy to manage single-hop wireless transmission.

Mesh-WiNoC can be visualized as a two-tier network, in which the bottom layer is a standard wired NoC and the upper layer consists of a set of radio hubs (transceivers) to enable wireless communication. WiNoC interconnects are not expected to completely substitute wired interconnects but instead to complement them. This approach consists of integrating a wireless radio hub into a set of routers.

Figure 5 sketches a 64 cores (8 × 8) mesh-WiNoC architecture with 16 radio hubs. The selection of 64 cores represents current CMP trends and complies with application benchmark suites used in this feasibility study [2], [3]. In the figure, each radio hub is connected to four tile cores, i.e., 16 radio hubs attached to 64 tiles, resulting in 100% radio hub-core density for the 64 processing cores in the mesh-WiNoC network. This provides an even distribution of radio hubs in the mesh-WiNoC architectural structure, with all tiles having access to both wireless channels and wireline links.

The key idea behind this concept is to reduce the latency produced by multi-hop communication in wired-NoC with one-hop wireless link communication. Given the example in Figure 5, two-dimensional (2D) wired-mesh requires 12 wireline hops for the packet to arrive at its destination tile when XY routing is employed, as represented by the bold black arrows. Interestingly, for the same scenario, such long-distance communication is achievable with a single hop by employing wireless communication through radio hubs, as depicted by the dotted line arrow. The routing strategy requires modification to prioritize the wireless network for serving long-range communication, while the rest of the communications are served by the wired interconnect. Thus, first, the distance (hop count) between source-destination tiles needs to be determined to ensure long-distance communication is assisted by the wireless channel. For a standard mesh network, given the subscripts of x and y denote the x- and y-coordinates, the Manhattan distance (d_M) is used to formulate the distance, expressed as in equation (1) [54].

$$d_{M}(i,j) = |i_{x} - j_{x}| + |i_{y} - j_{y}|$$
 (1)

1) THRESHOLD DISTANCE SELECTION METHODOLOGY

The effectiveness of DA+BMAC critically depends on determining the optimal threshold distance for routing decisions. We developed a systematic methodology to identify this threshold through a combination of analytical modeling and empirical evaluation.

Our analytical model considers three key factors:

- The relative latency between wireless and wired transmission
- Network contention effects at varying distances
- Energy consumption tradeoffs

For a packet traversing the mesh network, the end-to-end latency can be modeled as:

$$L_{wired}(d) = H_r \times T_r + (d-1) \times T_l + T_s \tag{2}$$

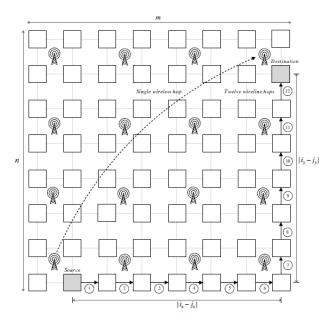


FIGURE 5. A conceptual illustration of single-hop wireless (dotted line arrow) versus twelve (12) multi-hops wired (bold black arrows) communication from the source to the destination.

where:

- Lwired (d) is the wired latency for distance d
- H_r is the average router delay (3 cycles in our implementation)
- T_r is the clock period
- *d* is the Manhattan distance between source and destination
- T_l is the link traversal time (1 cycle)
- T_s is the serialization delay

For wireless transmission, the latency model is:

$$L_{wireless}(d) = T_{token} + T_{serialize} + T_{wireless} + T_{descriptive} + 2 \times H_r \times T_r$$
(3)

where.

- $L_{wireless}(d)$ is the wireless latency for distance d
- T_{token} is the average token acquisition time
- T_{serialize} is the time to serialize the packet for wireless transmission
- Twireless is the wireless propagation time
- $T_{deserialize}$ is the time to deserialize the received packet

The crossover point where $L_{wired}(d) = L_{wireless}(d)$ provides an initial threshold estimate. We then conducted extensive simulations to refine this threshold, considering network contention effects under various traffic patterns.

Figure 6 shows the network throughput versus threshold distance for four synthetic traffic patterns at varying injection rates. Based on this analysis, we determined that a threshold distance of 5 hops represents the optimal value for our 8×8 mesh configuration with 16 radio hubs. This threshold maximizes throughput across different traffic patterns while providing consistent energy savings.

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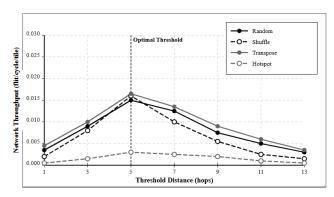


FIGURE 6. Network throughput as a function of threshold distance for various traffic patterns. The optimal threshold of 5 hops maximizes performance across different traffic patterns.

For larger network sizes, we found that the optimal threshold, $T_{optimal}$ scales approximately as:

$$T_{optimal} = \sqrt{N}/4$$
 (4)

where N is the number of cores in the network. This scaling relationship was validated through supplementary simulations on 16×16 (256-core) and 32×32 (1024-core) configurations.

2) ENHANCED DISTANCE-AWARE ROUTING ALGORITHM

The DA+BMAC routing algorithm integrates distance-awareness with the bidirectional MAC to optimize network performance. Algorithm 2 presents the DA+BMAC routing for mesh-WiNoC. The main procedure (lines 1-17) implements distance-aware routing by calculating the Manhattan distance between source and destination (lines 5-7) and comparing it to a predefined threshold (line 8). The predetermined threshold value is set to 5 hops for our 8×8 mesh configuration. When the distance exceeds this threshold, indicating long-range communication, the packet is directed to the wireless channel. Packets traveling long distances are routed through the wireless channel (lines 9-11), while short-distance packets use the wired mesh network (lines 13-15).

For wireless transmission, the

USE_WIRELESS_CHANNEL procedure (lines 18-30) applies the BMAC protocol, which allows token reversal when a pending request exists from the previous radio hub but not from the next hub (lines 24-26). This bidirectional capability reduces token waiting time compared to traditional token-ring approaches.

The USE_WIRED_CHANNEL procedure (lines 31-34) applies standard XY routing for wired communication. By reserving wireless transmission for long-distance communication and enabling bidirectional token circulation, this algorithm effectively balances network traffic and significantly improves both throughput and energy efficiency with minimal hardware overhead.

Together, these three components create a comprehensive routing solution that effectively balances traffic across both

Algorithm 2 Proposed Pseudocode for DA+BMAC Routing

// Main routing procedure for each packet

1: **procedure** DA_BMAC_ROUTE (packet, current_node, threshold)

2: $source \leftarrow packet.source$

3: $destination \leftarrow packet.destination$

4:

5: // Calculate Manhattan distance between source and destination

6: $distance \leftarrow | source.x-destination.$

x + |source.y-destination.y|

7:

8: **if** distance > threshold **then**

9: // Long-distance communication: use wireless channel

10: route to wireless \leftarrow true

11: USE_WIRELESS_CHANNEL (packet, current_node)

12: **else**

13: // Short-distance communication: use wired mesh

14: route_to_wireless ← **false**

15: USE_WIRED_CHANNEL (packet, current_node)

16: **end if**

17: end procedure

// Procedure for wireless channel routing with BMAC

18: **procedure** USE_WIRELESS_CHANNEL (packet, current node)

19: // Get the radio hub associated with current node

20: radio_hub ← GET_RADIO_HUB (current_node)

21: // Forward packet to radio hub

22: FORWARD_TO_RADIO_HUB (packet, radio_hub)

23: // Apply BMAC protocol for wireless transmission

24: if HAS_PENDING_REQUEST (radio_hub.prev) AND

25: NOT HAS_PENDING_REQUEST (radio_hub.next) then

26: APPLY BIDIRECTIONAL MAC (radio hub)

27: else

28: APPLY_BASELINE_MAC (radio_hub)

29: end if

30: end procedure

//procedure for wired channel routing

31: **procedure** USE_WIRED_CHANNEL (packet, current_node)

32: // Apply standard XY routing on mesh network

33: APPLY_XY_ROUTING (packet, current_node)

34: end procedure

planes of the network, leveraging the strengths of each interconnect type while mitigating their respective limitations.

3) HARDWARE IMPLEMENTATION CONSIDERATIONS

The DA+BMAC implementation requires minimal hardware additions to a standard mesh router. The distance calculation (Manhattan distance) is performed using two subtractors and an adder, with a comparison against the threshold value. This functionality adds approximately 200 gates per router,

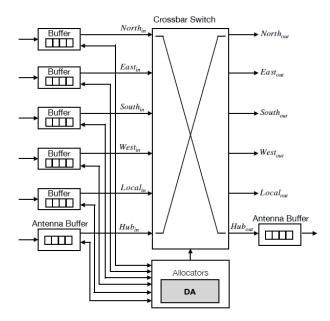


FIGURE 7. Router architecture with Distance-aware (DA) ar- bitration mechanism. Based on the source and destination communication distance between processing tiles, the DA arbitration mechanism adopts the distance threshold strategy for steering the data packets either by wired (north, east, south, or west) or wireless (radio hub) channel.

representing less than 5% area overhead compared to a baseline router. At the data link layer, BMAC reduces maximal waiting time by allowing tokens to reverse direction when the immediate previous radio hub has pending transmission requests while the next hub remains idle. This bidirectional capability is implemented through core components that monitors token flow patterns, manages possession and release protocols, and tracks adjacent radio hub activity states.

The threshold value is stored in a programmable register, allowing runtime adjustment for different traffic patterns or application requirements. This adaptive capability enables the system to optimize performance dynamically, though our experiments show that a fixed threshold of 5 works well across various synthetic and application traffic patterns. The critical path impact of the DA mechanism is minimal, as the distance calculation can be performed in parallel with routing table lookup, adding no additional latency to the router pipeline. The bidirectional token control logic similarly introduces no critical path delays, as the direction decision can be made before token transmission begins.

The design of the on-chip router architecture is one of the critical contributors to WiNoC system performance [55]. Figure 7 illustrates the proposed Distance-Aware (DA) router architecture interconnected with the receiver and transceiver of the radio hub counterpart. The main components of the DA router are constructed from buffer, allocator, and crossbar switch. For mesh topology, there are six directions: four cardinal directions (north, east, south, and west), one local direction for each processing element, and one direction for each radio hub component. When the input port receives

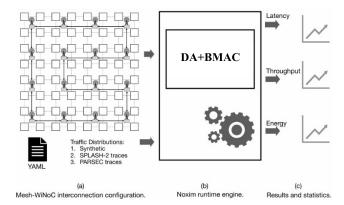


FIGURE 8. Methodology abstraction for simulation-based BMAC and DA+BMAC design space exploration. (a) YAML configuration file as an input to the WiNoC interconnect and its traffic distribution. (b) Cycle-accurate Noxim WiNoC simulator engine. (c) Simulation results and statistics in terms of latency, throughput, and energy consumption.

a packet, the DA mechanism computes the state of the wired or wireless selection based on the distance threshold depending on the distinct traffic characteristic. While BMAC optimizes token distribution at the MAC layer, DA routing ensures optimal traffic steering between wired and wireless planes based on communication distance thresholds. This dual-layer optimization prevents wireless channel overload while maintaining the collision-free advantages of token based-protocols.

When the wireless plane is preferred, the radio hub port output will be chosen for forwarding incoming packets wirelessly via an on-chip radio hub. In conjunction, the BMAC protocol, as described in Section III-B, is used as the radio access mechanism to perform wireless communication between processing tiles. Conversely, when the wireline plane is chosen, packet traversal goes through the crossbar switch to the output port (either north, east, south, or west) regardless of destination.

DA+BMAC integrates BMAC and the DA mechanism, which is implemented within the router microarchitecture as a traffic steering strategy to determine which planes to use, either wireless or wireline. Based on hop count distance between communication pairs, this approach carefully considers the strengths and limitations of each plane. For example, the wireless plane must not be overloaded as it can quickly become a bottleneck due to its modest bandwidth. In contrast, the wireline can be harnessed for short- and moderate-distance communications since it has the advantage of higher aggregate bandwidth. Accordingly, the DA+BMAC traffic steering mechanism is a critical determining factor that influences mesh-WiNoC performance.

IV. PERFORMANCE EVALUATION

A. DESIGN ENVIRONMENTS FOR NOXIM SIMULATOR

This section describes software tools, evaluation framework, and design environments for on-chip simulator platforms



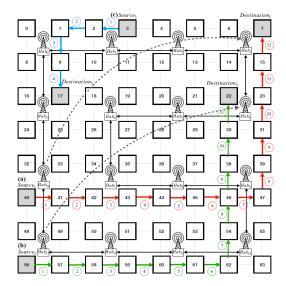


FIGURE 9. 64-cores mesh-WiNoC topology with 16 radio hubs. Each radio hub is integrated with the BMAC protocol and equipped with the bidirectional links in the daisy-chained ring topology. Every mesh-WiNoC tile has a DA routing mechanism for allowing traffic steering selection between wired or wireless transmission in the mesh-WiNoC architecture.

used in this research. The simulation of the BMAC protocol and DA routing technique in WiNoC architecture is important for design-space exploration and validation of these proposed designs. Figure 8 illustrates the evaluation environment implemented in this work. The custom-made cycle-accurate simulator based on Noxim [56] is used to evaluate performance. The mesh-based WiNoC topology is chosen because of its natural layout, easily mapped to an integrated circuit (IC) [4], [57]. Due to its physical regularity, this topology is also scalable and adaptable with a simple routing algorithm [4], [5]. The baseline architecture employs a token-ring access mechanism based on the work by Palesi et al. in [41]. In their work, a token circulates through radio hubs and allows the current hub holding the token to utilize the wireless radio medium in transmission mode for a certain number of clock cycles. The outputs of the mesh-WiNoC system simulation are data packet transmission latency, network throughput, and energy consumption.

B. SIMULATION SETUP

The simulation setup conducted in this research is depicted in in Table 2. The simulation uses 8×8 (64) processing cores, overlaid with 4×4 (16) radio hubs at the upper wireless layer to allow each NoC tile to have access to either the wired or wireless channel. All the simulations were executed for 100,000 cycles, and the first 1,000 clock cycles were used for system warm-up to a reach steady state. The experiment is based on the 8×8 mesh-WiNoC topological structure shown in Figure 9.

C. RESULTS OF BMAC

In this section, the performance evaluation of BMAC is conducted using various synthetic workloads, with latency and

TABLE 2. Simulation setup for 8 \times 8 cores mm-wave mesh winoc architecture with 16 radio hubs.

Parameter	Value	
Network Size	8×8 (64 cores)	
Radio Hub Nodes	4×4 (16 hubs)	
Radio Hub-Core Ratio	1:4 (25%)	
Topology	Mesh	
Link Width	16 bits	
Routing Algorithm	XY (Wireline), Single-hop (Wireless)	
Flow Control	Wormhole	
Selection Strategy	Random, Distance-Aware	
Wireless Frequency	60 GHz	
Wireless Data Rate	16 Gbps	
Packet Size	8 flits	
Flit Size	16 bits	
VC Buffer Size	4 flits	
Traffic Distribution	Random, Shuffle, Transpose, Hotspot	
Application Traces	Barnes (SPLASH-2), Fluidanimate (PARSEC)	
Simulation Parameters	Warm-up: 1,000 cycles, Simulation: 100,000 cycles	

throughput being the key performance metrics considered for comparison. The obtained results, depicting the average latency plotted against the packet injection rate (PIR), are illustrated in Figure 10. The BMAC approach is compared against the baseline token-ring MAC under various synthetic traffic conditions, namely (a) random, (b) shuffle, (c) transpose, and (d) hotspot.

In particular, the performance advantage of BMAC over baseline is more evident in the shuffle traffic pattern, as shown in Figure 10(b). In this traffic, BMAC can manage a maximum load of 0.029 flit/cycle/tile compared to 0.016 flit/cycle/tile for baseline token-ring MAC. This is because the communication patterns between pairs of nodes for shuffle traffic exhibit a traffic distribution among adjacent neighborhoods, enabling the BMAC approach to be feasible for this traffic.

The hotspot traffic pattern is employed to test BMAC's ability to handle unbalanced loads. The node at the center of the network is chosen as a hotspot with an 80% higher probability of receiving packets from other nodes. As shown in Figure 10(d), hotspot traffic demonstrates severe performance degradation compared to other traffic due to traffic injection being concentrated around the central hotspot node.

This particular node is loaded heavily and aggregates the congestion problem, causing saturation at a lower PIR. As can be observed, although both protocols were saturated at similar PIR, the BMAC protocol gave lower latency at 84 cycles compared to 111 cycles for the baseline token-ring, resulting in approximately 24% latency reduction at saturation PIR.

Network throughput refers to the consistent rate of data delivery within WiNoC, considering a specific injected bandwidth at the network input. Figure 11 presents the variation in network throughput for different injection loads in synthetic traffic scenarios. This comparison involves BMAC and the baseline token ring MAC protocol [41].

The saturation point indicates the peak or maximum achievable throughput. As can be seen in Figure 11(a)-(c), BMAC allows the network to reach a higher peak throughput compared to baseline, except for hotspot traffic as depicted

in Figure 11(d), which gives almost identical throughput. Simulation results show that the proposed BMAC improves network throughput by 61%, 83%, and 36% when compared with the baseline for random, shuffle, and transpose traffic, respectively.

This section has validated the performance of the BMAC scheme using bidirectional links, which enables the token to return to its past immediate radio hub, reducing the full round of maximal token waiting time. Through simulation work, BMAC demonstrated that it can achieve up to 83% network throughput improvement in shuffle traffic conditions with respect to the WiNoC baseline design. BMAC not only provides better performance with higher PIR saturation throughput but is also cost-effective because of the simple BMAC returning back mechanism that consumes negligible area overhead. Furthermore, from the scalability aspect, BMAC is scalable and realistic for large-scale WiNoC, which requires stringent on-chip requirements.

D. RESULTS OF DA+BMAC

In this section, the performance of distance-aware with BMAC protocol called DA+BMAC is evaluated and analyzed against the baseline and BMAC. Figure 12 summarizes the comparisons of latency under different traffic conditions. For all cases, the proposed DA+BMAC performs significantly better than BMAC and the baseline [41]. As can be observed from the figure, the improvement highly depends on the communication patterns. For instance, comparing the results obtained in non-hotspot traffic (random, shuffle, and transpose) with hotspot traffic results in slight PIR improvement as these communication patterns are mostly short-distance communication. In this scenario, most data packet communication traverses through the wired pathway, with less wireless channel utilization.

Specifically, for random traffic, the PIR saturated load of baseline, BMAC, and DA+BMAC are 0.0015, 0.0024, and 0.015 flit/cycle/tile, respectively. For shuffle traffic, the PIR of these three approaches is 0.0016, 0.0029, and 0.0101 flit/cycle/tile. Meanwhile, for transpose traffic, the PIR saturation points are 0.0019, 0.0025, and 0.01 flit/cycle/tile, respectively. The case of hotspot traffic is worth noting, as it causes significant load imbalance within WiNoC. DA+BMAC alleviates this effect and performs slightly better than the baseline and BMAC. In particular, the PIR-saturation for baseline and BMAC is 0.00011 and 0.00012 flit/cycle/tile for DA+BMAC.

Figure 13 shows the impact on network throughput for DA+BMAC, BMAC, and the baseline under synthetic traffic workloads. As shown, the performance gains of the proposed DA+BMAC depend on the traffic pattern of the network. Focusing on Figure 13(a)-(c), DA+BMAC shows significant improvement over the other two networks under random, shuffle, and transpose traffic scenarios. In contrast, as shown in Figure 13(d), DA+BMAC provides only marginal throughput improvement (7.14%) at network saturation in hotspot traffic. This is because this traffic's

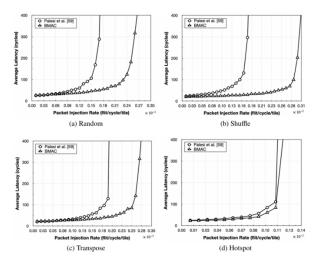


FIGURE 10. Performance impact on latency using BMAC against the baseline design under synthetic traffic (a) Random. (b) Shuffle. (c) Transpose. (d) Hotspot.

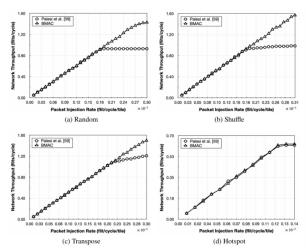


FIGURE 11. Performance impact on network throughput using BMAC against the baseline design under synthetic traffic (a) Random.
(b) Shuffle. (c) Transpose. (d) Hotspot.

communication pattern is concentrated on one specific node that is mostly short-distance, meaning it has only a low probability of utilizing the DA+BMAC scheme.

E. VALIDATION WITH SPLASH-2 AND PARSEC BENCHMARK SUITES

In this section, the performance of the proposed BMAC and DA+BMAC are investigated under realistic application traces using SPLASH-2 [58] and PARSEC [59] benchmark suites. Barnes and Fluidanimate application suites are considered for SPLASH-2 [58] and PARSEC [59] benchmark workloads, respectively.

Figure 14 illustrates the performance impact on latency and network throughput for the proposed BMAC and DA+BMAC when compared with the WiNoC baseline design. In general, the graphs show similar patterns for both benchmark traces but with different PIR saturated load values for BMAC and DA+BMAC



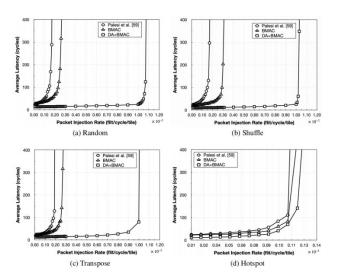


FIGURE 12. Performance impact on latency using DA+BMAC against BMAC and the baseline design under synthetic traffic. (a) Random. (b) Shuffle. (c) Transpose. (d) Hotspot.

improvement. In both benchmark traffic scenarios, the proposed joint-scheme DA+BMAC approach shows an attractively better performance over the baseline WiNoC design and the BMAC protocol on its own. Focusing on Figure 14(a), for Barnes traffic, the PIR saturation load of baseline, BMAC, and DA+BMAC are 0.000024, 0.000038, and 0.00026 flit/cycle/tile, respectively. Meanwhile, in Figure 14(b), the PIR saturation loads are 0.000023, 0.000037, and 0.00026 flit/cycle/tile, respectively, for the Fluidanimate animation application suite.

Figure 15 shows the simulation results of BMAC and DA+BMAC in terms of energy consumption over the baseline architecture under the SPLASH-2 and PARSEC benchmark workloads. As a general observation, BMAC can provide better energy characteristics with its bidirectional MAC approach at the upper layer of the WiNoC architecture.

Additionally, the DA+BMAC approach reveals further improvement in energy profile when the distance-aware routing mechanism is integrated with the BMAC protocol. The detailed analysis of energy saving at the saturated load for the WiNoC system is further quantified in Section IV-G.

F. COMPARISON WITH ADDITIONAL MAC PROTOCOLS

To strengthen our evaluation, we compare DA+BMAC against two additional state-of-the-art MAC protocols: (1) an adaptive CSMA scheme based on [43] and (2) a TDMA approach based on [47]. Figure 16 shows the comparison results in terms of network throughput for random and shuffle traffic patterns.

As shown in Figure 16, DA+BMAC consistently outperforms both comparison protocols, particularly at higher injection rates. For random traffic, DA+BMAC achieves 45% higher throughput than adaptive CSMA and 68% higher than TDMA at the saturation point. For shuffle traffic, the

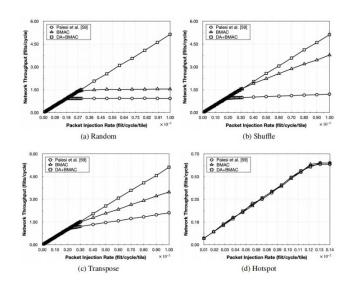


FIGURE 13. Performance impact on network throughput using DA+BMAC against BMAC and the baseline design under synthetic traffic (a) Random. (b) Shuffle. (c) Transpose. (d) Hotspot.

improvements are 38% and 72% over adaptive CSMA and TDMA, respectively.

The superior performance of DA+BMAC can be attributed to two key factors: (1) the bidirectional token movement reduces token waiting time significantly compared to unidirectional token schemes and contention-based approaches, and (2) the distance-aware routing effectively balances the load between wireless and wired networks, preventing congestion on either plane. While adaptive CSMA offers good performance at low injection rates due to its low overhead when contention is minimal, it suffers from increased collisions and backoff delays as network load increases. TDMA provides deterministic performance but lacks the flexibility to adapt to varying traffic patterns, resulting in lower overall utilization of the wireless medium.

G. PERFORMANCE AND ENERGY AT SATURATED LOAD

In this section, we present the network performance characteristics and energy consumption at the saturated load of the WiNoC when incorporating BMAC and DA+BMAC strategies. Moreover, the trade-off analysis between performance, energy, and resources is also discussed.

1) PERFORMANCE AT SATURATED LOAD

In this subsection, we evaluate the performance of WiNoC at the saturation load for baseline, BMAC, and DA+BMAC architectures. Figure 17 shows the normalized network throughput of the baseline, BMAC, and DA+BMAC schemes under synthetic (random, shuffle, transpose, and hotspot) and real-application (Barnes and Fluidanimate) benchmark traffic. Under both traffic patterns, it can be observed that, except for hotspot traffic, all workload scenarios reveal that BMAC introduces some throughput improvement over the baseline architecture. Meanwhile, with

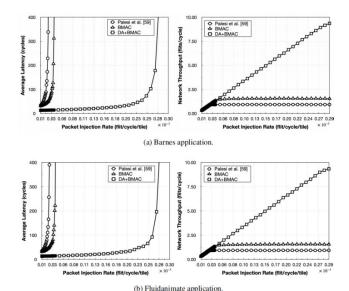


FIGURE 14. Performance impact on latency and network throughput under the SPLASH-2 and PARSEC benchmark traces. (a) Barnes application. (b) Fluidanimate application.

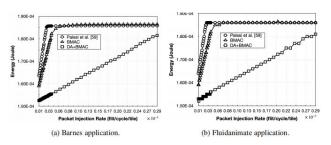


FIGURE 15. Energy consumption under the SPLASH-2 and PARSEC benchmark traces. (a) Barnes application. (b) Fluidanimate application.

the DA+BMAC approach, the gain in network throughput at the saturated load is substantially higher.

To further evaluate the performance of the proposed BMAC and DA+BMAC, the speedup in terms of network throughput against the baseline has been obtained. Figure 18 shows the network throughput speedup for synthetic traffic, Barnes, and Fluidanimate benchmark traffic. In all cases, except for hotspot traffic, the proposed BMAC design speedup is higher than the baseline mesh-WiNoC architecture. This is because the communication pattern in hotspot traffic is mostly short-distance, concentrating on one particular processing core that does not favor the proposed BMAC protocol. Interestingly, the proposed joint-approach DA+BMAC provides an apparently better speedup than BMAC and the baseline design. The throughput speedup can be improved up to 11.49× for synthetic random traffic, $10.85 \times$ for the Barnes application, and $11.37 \times$ for the Fluidanimate workload.

2) ENERGY CONSUMPTION AT SATURATED LOAD

This subsection evaluates the proposed designs of BMAC and DA+BMAC in terms of energy consumption at the

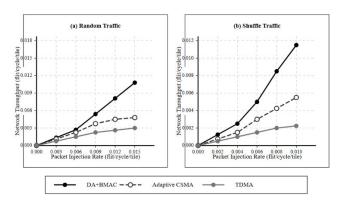


FIGURE 16. Normalized network throughput comparison for the baseline, BMAC, and DA+BMAC designs in the mesh-WiNoC architecture under synthetic, Barnes, and Fluidanimate traffic workloads.

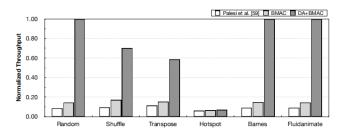


FIGURE 17. Normalized network throughput comparison for the baseline, BMAC, and DA+BMAC designs in the mesh-WiNoC architecture under synthetic, Barnes, and Fluidanimate traffic workloads.

saturated load for mesh-WiNoC architecture. Consequently, the percentage of energy savings is analyzed to investigate the energy characteristics of the proposed BMAC and DA+BMAC approaches. Figure 19 summarizes the normalized energy consumption under synthetic (random, shuffle, transpose, and hotspot) and SPLASH-2/PARSEC realistic application (Barnes and Fluidanimate) workloads. For all traffic workloads, the proposed BMAC protocol provides some energy reduction with respect to the baseline design. Furthermore, the energy reduction is more pronounced for the DA+BMAC joint-scheme, confirming that this approach is energy-friendly for the investigated mesh-WiNoC interconnects.

Energy saving is equally important as the number of cores grows in WiNoC because it implies an increment in traffic workload intensity [9]. Figure 20 shows the percentage of energy savings comparison for the proposed BMAC and DA+BMAC approaches in the mesh-WiNoC architecture under synthetic (random, shuffle, transpose, and hotspot), SPLASH-2 (Barnes), and PARSEC (Fluidanimate) application workloads. For shuffle synthetic traffic distribution, up to 8.33% and 15.00% of energy savings can be obtained when BMAC and DA+BMAC are utilized, respectively. Furthermore, for SPLASH-2 Barnes application traces, the proposed BMAC and DA+BMAC schemes can achieve up to 5.29% and 14.71% energy savings, respectively. Finally, up to 5.50% and 13.97% of energy can be saved for BMAC



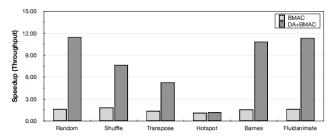


FIGURE 18. Performance speedup (throughput) comparison for the baseline, BMAC, and DA+BMAC designs in the mesh-WiNoC architecture under synthetic, Barnes, and Fluidanimate traffic workloads.

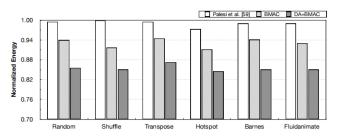


FIGURE 19. Normalized energy consumption comparison for the baseline, BMAC, and DA+BMAC designs in the mesh-WiNoC architecture under synthetic, Barnes, and Fluidanimate traffic workloads.

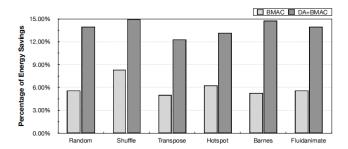


FIGURE 20. Percentage of energy savings comparison for the proposed BMAC and DA+BMAC designs in the mesh-WiNoC architecture under synthetic, Barnes, and Fluidanimate traffic workloads.

and DA+BMAC, respectively, under the Fluidanimate PAR-SEC benchmark traces, showing that the proposed BMAC and DA+BMAC approaches are also energy-friendly for the mesh-WiNoC architecture.

H. AREA AND TIMING OVERHEAD ANALYSIS

We synthesized the DA+BMAC components using Synopsys Design Compiler with an advanced node PDK to evaluate the hardware overhead. Table 3 summarizes the area and timing results for the key components.

The BMAC controller requires 623 logic gates, adding only 3.38% area overhead to the baseline router. The direction control logic consumes the majority of these gates (58%) while the neighbor awareness module and token state machine account for 25% and 17%, respectively. The DA logic requires an additional 212 gates, primarily for the Manhattan distance calculation and threshold comparison logic.

TABLE 3. Area and timing overhead analysis.

Component	Gate Count	Area (μm²)	Critical Path Delay (ps)	Power (mW)
Baseline Router	18,450	4,350	380	8.75
BMAC Controller	623	142	95	0.45
DA Logic	212	52	85	0.18
DA+BMAC Router	19,285	4,544	392	9.38
Overhead	4.53%	4.46%	3.16%	7.20%

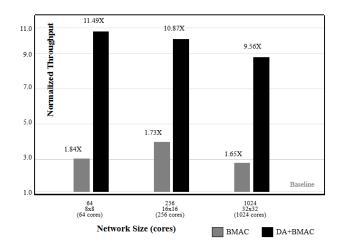


FIGURE 21. Scalability analysis showing normalized throughput of DA+BMAC compared to baseline across different network sizes under random traffic.

The critical path delay increased by only 3.16% (12ps) compared to the baseline router, which is negligible in the context of a 1GHz clock (1000ps period). This confirms our analysis that the DA mechanism does not introduce significant timing penalties, as most operations can be performed in parallel with existing router pipeline stages. DA+BMAC scales effectively to support thousands of processing cores while maintaining stringent on-chip design requirements, making it suitable for future many-core system implementations.

Power consumption increased by 7.20%, slightly higher than the area overhead due to the additional activity in the BMAC controller for token direction management. However, this localized power increase is more than offset by the system-level energy savings of up to 15% demonstrated in our experiments.

I. SCALABILITY ANALYSIS

To evaluate the scalability of DA+BMAC, we extended our simulations to larger network sizes: 16×16 (256 cores) and 32×32 (1024 cores). For each configuration, we maintained the same radio hub to core ratio (1:4) and adjusted the optimal threshold distance according to our derived formula $(T_{optimal} = \sqrt{N}/4)$.

Figure 21 shows the normalized throughput improvement of DA+BMAC over the baseline for different network sizes under random traffic pattern. The throughput gain remains consistent (within 15% variation) across all three network



TABLE 4. Scalability analysis for different network sizes.

Network Size	Cores	Optimal Threshold	Throughput Improvement	Energy Saving
8×8	64	5 hops	11.49×	15.00%
16×16	256	8 hops	10.87×	14.25%
32×32	1024	16 hops	9.56×	13.78%

sizes, confirming that our approach scales effectively to larger networks. Table 4 presents the optimal threshold distances and the corresponding network performance metrics for different network sizes. As the network size increases, we observe a slight decrease in both throughput improvement and energy savings. This trend can be attributed to two factors: (1) increased network diameter leading to higher average token acquisition times, and (2) higher contention for wireless channels in larger networks. However, even at 1024 cores, DA+BMAC still achieves impressive throughput improvement $(9.56\times)$ and energy savings (13.78%), demonstrating its effectiveness for future many-core systems.

The token reversal frequency analysis shows that in the 1024-core configuration, token reversal occurs approximately 22% less frequently than in the 64-core network. This reduction is expected as the token ring becomes larger, making immediate neighbors less likely to have pending requests simultaneously. Nevertheless, the bidirectional capability continues to provide significant benefit even at larger scales.

J. DISCUSSION

There are still important design challenges with conventional NoC, such as high latency and power consumption caused by long-distance multi-hop communication among processing cores [19], [22], [60], [61]. Motivated by the unique capabilities of single-hop wireless interconnects, WiNoC is a viable solution as a complement to conventional NoC to alleviate long-distance communication. However, in WiNoC architecture, wireless channel bandwidth capacity is limited and needs to be shared with multiple radio hubs, which led to the DA+BMAC designs proposed in this research.

Several WiNoC proposals have been presented with various topological structures roughly classified into regular [21], [26], [38], [40], [42], [62], [63] and irregular [33], [36], [37], [39], [41], [64] architectures with numerous processing cores, ranging from 54–1024 cores [24], [26], [33], [36], [37], [65], [66]. Depending on the proposed WiNoC structure, there are also various numbers of radio hubs, varying from 4–256 subnets integrated into the proposed WiNoC structure [21], [25], [37], [38], [39], [65], [67]. Furthermore, these WiNoC designs are implemented with single- to multi-channel wireless configurations depending on the adopted MAC protocol and wireless frequencies.

For the scope of work, this research uses a regular mesh topology with 64 cores, 16 radio hubs, and single-channel wireless communication as its WiNoC structure for evaluating the proposed BMAC and DA+BMAC using the Noxim

NoC simulator. However, these designs are general and can be implemented on a larger scale and with any topological structure of WiNoC architecture. Because there are no existing works that use a similar WiNoC structure and configuration as in this study, due to the variety of network sizes, number of radio hub subnets, and implementation of multiple wireless channels [24], [46], [65], [66], [68], [69], the performance of DA+BMAC is compared to the WiNoC token-based baseline design for a fair comparison. Moreover, the existing proposed WiNoC designs were evaluated with different tools, including Phoenixsim [71], Booksim [72], Multi2sim [73], Omnet++ [74], Garnet [75], Orion 2.0 [76], and researchers' own custom-made in-house NoC simulators.

DA+BMAC integrates the BMAC protocol with the DA routing mechanism to take full advantage of single-hop wireless capabilities for an optimal proportion of wired-wireless communication in WiNoC. To reduce the full round of daisy-chained maximal token waiting time at the upper layer of WiNoC, the BMAC approach uses bidirectional links to allow the token to turn to its adjacent passed immediate radio hub. Additionally, at the lower layer of WiNoC, the DA routing scheme uses a distance-based traffic steering technique to balance network bandwidth between wired and wireless channels to improve WiNoC performance while providing energy savings.

This proposed DA+BMAC has been evaluated with extensive simulation work, considering both synthetic traffic and benchmark traces to quantify the potential improvement of this approach. Experimental work reveals attractive results with up to 11.49× throughput improvement and 15.00% energy savings with respect to the WiNoC token-based baseline design, confirming the effectiveness of this approach. Through simulation results, DA+BMAC demonstrated that WiNoC performance and energy profile are improved even in the presence of application-specific PARSEC [59] and SPLASH-2 [58] benchmark traffic workloads. DA+BMAC improves the MAC protocol and routing mechanism in WiNoC architecture, resulting in improved network performance and energy characteristics.

Compared with other existing WiNoC works, which mostly use channelization protocols [25], [46], [63], [65], [66], [67], [69], [77], apart from its collision-free protocol, the main advantage of this DA+BMAC proposal is based on its low-complexity radio hub transceiver design and network bandwidth balancing routing mechanism. Furthermore, DA+BMAC bridges the gap for research investigations with the bidirectional token-based MAC technique, particularly in the regular mesh-topology WiNoC architecture, in comparison with other existing related works that use similar token-based techniques, which are mostly implemented in various topologies such as SWNoC [26], [33], [46], [64], honeycomb [36], [37], delta multistage [36], or mesh-oftree [36]. Due to its design simplicity, DA+BMAC is also scalable and suitable for WiNoC architecture, which demands stringent on-chip design requirements and is envisaged to cater to thousands of processing cores [65], [78], [79].



The proposed distance-aware routing mechanism determines packet transmission paths based on Manhattan distance calculations between source-destination processing cores. While our bidirectional approach significantly reduces average token acquisition time from O(N) to O(N/2) in optimal scenarios (where N represents the number of radio hubs), the relationship between token circulation patterns and overall network latency under varying traffic loads requires deeper investigation.

V. CONCLUSION

This paper proposes DA+BMAC, the distance-aware bidirectional medium access control for mesh-WiNoC architecture. This research endeavor enhances the routing and MAC protocols for WiNoC by controlling the workload between wired and wireless channels based on communication distance. It also improves token access with bidirectional MAC to reduce the maximum token waiting time. The proposed design not only improves WiNoC performance but also saves energy over the baseline architecture.

The BMAC approach for mesh-WiNoC architecture uses bidirectional links to allow the token to serve its past immediate radio hub. This technique improves token distribution by preventing the worst-case full-trip token waiting time. The BMAC technique demonstrates up to 1.84× throughput improvement and 8.33% energy savings compared to the baseline WiNoC architecture.

This research also proposed a distance-aware routing algorithm to complement BMAC for mesh-WiNoC architecture. DA+BMAC effectively controls packet transmission between wired and wireless communication based on a certain distance between source and destination. Because the aggregated bandwidth for wireless is much less than wired NoC, long-distance communication is performed with single-hop wireless channels. In contrast, wired channels are used for short-distance communication as they have far greater aggregated bandwidth. Over the baseline WiNoC architecture, DA+BMAC improves throughput by up to 11.49× and saves 15.00% energy.

In this paper, DA+BMAC techniques are presented for improving the performance and energy consumption of mesh-WiNoC architecture. This proposed work is general and can be applied to any WiNoC topology. Future investigations should explore adaptive token circulation policies that dynamically adjust based on traffic characteristics, priority-based token allocation schemes for real-time applications, and multi-token protocols for enhanced parallelism in large-scale networks. These enhancements would significantly strengthen the practical deployment viability and reliability of DA+BMAC in many-core systems. Another interesting exploration would be to extend the investigation to other types of topologies such as small-world [21], [33], [64], [80] or honeycomb [36], [37] topologies as future work. Our scalability analysis has validated the architecture's effectiveness for larger network sizes including 256 and 1024 processing cores, confirming its suitability for future many-core systems.

REFERENCES

- [1] W.-K. Chen, *Linear Networks and Systems*. Belmont, CA, USA: Wadsworth, 1993, pp. 123–135.
- [2] J. U. Duncombe, "Infrared navigation—Part I: An assessment of feasibility," *IEEE Trans. Electron Devices*, vol. ED-11, no. 1, pp. 34–39, Jan. 1959.
- [3] E. P. Wigner, "Theory of traveling-wave optical laser," *Phys. Rev.*, vol. 134, pp. A635–A646, Dec. 1965.
- [4] H. Kurss and W. Kahn, "A note on reflector arrays," *IEEE Trans. Antennas Propag.*, vol. AP-15, no. 5, pp. 692–693, Sep. 1967.
- [5] E. E. Reber, R. L. Michell, and C. J. Carter, "Oxygen absorption in the Earth's atmosphere," Aerospace Corp., Los Angeles, CA, USA, Tech. Rep. TR-0200 (4230-46)-3, Nov. 1988.
- [6] J. H. Davis and J. R. Cogdell, "Calibration program for the 16-foot antenna," Elect. Eng. Res. Lab., Univ. Texas, Austin, TX, USA, Tech. Rep. Memo. NGL-006-69-3, Nov. 1987.
- [7] Transmission Systems for Communications, 3rd ed., Western Electric Co., Winston-Salem, NC, USA, 1985, pp. 44–60.
- [8] S. Kumar, A. Jantsch, J.-P. Soininen, M. Forsell, M. Millberg, J. Oberg, K. Tiensyrja, and A. Hemani, "A network on chip architecture and design methodology," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI. New Paradigms VLSI Syst. Design. (ISVLSI)*, Pittsburgh, PA, USA, Apr. 2002, pp. 117–124, doi: 10.1109/ISVLSI.2002.1016885.
- [9] J. Turner, "New directions in communications (or which way to the information age?" *IEEE Commun. Mag.*, vol. COM-24, no. 10, pp. 8–15, Oct. 1986, doi: 10.1109/MCOM.1986.1092946.
- [10] W. P. Risk, G. S. Kino, and H. J. Shaw, "Fiber-optic frequency shifter using a surface acoustic wave incident at an oblique angle," *Opt. Lett.*, vol. 11, no. 2, pp. 115–117, Feb. 1986, doi: 10.1364/ol.11.000115.
- [11] P. Kopyt, B. Salski, P. Zagrajek, D. Janczak, M. Sloma, M. Jakubowska, M. Olszewska-Placha, and W. Gwarek, "Electric properties of graphene-based conductive layers from DC up to terahertz range," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 3, pp. 480–490, May 2016, doi: 10.1109/TTHZ.2016.2544142.
- [12] D. Vantrease, R. Schreiber, M. Monchiero, M. McLaren, N. P. Jouppi, M. Fiorentino, A. Davis, N. Binkert, R. G. Beausoleil, and J. H. Ahn, "Corona: System implications of emerging nanophotonic technology," in *Proc. Int. Symp. Comput. Archit.*, Beijing, China, Jun. 2008, pp. 153–164, doi: 10.1109/isca.2008.35.
- [13] B. S. Feero and P. P. Pande, "Networks-on-chip in a three-dimensional environment: A performance evaluation," *IEEE Trans. Comput.*, vol. 58, no. 1, pp. 32–45, Jan. 2009, doi: 10.1109/TC.2008.142.
- [14] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, V. Narayanan, and M. Kandemir, "Design and management of 3D chip multiprocessors using network-in-memory," ACM SIGARCH Comput. Archit. News, vol. 34, no. 2, pp. 130–141, May 2006, doi: 10.1145/1150019.1136497.
- [15] V. F. Pavlidis and E. G. Friedman, "3-D topologies for networks-onchip," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 10, pp. 1081–1090, Oct. 2007, doi: 10.1109/TVLSI.2007.893649.
- [16] M. F. Chang, V. P. Roychowdhury, L. Zhang, H. Shin, and Y. Qian, "RF/wireless interconnect for inter- and intra-chip communications," *Proc. IEEE*, vol. 89, no. 4, pp. 456–466, Apr. 2001, doi: 10.1109/5.920578.
- [17] B. A. Floyd, C.-M. Hung, and K. K. O, "Intra-chip wireless interconnect for clock distribution implemented with integrated antennas, receivers, and transmitters," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 543–552, May 2002, doi: 10.1109/4.997846.
- [18] A. Karkar, T. Mak, K.-F. Tong, and A. Yakovlev, "A survey of emerging interconnects for on-chip efficient multicast and broadcast in many-cores," *IEEE Circuits Syst. Mag.*, vol. 16, no. 1, pp. 58–72, 1st Quart., 2016, doi: 10.1109/MCAS.2015.2510199.
- [19] A. Ganguly, K. Chang, S. Deb, P. P. Pande, B. Belzer, and C. Teuscher, "Scalable hybrid wireless network-on-chip architectures for multicore systems," *IEEE Trans. Comput.*, vol. 60, no. 10, pp. 1485–1502, Oct. 2011, doi: 10.1109/TC.2010.176.
- [20] S. Deb, K. Chang, A. Ganguly, X. Yu, C. Teuscher, P. Pande, D. Heo, and B. Belzer, "Design of an efficient NoC architecture using millimeter-wave wireless links," in *Proc. 13th Int. Symp. Quality Electron. Design (ISQED)*, San Jose, CA, USA, Mar. 2012, pp. 165–170, doi: 10.1109/ISQED.2012.6187490.



- [21] D. DiTomaso, A. Kodi, S. Kaya, and D. Matolak, "IWISE: Inter-router wireless scalable express channels for network-on-chips (NoCs) architecture," in *Proc. IEEE 19th Annu. Symp. High Perform. Interconnects*, Santa Clara, CA, USA, Aug. 2011, pp. 11–18, doi: 10.1109/HOTI.2011.12.
- [22] Y. P. Zhang, Z. M. Chen, and M. Sun, "Propagation mechanisms of radio waves over intra-chip channels with integrated antennas: Frequency-domain measurements and time-domain analysis," *IEEE Trans. Antennas Propag.*, vol. 55, no. 10, pp. 2900–2906, Oct. 2007, doi: 10.1109/TAP.2007.905867.
- [23] S. Abadal, B. Sheinman, O. Katz, O. Markish, D. Elad, Y. Fournier, D. Roca, M. Hanzich, G. Houzeaux, M. Nemirovsky, E. Alarcón, and A. Cabellos-Aparicio, "Broadcast-enabled massive multicore architectures: A wireless RF approach," *IEEE Micro*, vol. 35, no. 5, pp. 52–61, Sep. 2015, doi: 10.1109/MM.2015.123.
- [24] A. Kodi, A. Louri, and J. Wang, "Design of energy-efficient channel buffers with router bypassing for network-on-chips (NoCs)," in *Proc. Int. Symp. Quality Electron. Design*, Mar. 2009, pp. 826–832, doi: 10.1109/ISQED.2009.4810399.
- [25] M. S. Shamim, N. Mansoor, R. S. Narde, V. Kothandapani, A. Ganguly, and J. Venkataraman, "A wireless interconnection framework for seamless inter and intra-chip communication in multichip systems," *IEEE Trans. Comput.*, vol. 66, no. 3, pp. 389–402, Mar. 2017, doi: 10.1109/TC.2016.2605093.
- [26] S. Deb, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, "Wireless NoC as interconnection backbone for multicore chips: Promises and challenges," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 2, no. 2, pp. 228–239, Jun. 2012, doi: 10.1109/JETCAS.2012.2193835.
- [27] X. Yu, S. P. Sah, H. Rashtian, S. Mirabbasi, P. P. Pande, and D. Heo, "A 1.2-pJ/bit 16-Gb/s 60-GHz OOK transmitter in 65-nm CMOS for wireless network-on-chip," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2357–2369, Oct. 2014, doi: 10.1109/TMTT.2014.2347919.
- [28] X. Yu, H. Rashtian, S. Mirabbasi, P. P. Pande, and D. Heo, "An 18.7-Gb/s 60-GHz OOK demodulator in 65-nm CMOS for wireless network-on-chip," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 799–806, Mar. 2015, doi: 10.1109/TCSI.2014.2386751.
- [29] K. Kim and K. K. O, "Characteristics of integrated dipole antennas on bulk, SOI, and SOS substrates for wireless communication," in *Proc. IEEE Int. Interconnect Technol. Conf.*, San Francisco, CA, USA, Jun. 1998, pp. 21–23, doi: 10.1109/IITC.1998.704741.
- [30] S. R. Govindarajulu, R. Hokayem, and E. A. Alwan, "A 60 GHz millimeter-wave antenna array for 3D antenna-in-package applications," *IEEE Access*, vol. 9, pp. 143307–143314, 2021, doi: 10.1109/ACCESS.2021.3121320.
- [31] J.-J. Lin, H.-T. Wu, Y. Su, L. Gao, A. Sugavanam, and J. E. Brewer, "Communication using antennas fabricated in silicon integrated circuits," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1678–1687, Aug. 2007, doi: 10.1109/JSSC.2007.900236.
- [32] D. Zhao and Y. Wang, "SD-MAC: Design and synthesis of a hardware-efficient collision-free QoS-aware MAC protocol for wireless network-on-chip," *IEEE Trans. Comput.*, vol. 57, no. 9, pp. 1230–1245, Sep. 2008, doi: 10.1109/TC.2008.86.
- [33] S. Deb, K. Chang, X. Yu, S. P. Sah, M. Cosic, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, "Design of an energy-efficient CMOS-compatible NoC architecture with millimeter-wave wireless interconnects," *IEEE Trans. Comput.*, vol. 62, no. 12, pp. 2382–2396, Dec. 2013, doi: 10.1109/TC.2012.224.
- [34] M. O. Agyeman, Q.-T. Vien, A. Ahmadinia, A. Yakovlev, K.-F. Tong, and T. Mak, "A resilient 2-D waveguide communication fabric for hybrid wired-wireless NoC design," *IEEE Trans. Parallel Distrib. Syst.*, vol. 28, no. 2, pp. 359–373, Feb. 2017, doi: 10.1109/TPDS.2016.2575836.
- [35] W. Bux, "Token-ring local-area networks and their performance," *Proc. IEEE*, vol. 77, no. 2, pp. 238–256, Feb. 1989, doi: 10.1109/5.18625.
- [36] A. Karkar, R. Al-Dujaily, A. Yakovlev, K. Tong, and T. Mak, "Surface wave communication system for on-chip and off-chip interconnects," in *Proc. 5th Int. Workshop Netw. Chip Archit.*, Porto Alegre, Brazil, Dec. 2012, pp. 11–16.
- [37] R. Afsharmazayejani, F. Yazdanpanah, A. Rezaei, M. Alaei, and M. Daneshtalab, "HoneyWiN: Novel honeycomb-based wireless NoC architecture in many-core era," in *Proc. Int. Symp. Appl. Reconfigurable Comput.*, Santorini, Greece, 2018, pp. 304–316.
- [38] D. DiTomaso, A. Kodi, D. Matolak, S. Kaya, S. Laha, and W. Rayess, "A-WiNoC: Adaptive wireless network-on-chip architecture for chip multiprocessors," *IEEE Trans. Parallel Distrib. Syst.*, vol. 26, no. 12, pp. 3289–3302, Dec. 2015, doi: 10.1109/TPDS.2014.2383384.

- [39] V. Vijayakumaran, M. P. Yuvaraj, N. Mansoor, N. Nerurkar, A. Ganguly, and A. Kwasinski, "CDMA enabled wireless network-on-chip," ACM J. Emerg. Technol. Comput. Syst., vol. 10, no. 4, pp. 1–20, Jun. 2014, doi: 10.1145/2536778.
- [40] H. K. Mondal, S. H. Gade, M. S. Shamim, S. Deb, and A. Ganguly, "Interference-aware wireless network-on-chip architecture using directional antennas," *IEEE Trans. Multi-Scale Comput. Syst.*, vol. 3, no. 3, pp. 193–205, Jul. 2017, doi: 10.1109/TMSCS.2016.2595527.
- [41] M. Palesi, M. Collotta, A. Mineo, and V. Catania, "An efficient radio access control mechanism for wireless network-on-chip architectures," *J. Low Power Electron. Appl.*, vol. 5, no. 2, pp. 38–56, Mar. 2015, doi: 10.3390/jlpea5020038.
- [42] G. Piro, S. Abadal, A. Mestres, E. Alarcón, J. Solé-Pareta, L. A. Grieco, and G. Boggia, "Initial MAC exploration for graphene-enabled wireless networks-on-chip," in *Proc. Int. Conf. Nanoscale Comput. Commun.*, Boston, MA, USA, Sep. 2014, p. 7, doi: 10.1145/2619955. 2619963.
- [43] A. Mestres, S. Abadal, J. Torrellas, E. Alarcón, and A. Cabellos-Aparicio, "A MAC protocol for reliable broadcast communications in wireless network-on-chip," in *Proc. Int. Workshop Netw. Chip Archit.*, China, Dec. 2016, pp. 21–26, doi: 10.1145/2994133.2994137.
- [44] L. Kleinrock and F. Tobagi, "Packet switching in radio channels: Part I-carrier sense multiple-access modes and their throughput-delay characteristics," *IEEE Trans. Commun.*, vol. COM-23, no. 12, pp. 1400–1416, Dec. 1975, doi: 10.1109/TCOM.1975.1092768.
- [45] R. Binder, N. Abramson, F. Kuo, A. Okinaka, and D. Wax, "ALOHA packet broadcasting: A retrospect," in *Proc. May Nat. Comput. Conf. Expo. (AFIPS)*, May 1975, pp. 203–215, doi: 10.1145/1499949.1499985.
- [46] A. Ganguly, K. Chang, P. P. Pande, B. Belzer, and A. Nojeh, "Performance evaluation of wireless networks on chip architectures," in *Proc. 10th Int. Symp. Quality Electron. Design*, San Jose, CA, USA, Mar. 2009, pp. 350–355, doi: 10.1109/ISQED.2009.4810319.
- [47] L. G. G. Morales, J. E. A. Cobo, and N. Bagherzadeh, "A new approach to the population-based incremental learning algorithm using virtual regions for task mapping on NoCs," *J. Syst. Archit.*, vol. 97, pp. 443–454, Aug. 2019, doi: 10.1016/j.sysarc.2019.01.013.
- [48] N. Mansoor and A. Ganguly, "Reconfigurable wireless network-onchip with a dynamic medium access mechanism," in *Proc. 9th Int. Symp. Netw. Chip*, Vancouver, BC, Canada, Sep. 2015, pp. 1–8, doi: 10.1145/2786572.2788711.
- [49] J. L. Abellán, A. K. Deb, and A. Ganguly, "Replica: A wireless manycore for communication intensive and approximate data," *Comput. Archit. Lett.*, vol. 17, no. 2, pp. 197–200, Jul. 2018, doi: 10.1145/3297858.3304033.
- [50] D. Zhao, Y. Wang, J. Li, and T. Kikkawa, "Design of multi-channel wireless NoC to improve on-chip communication capacity," in *Proc. Int. Symp. Netw. Chip*, Pittsburgh, PA, USA, May 2011, pp. 177–184, doi: 10.1145/1999946.1999975.
- [51] M. S. Shamim, N. Mansoor, A. Samaiyar, A. Ganguly, S. Deb, and S. S. Ram, "Energy-efficient wireless network-on-chip architecture with log-periodic on-chip antennas," in *Proc. 24th, Ed., Great Lakes Symp. (VLSI)*, Knoxville, TN, USA, May 2014, pp. 85–86, doi: 10.1145/2591513.2591566.
- [52] X. Meng, B. Chi, and Z. Wang, "A 152-GHz OOK transmitter with 3-dBm output power in 65-nm CMOS," *IEEE Microw. Wire-less Compon. Lett.*, vol. 27, no. 8, pp. 748–750, Aug. 2017, doi: 10.1109/LMWC.2017.2723722.
- [53] A. B. Kahng, B. Lin, and S. Nath, "ORION3.0: A comprehensive NoC router estimation tool," *IEEE Embedded Syst. Lett.*, vol. 7, no. 2, pp. 41–45, Jun. 2015, doi: 10.1109/LES.2015.2402197.
- [54] W. Amin, F. Hussain, S. Anjum, S. Khan, N. K. Baloch, Z. Nain, and S. W. Kim, "Performance evaluation of application mapping approaches for network-on-chip designs," *IEEE Access*, vol. 8, pp. 63607–63631, 2020, doi: 10.1109/ACCESS.2020. 2982675.
- [55] L. P. Carloni, P. Pande, and Y. Xie, "Networks-on-chip in emerging interconnect paradigms: Advantages and challenges," in *Proc. 3rd ACM/IEEE Int. Symp. Netw. Chip*, La Jolla, CA, USA, May 2009, pp. 93–102, doi: 10.1109/NOCS.2009.5071456.
- [56] V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti, "Noxim: An open, extensible and cycle-accurate network on chip simulator," in *Proc. IEEE 26th Int. Conf. Appl.-Specific Syst., Archit. Processors (ASAP)*, Toronto, ON, Canada, Jul. 2015, pp. 162–163, doi: 10.1109/ASAP.2015.7245728.



- [57] C. Wang, W.-H. Hu, and N. Bagherzadeh, "A wireless network-on-chip design for multicore platforms," in *Proc. 19th Int. Euromicro Conf. Par*allel, Distrib. Network-Based Process., Ayia Napa, Cyprus, Feb. 2011, pp. 409–416, doi: 10.1109/PDP.2011.37.
- [58] S. C. Woo, M. Ohara, E. Torrie, J. P. Singh, and A. Gupta, "The SPLASH-2 programs: Characterization and methodological considerations," in *Proc. Int. Symp. Comput. Archit.*, Santa Margherita Ligure, Italy, Jun. 1995, pp. 24–36, doi: 10.1109/ISCA.1995.524546.
- [59] C. Bienia, S. Kumar, J. P. Singh, and K. Li, "The PARSEC benchmark suite: Characterization and architectural implications," in *Proc. Int. Conf. Parallel Archit. Compilation Techn.*, Toronto, ON, Canada, 2008, pp. 72–81.
- [60] X. Yu, J. Baylon, P. Wettin, D. Heo, P. P. Pande, and S. Mirabbasi, "Architecture and design of multichannel millimeter-wave wireless NoC," *IEEE Des. Test*, vol. 31, no. 6, pp. 19–28, Dec. 2014, doi: 10.1109/MDAT.2014.2322995.
- [61] S. Abadal, J. Torrellas, E. Alarcón, and A. Cabellos-Aparicio, "OrthoNoC: A broadcast-oriented dual-plane wireless network-on-chip architecture," *IEEE Trans. Parallel Distrib. Syst.*, vol. 29, no. 3, pp. 628–641, Mar. 2018, doi: 10.1109/TPDS.2017.2764901.
- [62] S. B. Lee, S. W. Tam, I. Pefkianakis, S. Lu, M. F. Chang, C. Guo, G. Reinman, C. Peng, M. Naik, L. Zhang, and J. Cong, "A scalable micro wireless interconnect structure for CMPs," in *Proc. Int. Conf. Mobile Comput. Netw.*, Beijing, China, Sep. 2009, pp. 217–228, doi: 10.1145/1614320.1614345.
- [63] K. Chang, S. Deb, A. Ganguly, X. Yu, S. P. Sah, P. P. Pande, B. Belzer, and D. Heo, "Performance evaluation and design trade-offs for wireless network-on-chip architectures," ACM J. Emerg. Technol. Comput. Syst., vol. 8, no. 3, pp. 1–25, Aug. 2012, doi: 10.1145/2287696.2287706.
- [64] M. O. Agyeman, A. Ahmadinia, and A. Shahrabi, "Heterogeneous 3D network-on-chip architectures: Area and power aware design techniques," J. Circuits, Syst. Comput., vol. 22, no. 4, Apr. 2013, Art. no. 1350016, doi: 10.1142/s0218126613500163.
- [65] T. Majumder, P. P. Pande, and A. Kalyanaraman, "Wireless NoC platforms with dynamic task allocation for maximum likelihood phylogeny reconstruction," *IEEE Design Test*, vol. 31, no. 3, pp. 54–64, Jun. 2014, doi: 10.1109/MDAT.2013.2288778.
- [66] N. Mansoor, S. Shamim, and A. Ganguly, "A demand-aware predictive dynamic bandwidth allocation mechanism for wireless network-on-chip," in *Proc. ACM/IEEE Int. Workshop Syst. Level Interconnect Predict. (SLIP)*, Austin, TX, USA, Jun. 2016, pp. 1–8, doi: 10.1145/2947357.2947361.
- [67] H. I. Gaha and M. Balti, "Novel bi-UWB on-chip antenna for wireless NoC," *Micromachines*, vol. 13, no. 2, p. 231, Jan. 2022, doi: 10.3390/mi13020231.
- [68] Z. Qian, P. Bogdan, G. Wei, C.-Y. Tsui, and R. Marculescu, "A traffic-aware adaptive routing algorithm on a highly reconfigurable network-on-chip architecture," in *Proc. 8th IEEE/ACM/IFIP Int. Conf. Hardw./Softw. Codesign Syst. Synth.*, Tampere, Finland, Oct. 2012, pp. 161–170, doi: 10.1145/2380445.2380475.
- [69] M. M. Rahaman, P. Ghosal, and C. Giri, "WiZ-BMS: A hybrid wireless network-on-chip design with fully adaptive routing," in *Proc. IEEE Int. Symp. Smart Electron. Syst. (iSES)*, Warangal, India, Dec. 2022, pp. 242–247, doi: 10.1109/iSES54909.2022.00056.
- [70] A. Rezaei, M. Daneshtalab, M. Palesi, and D. Zhao, "Efficient congestion-aware scheme for wireless on-chip networks," in *Proc. 24th Euromicro Int. Conf. Parallel, Distrib., Netw.-Based Process. (PDP)*, Heraklion, Greece, Feb. 2016, pp. 742–749, doi: 10.1109/PDP.2016.88.
- [71] J. Chan, G. Hendry, A. Biberman, K. Bergman, and L. P. Carloni, "PhoenixSim: A simulator for physical-layer analysis of chip-scale photonic interconnection networks," in *Proc. Design, Automation Test Eur. Conf. Exhib.*, Dresden, Germany, Mar. 2010, pp. 691–696, doi: 10.1109/DATE.2010.5457114.
- [72] N. Jiang, D. U. Becker, G. Michelogiannakis, J. Balfour, B. Towles, D. E. Shaw, J. Kim, and W. J. Dally, "A detailed and flexible cycleaccurate network-on-chip simulator," in *Proc. IEEE Int. Symp. Per*form. Anal. Syst. Softw., Austin, TX, USA, Apr. 2013, pp. 86–96, doi: 10.1109/ISPASS.2013.6557149.
- [73] R. Ubal, B. Jang, P. Mistry, D. Schaa, and D. Kaeli, "Multi2Sim: A simulation framework for CPU-GPU computing," in *Proc. 21st Int. Conf. Parallel Architectures Compilation Techn. (PACT)*, Sep. 2012, pp. 335–344.
- [74] A. Varga and R. Hornig, "An overview of the OMNeT++ simulation environment," in *Proc. 1st Int. ICST Conf. Simulation Tools Techn. Commun. Netw. Syst.*, Marseille, France, Mar. 2008, p. 60.

- [75] N. Agarwal, T. Krishna, L.-S. Peh, and N. K. Jha, "GARNET: A detailed on-chip network model inside a full-system simulator," in *Proc. IEEE Int. Symp. Perform. Anal. Syst. Softw.*, Boston, MA, USA, Apr. 2009, pp. 33–42, doi: 10.1109/ISPASS.2009.4919636.
- [76] A. B. Kahng, B. Li, L.-S. Peh, and K. Samadi, "ORION 2.0: A fast and accurate NoC power and area model for early-stage design space exploration," in *Proc. Design, Autom. Test Eur. Conf. Exhib.*, Dresden, Germany, Apr. 2009, pp. 423–428, doi: 10.1109/DATE.2009.5090700.
- [77] A. Sharma and Y. R. Kim, "Energy-efficient and rotationally adjustable millimeter-wave wireless interconnects," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 14, no. 3, pp. 551–562, Sep. 2024, doi: 10.1109/JET-CAS.2024.3422371.
- [78] D. W. Matolak, A. Kodi, S. Kaya, D. Ditomaso, S. Laha, and W. Rayess, "Wireless networks-on-chips: Architecture, wireless channel, and devices," *IEEE Wireless Commun.*, vol. 19, no. 5, pp. 58–65, Oct. 2012, doi: 10.1109/MWC.2012.6339473.
- [79] P. P. Pande, A. Ganguly, K. Chang, and C. Teuscher, "Hybrid wireless network on chip: A new paradigm in multi-core design," in *Proc. 2nd Int. Workshop Netw. Chip Architectures*, Microarchitecture, CA, USA, Dec. 2009, pp. 71–76, doi: 10.1145/1645213.1645230.
- [80] D. Zhao, Y. Ouyang, Q. Wang, and H. Liang, "Cm3WiNoCs: Congestion-aware millimeter-wave multichannel wireless networks-on-chip," *IEEE Access*, vol. 8, pp. 24098–24107, 2020, doi: 10.1109/ACCESS.2020.2970425.
- [81] S. Abadal, "WiSync: An architecture for fast synchronization through on-chip wireless communication," in *Proc. Int. Conf. Architectural Sup*port Program. Lang. Operating Syst., Vancouver, BC, Canada, Apr. 2016, vol. 51, no. 4, pp. 3–17, doi: 10.1145/2954679.2872396.
- [82] S.-Y. Lee, M.-Y. Ku, S.-Y. Pan, and C.-C. Lin, "Reconfigurable and scalable artificial intelligence acceleration hardware architecture with RISC-V CNN coprocessor for real-time seizure detection," *IEEE Access*, vol. 13, pp. 31057–31068, 2025, doi: 10.1109/ACCESS.2025.3538781.
- [83] M. O. Agyeman, A. Ahmadinia, and N. Bagherzadeh, "Performance and energy aware inhomogeneous 3D networks-on-chip architecture generation," *IEEE Trans. Parallel Distrib. Syst.*, vol. 27, no. 6, pp. 1756–1769, Jun. 2016, doi: 10.1109/TPDS.2015.2457444.



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