Jaina K. Patel

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ACADEMIC DETAILS

Qualification	University	Institute	Year	CPI
Master of Engineering: Computer Engineering	University of Toronto	The Edward S. Rogers Sr. Department	Sept 2018-present	3.7/4
Bachelor of Engineering: Electronics and Communication	Gujarat Technological University	L.D. College of Engineering	Aug 2014-May 2018	9.19/10

FIELD OF INTEREST

- RTL Designing and Verification, Designing on FPGA, ASIC Design, Computer Architecture

TECHNICAL SKILLS

- **Languages:** C, Verilog, VHDL, Cuda Programming
- **Scripts:** Shell, Perl
- **Tools:** Xilinx ISE Design Suite, Questasim, Modelsim, Vivado, MAX+PLUS II- Altera, Altera Quartus, Cadence Virtuoso, Encounter, Microwind, MATLAB, Atmel Studios

EXPERIENCE

- **University of Toronto** (Winter 2019, Summer 2019)
  Teaching Assistant
  1) Course: Computer Organization (CSC258)
  2) Tasks: Conducting laboratory sessions on verilog, evaluating and managing labs and exams

- **Dhirubhai Ambani Institute of Information and Communication Technology** Gujarat, India
  Research Intern (Summer 2018)
  Trained by: Dr. Amit Bhatt (Professor)
  1) RTL Design and Implementation of a 5-Stage Pipelining Architecture for RISCV-32 bit Instruction Set architecture using verilog on Xilinx ISE Design Suite 14.7.
  2) Designed Fetch, Decode, Execute, Memory and Write back stages for Arithmetic, Logical, Memory and Branch Instructions along with Hazard detection and Control unit which decides whether the dependencies between the instructions can be avoided using forwarding or stalling.
  3) Synthesized the design using Cadence Synthesis Tool (slack balancing).

- **"WE HEAR"** (A start-up) GUSEC, India
  Intern (Fall 2017)
  1) Worked with the R&D team to develop an efficient and cost-effective Hearing Aid using Bone Conduction Hearing Technology.

ACADEMIC PROJECTS

- **Re-configurable Cache Implementation on FPGA** (Winter 2019-Present)
  Guided by: Dr. Natalie Enright Jerger (*Professor, University of Toronto*)
  1) Designed a 64KB reconfigurable-cache memory supporting Direct Mapped (D.M.) and 2-way, 4-way or 8-way Set Associative (S.A.) cache modes to study the relationship between the performance of the processor for different benchmarks and cache memory parameters.
  2) These results will then be used to provide the processor run-time cache reconfiguration.

- **Hardware Implementation of Video Encoder** (Winter 2019)
  Guided by: Prof. Ihab Amer (*Professor, University of Toronto*)
  1) Boosting Performance per Watt of a Video encoder through Hardware Acceleration, as the encoder spends

the bulk portion of its run-time on motion estimation/compensation.
2) Implemented motion estimation/compensation on a hardware to get better Rate-Distortion with efficient memory footprint.

- **Hidden Supports** (Winter 2019)
  1) Studied performance enhancement in GPUs over CPUs for a highly parallel algorithm- Hidden supports. Needed for a 3D zoetrope involved in manufacturing of individual frame in a 3D printed animation.
  2) The speedup for this algorithm on Nvidia GTX-980 GPU over Intel Core-i7 CPU was 120.5x(average).

- **Successive Approximation Analog to Digital Converter (SAR ADC)** (Fall 2018)
  1) Designed the Schematic and Layout of the Digital logic component of the SAR ADC with STA analysis.
  2) Integrated the whole SAR ADC in the given pad-frame of 720x980 um and Performed necessary DRC, LVS and calculated timing constraints of the design.

- **CAD Tool for RAM Mapping** (Fall 2018)
  1) Designed a CAD Tool with reference to Stratix IV-like RAM architecture that maps "logical RAMs" needed by the given circuit design to "physical RAMs".
  2) The tool supported 3 physical RAMS- 2 BlockRams of 8k and 128k and a LUTRAM.

- **Multiport UART communication protocol implementation on FPGA (Verilog)** (Spring 2018)
  Guided by: Mr. Ghanshyam Doshi (*Scientist, Space Application Centre (SAC), Ahmedabad, India*)
  1) Designed multiple channels of UART communication protocol using finite state machine with each channel working on different baud rate.
  2) Verified this design on Xilinx Spartan6 FPGA with a master-slave configuration between 2 PCs for a two-way communication.

- **RTL Design and Verification using Verilog:**
  1) Synchronous and Asynchronous First In First Out (FIFO)
  2) Arithmetic and Logical Unit (ALU) and Booth Multiplier
  3) Round Robin Arbiter and Universal Shift Register
  4) FIR Filter designing and optimization to compare signal processing on DSP and FPGA

COURSES

- **Fall 2018:** Reconfigurable Computing & FPGA Architecture, VLSI Design Methodologies, Computer Architecture
- **Winter 2019:** Parallel Computer Architecture & Programming, Hardware-Accelerated Digital Systems, Programming Massively Parallel Multiprocessors & Heterogeneous Systems (CUDA Programming)

PUBLICATION

- Drashtiben G Patel, Jaina K Patel, Pranati R Trivedi,"Emerging Technologies: Li-Fi and IoT for Healthcare Monitoring", in IEEE conference ICTEE-2017, Pune, Maharashtra, India, Dec 2017
- Jaina Patel, "RISC (16 Bit) Processor Design using Verilog in Modelsim", International Journal of Innovative Research in Science, Engineering and Technology (IJIRSET), Vol. 6, Issue 10, Oct 2017

SCHOLARSHIP AND CERTIFICATES

- Received Scholarships from 'The Government of India-Ministry of Human Resource Development' and 'Innovation in Science Pursuit for Inspired Research' for being top 1% student of the state for higher education
- Trained in PLC and SCADA (SIMATIC S7-1200 and SIMATIC S7-300) by Siemens Center of Excellence.

EXTRA CURRICULAR ACTIVITIES

- Co-Founder of Literary Club at college which enhances soft skills of students lacking English competency. Conducted and Organised events and workshops at IEEE Student Branch Club, IEEE Women In Engineering Club, and Robocon Club (Technical Club) at LDCE (3 years)