IPD GROUP 2 ENCORE 1.0

JAINAM BHEDA(TE)

JAYESH VYAS(TE)

RUSHABH DESAI(SE)

SAKET TEJPAL(SE)

This document details the design of a buck converter that steps down an input voltage of 24V to an output voltage of 5V with an efficiency of at least 90%. The design considerations include component selection, calculations, and the PCB layout process using KiCad.

Circuit Components

1 Power NMOS

Selected NMOS: IRF540

Rating: Suitable for the expected current and voltage levels.

2 Inductor

Inductor Value (L): 130 µH (standard value)

Current Rating: Chosen to handle the peak inductor current with a safety margin.

3 Capacitor

Output Capacitor (C): 47 µF

Voltage Rating: Rated for at least 10V to ensure reliability.

4 Resistors

Used for feedback and gate drive as needed.

Gate Resistor: Calculated to limit current to the gate of the NMOS.

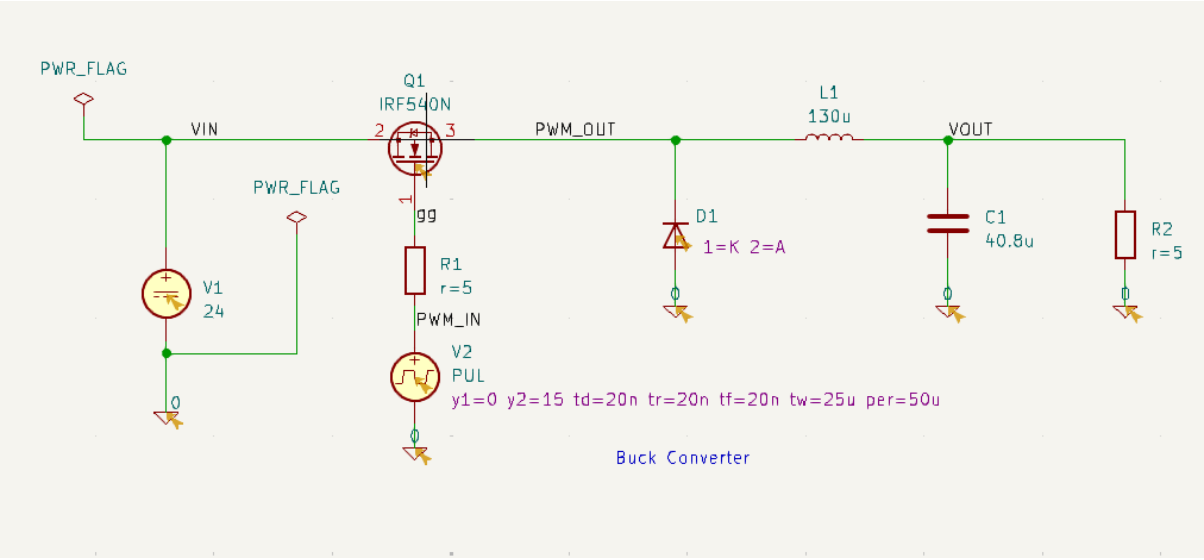
5 Diode

Selected Diode: Schottky diode rated for at least 5A and 30V.

Semantic Diagram

A semantic diagram was created to illustrate the relationships between the components used in the buck converter design. This includes:

- NMOS switching control
- Inductor energy storage
- Diode rectification
- Output filtering with capacitors



IPD Group no. 2
En-core – 1

Jainam Bheda, Jayesh Vyas., Rushabh desai, Suhrit

DD MM YYYY

Buck Converter.

step down voltage from higher level (24 V) to (5V) using switching (power NMOS), an inductor, a diode, and a capacitor

The basic operation involves switching the NMOS on/off, which allows energy to be stored in inductor and then transferred to O/P capacitor.

Input voltage (Vin) : 24V.
Output voltage (Vout) = 5V.
Output current (Iout) = 1A.
Maximum input power Pin = 24W
min η % = 90%

$P_{out} = V_{out} \times I_{out}$.
$= 5V \times 1A = 5W$ //

$V_{inmin} = 24 - 0.48 = 23.52V$.
$V_{inmax} = 24 + 0.48 = 24.48V$

$P_{inmax} = \frac{P_{out}}{\eta} = \frac{5W}{0.9} \approx 5.56W$ //

Duty cycle $D = \frac{V_{out}}{V_{in}}$

$D = \frac{5V}{23.52V} \approx 0.2125$ //

Inductor selection.

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{\Delta I_L \times V_{in} \times F}$$

where ΔI_L is inductor ripple current (we will assume is 30% of Iout)

$\Delta I_L = 0.3A$

F = switching frequency (assume 100KHz)

$$L = \frac{5 \times 18.52}{0.3 \times 23.52 \times 100000}$$

$= 0.0001304H$

$L = 130.4\mu H.$ //

O/P capacitor C1

$$C = \frac{I_{out} \times D}{\Delta V_{out} \times F}$$

ΔV_{out} 1% of 5V

$$C = \frac{1A \times 0.2125}{0.05V \times 100KHz} = 42.5\mu F$$ //

Foowarrd current Rating (I_F) : at least 1.5 times $I_{out(max)}$

$I_F \geq 1.5A$ //

Reverse voltage Rating (V_R) : at least 30V (1.2 times V_{inmax})

$V_R \geq 30V$ //

$\Delta I_L = 0.3A$

$I_{L(max)} = I_{out(max)} + \frac{\Delta I_L}{2}$

$= 1A + 0.15A$

$I_{Lmax} = 1.15A$ //

NMOS

$V_{DS(max)} \geq V_{inmax} + V_{out}$

$I_{SW(max)} = 1.15A.$

The capacitor should be rated at least 1.5 times O/P voltage.

$V_{C1} \geq 1.5 \times 5 = 7.5V.$

1) Inductor (L1):
   - Value : 130 μH
   - Current rating : At least 1.5A.

2) Output capacitor (C1);
   - Value : 40.8 μF
   - ~~current~~ voltage rating : At least 10V

3) Diode
   - Forward current : At least 1.5A. //
   - Reverse voltage : At least 30V //

4) NMOS transistor.
   - Voltage rating : At least 30V //
   - ~~current~~ Rating : At least 1.5A. //

Conclusion

The design of the buck converter meets the specified requirements for input and output voltage and current. The selected components and PCB layout ensure efficient operation with a conversion efficiency of at least 90%. The design was verified through simulations, ensuring stability and performance.

Refrences:

Basic Calculation of a Buck Converter's Power Stage (Rev. B)