**IPD GROUP 2 ENCORE 1.0**

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This document details the design of a buck converter that steps down an input voltage of 24V to an output voltage of 5V with an efficiency of at least 90%. The design considerations include component selection, calculations, and the PCB layout process using KiCad.

**Circuit Components**

1. Power NMOS

Selected NMOS: IRF540

Rating: Suitable for the expected current and voltage levels.

2 Inductor

Inductor Value (L): 130 µH (standard value)

Current Rating: Chosen to handle the peak inductor current with a safety margin.

3 Capacitor

Output Capacitor (C): 47 µF

Voltage Rating: Rated for at least 10V to ensure reliability.

4 Resistors

Used for feedback and gate drive as needed.

Gate Resistor: Calculated to limit current to the gate of the NMOS.

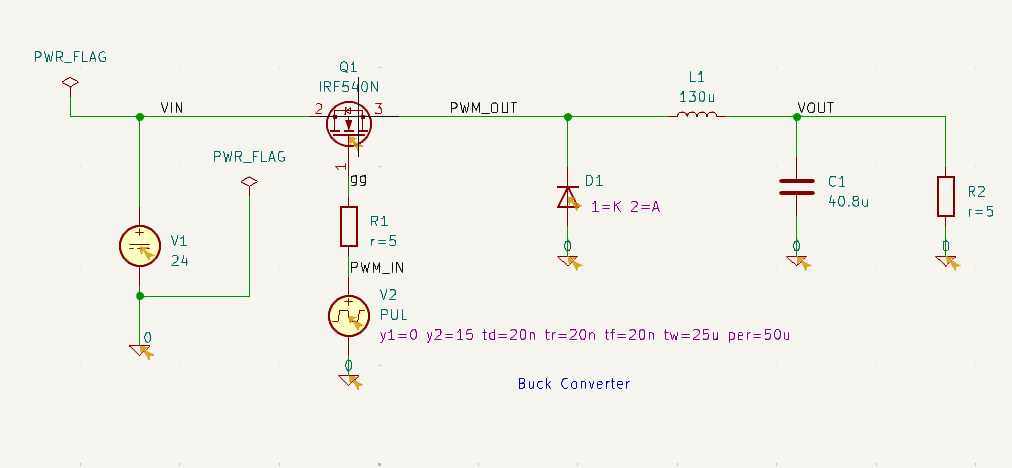
5 Diode

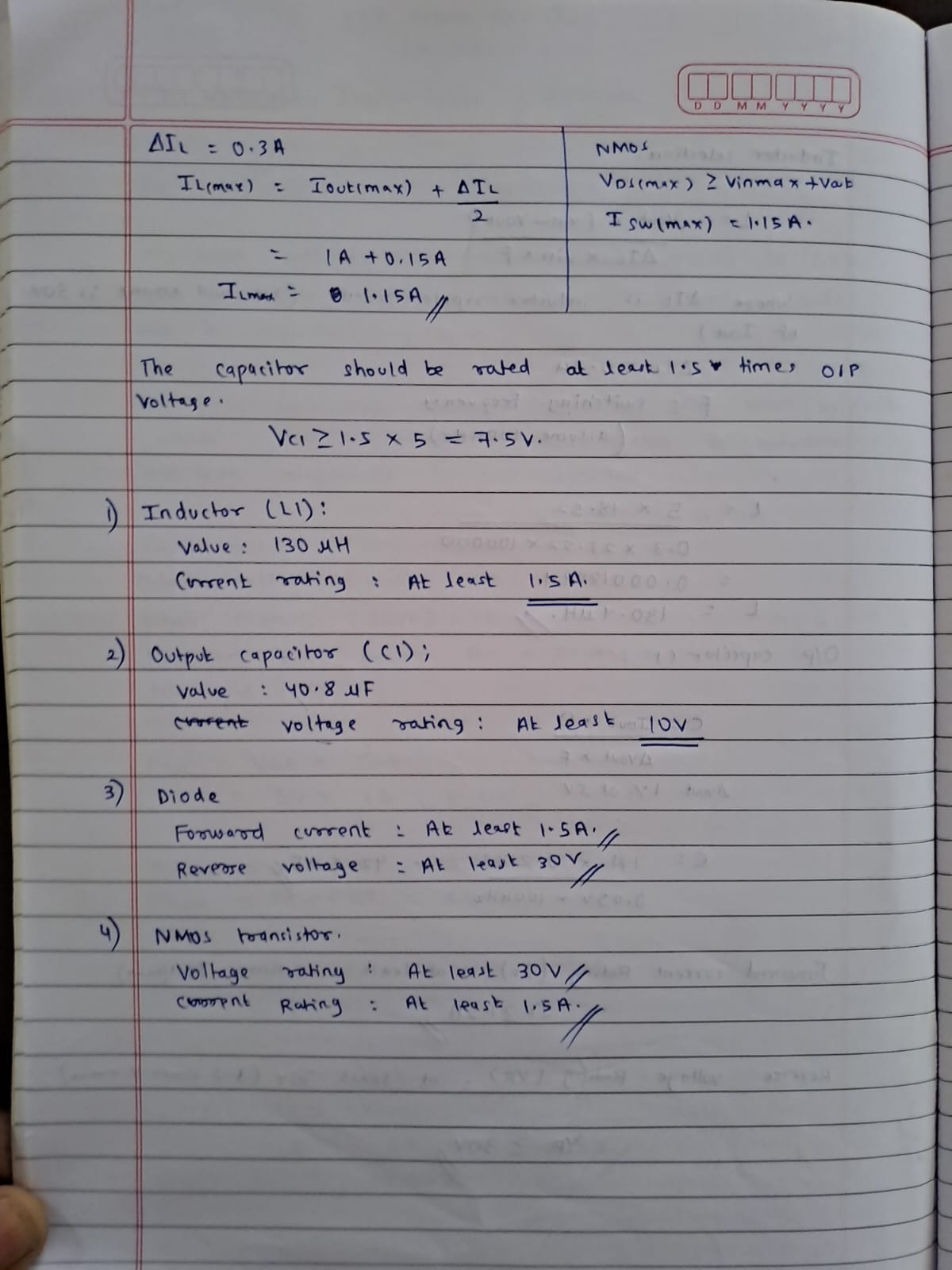
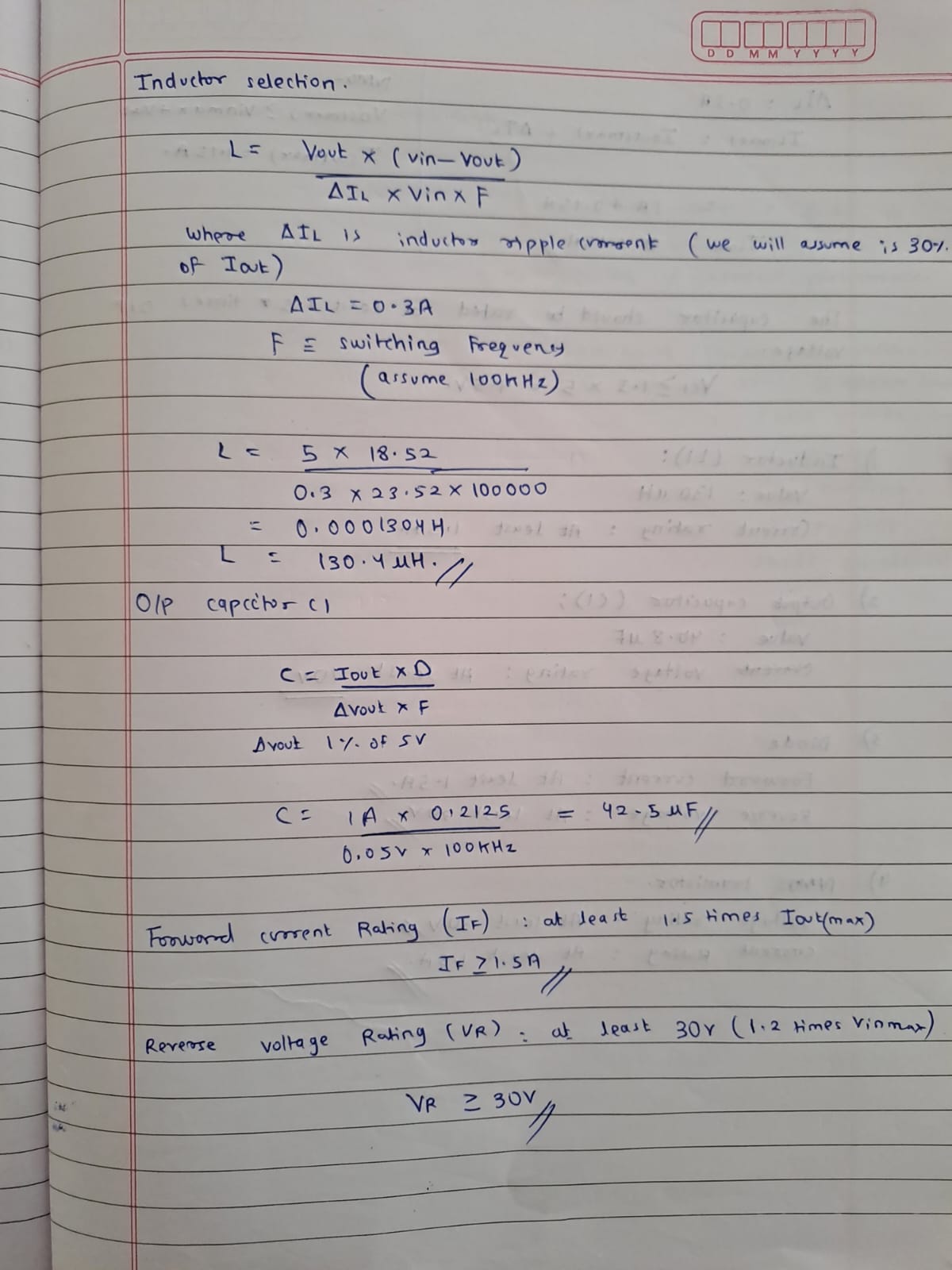
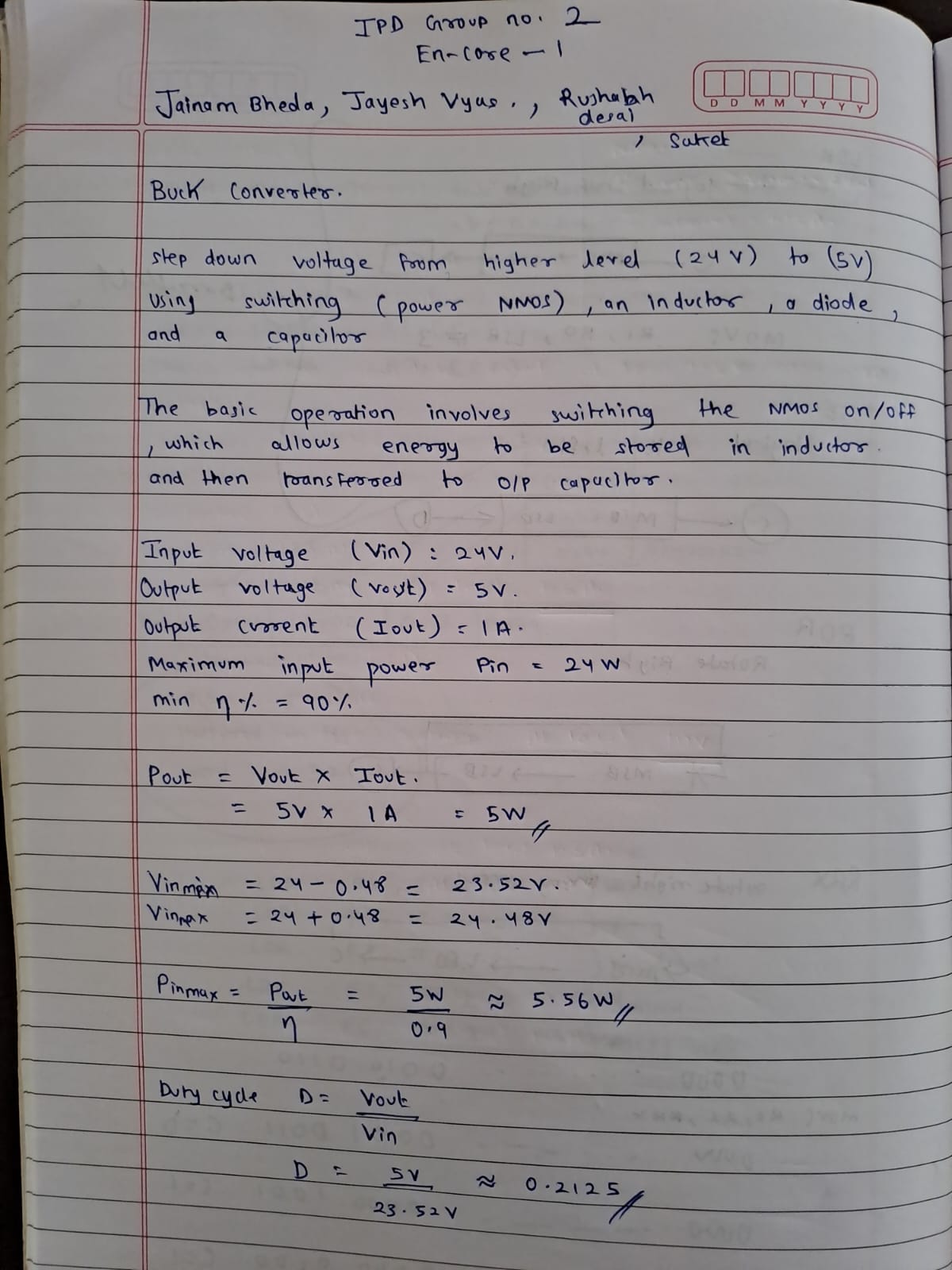
Selected Diode: Schottky diode rated for at least 5A and 30V.

**Semantic Diagram**

A semantic diagram was created to illustrate the relationships between the components used in the buck converter design. This includes:

* NMOS switching control
* Inductor energy storage
* Diode rectification
* Output filtering with capacitors





**Conclusion**

The design of the buck converter meets the specified requirements for input and output voltage and current. The selected components and PCB layout ensure efficient operation with a conversion efficiency of at least 90%. The design was verified through simulations, ensuring stability and performance.  
  
**Refrences:**

[Basic Calculation of a Buck Converter's Power Stage (Rev. B)](https://www.ti.com/lit/an/slva477b/slva477b.pdf?ts=1725936588246)