MULTIPLEXER 8:1

module mux8\_1\_case(input D0,D1,D2,D3,D4,D5,D6,D7, input [2:0]S,output reg Y);

always @ (\*)

begin

case (S)

3'b000 : Y = D0; 3'b001 : Y = D1;

3'b010 : Y = D2; 3'b011 : Y = D3;

3'b100 : Y = D4; 3'b101 : Y = D5;

3'b110 : Y = D6; 3'b111 : Y = D7;

default : Y = 1'b0;

endcase

end

endmodules

TESTBENCH

module mux8\_1\_gate(input D0,D1,D2,D3,D4,D5,D6,D7, input [2:0]S,output Y);

wire inv0, inv1, inv2;

wire a0, a1, a2, a3, a4, a5, a6, a7 ;

not not\_0 (inv0, S[0]);

not not\_1 (inv1, S[1]);

not not\_2 (inv2, S[2]);

and and\_0 (a0, inv2, inv1, inv0,D0);

and and\_1 (a1, inv2, inv1, S[0],D1);

and and\_2 (a2, inv2, S[1], inv0,D2);

and and\_3 (a3, inv2, S[1], S[0],D3);

and and\_4 (a4, S[2], inv1, inv0,D4);

and and\_5 (a5, S[2], inv1, S[0],D5);

and and\_6 (a6, S[2], S[1], inv0,D6);

and and\_7 (a7, S[2], S[1], S[0],D7);

or or\_0(Y, a0, a1, a2, a3, a4, a5, a6, a7);

endmodule