```
# ++++++++++++++++++++++++++++++++++++++++++++++
# ++++++++++       REPORT INFO       ++++++++++
# ++++++++++++++++++++++++++++++++++++++++++++++
#
#
# SUMMARY
# ================================================
# |     Property     |           Value           |
# ================================================
# | User             | runner                    |
# | Host             | c8262c8d9b11              |
# | Tool             | Riviera-PRO 2025.04       |
# | Report file      | /home/runner/cov.txt      |
# | Report date      | 2026-02-26 19:51          |
# | Report arguments | -verbose                  |
# | Input file       | /home/runner/fcover.acdb  |
# | Input file date  | 2026-02-26 19:51          |
# | Number of tests  | 1                         |
# ================================================
#
#
# TEST DETAILS
# ================================================================================
# | Property |                              Value                               |
# ================================================================================
# | Test     | fcover.acdb:riscv_random_test_100                                |
# | Status   | Ok                                                               |
# | Args     | asim +access+r +UVM_TESTNAME=riscv_random_test -sv_seed 100      |
# | Simtime  | 13535 ns                                                         |
# | Cputime  | 24.267 s                                                         |
# | Seed     | 100                                                              |
# | Date     | 2026-02-26 19:50                                                 |
# | User     | runner                                                           |
# | Host     | c8262c8d9b11                                                     |
# | Host os  | Linux64                                                          |
# | Tool     | Riviera-PRO 2025.04 (simulator)                                  |
# ================================================================================
#
#
# ++++++++++++++++++++++++++++++++++++++++++++++
# ++++++++++     DESIGN HIERARCHY    ++++++++++
# ++++++++++++++++++++++++++++++++++++++++++++++
#
#
# CUMULATIVE SUMMARY
# ================================================
```

```
# |    Coverage Type    | Weight | Hits/Total |
# ===============================================
# | Covergroup Coverage |      1 |    96.010% |
# |---------------------|--------|------------|
# | Types               |        |    13 / 19 |
# ===============================================
# CUMULATIVE INSTANCE-BASED COVERAGE: 96.010%
# COVERED INSTANCES: 0 / 1
# FILES: 1
#
#
# CLASS - /riscv_coverage : work.riscv_coverage
#
#
#     SUMMARY
#     ===============================================
#     |    Coverage Type    | Weight | Hits/Total |
#     ===============================================
#     | Covergroup Coverage |      1 |    96.010% |
#     |---------------------|--------|------------|
#     | Types               |        |    13 / 19 |
#     ===============================================
#     WEIGHTED AVERAGE LOCAL: 96.010%
#
#
#     COVERGROUP COVERAGE
#
=============================================================================================
#     |                   Covergroup                   |   Hits   |  Goal /  |  Status
|
#     |                                                |          | At Least |
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_opcode                | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_opcode               | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
```

```
#     | bin R_TYPE                                      |      266 |        1 | Covered
|
#     | bin I_TYPE                                      |      324 |        1 | Covered
|
#     | bin LOAD_TYPE                                   |      436 |        1 | Covered
|
#     | bin STORE_TYPE                                  |      232 |        1 | Covered
|
#     | bin BRANCH_TYPE                                 |       80 |        1 | Covered
|
#     | bin JAL_TYPE                                    |       52 |        1 | Covered
|
#     | bin JALR_TYPE                                   |       54 |        1 | Covered
|
#     | bin LUI_TYPE                                    |      536 |        1 | Covered
|
#     | bin AUIPC_TYPE                                  |       46 |        1 | Covered
|
#     | illegal default bin illegal_opcode              |        0 |    -     | Zero
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_funct3                | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin f3_vals[0]                                  |      236 |        1 | Covered
|
#     | bin f3_vals[1]                                  |      168 |        1 | Covered
|
#     | bin f3_vals[2]                                  |      804 |        1 | Covered
|
#     | bin f3_vals[3]                                  |      148 |        1 | Covered
|
#     | bin f3_vals[4]                                  |      158 |        1 | Covered
|
#     | bin f3_vals[5]                                  |      156 |        1 | Covered
|
#     | bin f3_vals[6]                                  |      170 |        1 | Covered
|
#     | bin f3_vals[7]                                  |      186 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::opcode_funct3_cross           | 100.000% | 100.000% | Covered
|
```

```
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin <R_TYPE,f3_vals[0]>                       |       46 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[1]>                       |       34 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[2]>                       |       38 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[3]>                       |       32 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[4]>                       |       28 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[5]>                       |       26 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[6]>                       |       26 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[7]>                       |       36 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[0]>                       |       30 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[1]>                       |       34 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[2]>                       |       40 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[3]>                       |       44 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[4]>                       |       38 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[5]>                       |       40 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[6]>                       |       46 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[7]>                       |       52 |        1 | Covered
|
#     | bin <LOAD_TYPE,f3_vals[2]>                    |      436 |        1 | Covered
|
#     | bin <STORE_TYPE,f3_vals[2]>                   |      232 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[0]>                  |       10 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[1]>                  |       18 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[4]>                  |       12 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[5]>                  |       14 |        1 | Covered
|
```

```
#     | bin <BRANCH_TYPE,f3_vals[6]>                    |       12 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[7]>                    |       14 |        1 | Covered
|
#     | bin <JALR_TYPE,f3_vals[0]>                      |        4 |        1 | Covered
|
#     | ignore bin no_f3_jal                            |       52 |    -     |
Occurred  |
#     | ignore bin no_f3_lui                            |      536 |    -     |
Occurred  |
#     | ignore bin no_f3_auipc                          |       46 |    -     |
Occurred  |
#     | ignore bin jalr_f1                              |        8 |    -     |
Occurred  |
#     | ignore bin jalr_f2                              |        2 |    -     |
Occurred  |
#     | ignore bin jalr_f3                              |       12 |    -     |
Occurred  |
#     | ignore bin jalr_f4                              |       10 |    -     |
Occurred  |
#     | ignore bin jalr_f5                              |        8 |    -     |
Occurred  |
#     | ignore bin jalr_f6                              |        2 |    -     |
Occurred  |
#     | ignore bin jalr_f7                              |        8 |    -     |
Occurred  |
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_decode                 | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_funct3                | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin ADD_SUB                                     |       46 |        1 | Covered
|
#     | bin SLL                                         |       34 |        1 | Covered
|
#     | bin SLT                                         |       38 |        1 | Covered
|
```

```
#     | bin SLTU                                          |       32 |        1 | Covered
|
#     | bin XOR                                           |       28 |        1 | Covered
|
#     | bin SR                                            |       26 |        1 | Covered
|
#     | bin OR                                            |       26 |        1 | Covered
|
#     | bin AND                                           |       36 |        1 | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_funct7                  | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | bin base                                          |      228 |        1 | Covered
|
#     | bin alt                                           |       38 |        1 | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_f3_f7                     | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | bin <ADD_SUB,base>                                |       28 |        1 | Covered
|
#     | bin <ADD_SUB,alt>                                 |       18 |        1 | Covered
|
#     | bin <SLL,base>                                    |       34 |        1 | Covered
|
#     | bin <SLT,base>                                    |       38 |        1 | Covered
|
#     | bin <SLTU,base>                                   |       32 |        1 | Covered
|
#     | bin <XOR,base>                                    |       28 |        1 | Covered
|
#     | bin <SR,base>                                     |        6 |        1 | Covered
|
#     | bin <SR,alt>                                      |       20 |        1 | Covered
|
#     | bin <OR,base>                                     |       26 |        1 | Covered
|
#     | bin <AND,base>                                    |       36 |        1 | Covered
|
```

```
#
================================================================================
#     | TYPE /riscv_coverage/cov_registers             | 100.000% | 100.000% | Covered
|
#
================================================================================
#     | INSTANCE <UNNAMED1>                            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rs1                  | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                       |      824 |        1 | Covered
|
#     | bin low                                        |      214 |        1 | Covered
|
#     | bin mid                                        |      528 |        1 | Covered
|
#     | bin high                                       |      460 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rs2                  | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                       |      634 |        1 | Covered
|
#     | bin low                                        |      210 |        1 | Covered
|
#     | bin mid                                        |      728 |        1 | Covered
|
#     | bin high                                       |      454 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd                   | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                       |       98 |        1 | Covered
|
#     | bin low                                        |      278 |        1 | Covered
|
```

```
#     | bin mid                                          |     1004 |        1 | Covered
|
#     | bin high                                         |      646 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_rs1_rd                   | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin <zero,zero>                                  |       50 |        1 | Covered
|
#     | bin <zero,low>                                   |      108 |        1 | Covered
|
#     | bin <zero,mid>                                   |      408 |        1 | Covered
|
#     | bin <zero,high>                                  |      258 |        1 | Covered
|
#     | bin <low,zero>                                   |        4 |        1 | Covered
|
#     | bin <low,low>                                    |       36 |        1 | Covered
|
#     | bin <low,mid>                                    |      108 |        1 | Covered
|
#     | bin <low,high>                                   |       66 |        1 | Covered
|
#     | bin <mid,zero>                                   |       28 |        1 | Covered
|
#     | bin <mid,low>                                    |       66 |        1 | Covered
|
#     | bin <mid,mid>                                    |      242 |        1 | Covered
|
#     | bin <mid,high>                                   |      192 |        1 | Covered
|
#     | bin <high,zero>                                  |       16 |        1 | Covered
|
#     | bin <high,low>                                   |       68 |        1 | Covered
|
#     | bin <high,mid>                                   |      246 |        1 | Covered
|
#     | bin <high,high>                                  |      130 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_rs2_rd                   | 100.000% | 100.000% | Covered
|
```

```
#     |---------------------------------------------|----------|----------|--------
---|
#     | bin <zero,zero>                             |       16 |        1 | Covered
|
#     | bin <zero,low>                              |      102 |        1 | Covered
|
#     | bin <zero,mid>                              |      310 |        1 | Covered
|
#     | bin <zero,high>                             |      206 |        1 | Covered
|
#     | bin <low,zero>                              |       22 |        1 | Covered
|
#     | bin <low,low>                               |       24 |        1 | Covered
|
#     | bin <low,mid>                               |      100 |        1 | Covered
|
#     | bin <low,high>                              |       64 |        1 | Covered
|
#     | bin <mid,zero>                              |       36 |        1 | Covered
|
#     | bin <mid,low>                               |       90 |        1 | Covered
|
#     | bin <mid,mid>                               |      358 |        1 | Covered
|
#     | bin <mid,high>                              |      244 |        1 | Covered
|
#     | bin <high,zero>                             |       24 |        1 | Covered
|
#     | bin <high,low>                              |       62 |        1 | Covered
|
#     | bin <high,mid>                              |      236 |        1 | Covered
|
#     | bin <high,high>                             |      132 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_imm                | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                         | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_imm               | 100.000% | 100.000% | Covered
|
```

```
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin zero                                      |      286 |        1 | Covered
|
#     | bin small_pos                                 |      132 |        1 | Covered
|
#     | bin mid_pos                                   |      480 |        1 | Covered
|
#     | bin large_pos                                 |      398 |        1 | Covered
|
#     | bin mid_neg                                   |       76 |        1 | Covered
|
#     | bin large_neg                                 |       84 |        1 | Covered
|
#     | ignore bin small_neg                          |        8 |    -     |
Occurred  |
#
================================================================================
#     | TYPE /riscv_coverage/cov_branch               | 100.000% | 100.000% | Covered
|
#
================================================================================
#     | INSTANCE <UNNAMED1>                           | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_branch              | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin BEQ                                       |       10 |        1 | Covered
|
#     | bin BNE                                       |       18 |        1 | Covered
|
#     | bin BLT                                       |       12 |        1 | Covered
|
#     | bin BGE                                       |       14 |        1 | Covered
|
#     | bin BLTU                                      |       12 |        1 | Covered
|
#     | bin BGEU                                      |       14 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_forward              | 100.000% | 100.000% | Covered
|
```

```
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                                | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_forward_a                | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin normal                                         |     1887 |        1 | Covered
|
#     | bin mem                                            |      105 |        1 | Covered
|
#     | bin ex                                             |       34 |        1 | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_forward_b                | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin normal                                         |     1963 |        1 | Covered
|
#     | bin mem                                            |       12 |        1 | Covered
|
#     | bin ex                                             |       51 |        1 | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_ab                         | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin <normal,normal>                                |     1830 |        1 | Covered
|
#     | bin <normal,mem>                                   |        8 |        1 | Covered
|
#     | bin <normal,ex>                                    |       49 |        1 | Covered
|
#     | bin <mem,normal>                                   |      102 |        1 | Covered
|
#     | bin <mem,mem>                                      |        3 |        1 | Covered
|
#     | bin <ex,normal>                                    |       31 |        1 | Covered
|
```

```
#     | bin <ex,ex>                                        |        2 |        1 | Covered
|
#     | ignore bin rare_ex_mem                             |        1 |    -     |
Occurred  |
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_hazard                  | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                              | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_stall                  | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin no_stall                                     |     1929 |        1 | Covered
|
#     | bin stall                                        |       97 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_flush                 | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin no_flush                                     |     1929 |        1 | Covered
|
#     | bin flush                                        |       97 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_stall_flush             | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin <no_stall,no_flush>                          |     1929 |        1 | Covered
|
#     | bin <stall,flush>                                |       97 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_redirect               | 100.000% | 100.000% | Covered
|
```

```
#
=================================================================================================
#     | INSTANCE <UNNAMED1>                                 | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_redirect                  | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin no_redirect                                 |     1949 |        1 | Covered
|
#     | bin redirect                                    |       77 |        1 | Covered
|
#
=================================================================================================
#     | TYPE /riscv_coverage/cov_branch_outcome         |  97.222% | 100.000% |
Uncovered |
#
=================================================================================================
#     | INSTANCE <UNNAMED1>                             |  97.222% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_branch_funct3         | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin BEQ                                         |       10 |        1 | Covered
|
#     | bin BNE                                         |       18 |        1 | Covered
|
#     | bin BLT                                         |       12 |        1 | Covered
|
#     | bin BGE                                         |       14 |        1 | Covered
|
#     | bin BLTU                                        |       12 |        1 | Covered
|
#     | bin BGEU                                        |       14 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_taken                 | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
```

```
#     | bin not_taken                                  |       56 |        1 | Covered
|
#     | bin taken                                      |       24 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::branch_outcome_cross         |  91.666% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin <BEQ,not_taken>                            |       10 |        1 | Covered
|
#     | bin <BNE,not_taken>                            |        9 |        1 | Covered
|
#     | bin <BNE,taken>                                |        9 |        1 | Covered
|
#     | bin <BLT,not_taken>                            |        9 |        1 | Covered
|
#     | bin <BLT,taken>                                |        3 |        1 | Covered
|
#     | bin <BGE,not_taken>                            |       10 |        1 | Covered
|
#     | bin <BGE,taken>                                |        4 |        1 | Covered
|
#     | bin <BLTU,not_taken>                           |        8 |        1 | Covered
|
#     | bin <BLTU,taken>                               |        4 |        1 | Covered
|
#     | bin <BGEU,not_taken>                           |       10 |        1 | Covered
|
#     | bin <BGEU,taken>                               |        4 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_hazard_source         |  93.333% | 100.000% |
Uncovered |
#
================================================================================
#     | INSTANCE <UNNAMED1>                            |  93.333% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_stall_opocde         | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
```

```
#     | bin load_caused                                 |       97 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_fwd_a_opcode          | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                      |       89 |        1 | Covered
|
#     | bin i_type                                      |       20 |        1 | Covered
|
#     | bin lui                                         |       16 |        1 | Covered
|
#     | bin auipc                                       |        1 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_fwd_b_opcode          |  80.000% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                      |       23 |        1 | Covered
|
#     | bin i_type                                      |        8 |        1 | Covered
|
#     | bin load                                        |        9 |        1 | Covered
|
#     | bin auipc                                       |        1 |        1 | Covered
|
#     | bin jal                                         |        0 |        1 | Zero
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_reg_hazard             | 100.000% | 100.000% | Covered
|
#
================================================================================
#     | INSTANCE <UNNAMED1>                             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd_eq_rs1             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
```

```
#     | bin no_match                                    |      566 |        1 | Covered
|
#     | bin match                                       |       24 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd_eq_rs2             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin no_match                                    |      258 |        1 | Covered
|
#     | bin match                                       |        8 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rs1_eq_rs2            | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin no_match                                    |      262 |        1 | Covered
|
#     | bin match                                       |        4 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_instr_sequence         |  98.639% | 100.000% |
Uncovered |
#
================================================================================
#     | INSTANCE <UNNAMED1>                             |  98.639% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_prev_type             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                      |      172 |        1 | Covered
|
#     | bin i_type                                      |      306 |        1 | Covered
|
#     | bin load                                        |      526 |        1 | Covered
|
#     | bin store                                       |      231 |        1 | Covered
|
```

```
#     | bin branch                                      |       93 |        1 | Covered
|
#     | bin jal                                         |       73 |        1 | Covered
|
#     | bin lui                                         |      516 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_curr_type             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                      |      266 |        1 | Covered
|
#     | bin i_type                                      |      324 |        1 | Covered
|
#     | bin load                                        |      436 |        1 | Covered
|
#     | bin store                                       |      232 |        1 | Covered
|
#     | bin branch                                      |       80 |        1 | Covered
|
#     | bin jal                                         |       52 |        1 | Covered
|
#     | bin lui                                         |      534 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::seq_cross                     |  95.918% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin <r_type,r_type>                             |      142 |        1 | Covered
|
#     | bin <r_type,i_type>                             |        7 |        1 | Covered
|
#     | bin <r_type,load>                               |        5 |        1 | Covered
|
#     | bin <r_type,store>                              |        2 |        1 | Covered
|
#     | bin <r_type,branch>                             |        6 |        1 | Covered
|
#     | bin <r_type,jal>                                |        2 |        1 | Covered
|
#     | bin <r_type,lui>                                |        6 |        1 | Covered
|
```

```
#     | bin <i_type,r_type>                          |       10 |        1 | Covered
|
#     | bin <i_type,i_type>                          |      269 |        1 | Covered
|
#     | bin <i_type,load>                            |        2 |        1 | Covered
|
#     | bin <i_type,store>                           |        5 |        1 | Covered
|
#     | bin <i_type,branch>                          |        4 |        1 | Covered
|
#     | bin <i_type,jal>                             |        2 |        1 | Covered
|
#     | bin <i_type,lui>                             |       11 |        1 | Covered
|
#     | bin <load,r_type>                            |       87 |        1 | Covered
|
#     | bin <load,i_type>                            |       12 |        1 | Covered
|
#     | bin <load,load>                              |      415 |        1 | Covered
|
#     | bin <load,store>                             |        3 |        1 | Covered
|
#     | bin <load,jal>                               |        1 |        1 | Covered
|
#     | bin <load,lui>                               |        5 |        1 | Covered
|
#     | bin <store,r_type>                           |        2 |        1 | Covered
|
#     | bin <store,i_type>                           |        3 |        1 | Covered
|
#     | bin <store,store>                            |      216 |        1 | Covered
|
#     | bin <store,branch>                           |        2 |        1 | Covered
|
#     | bin <store,jal>                              |        3 |        1 | Covered
|
#     | bin <store,lui>                              |        3 |        1 | Covered
|
#     | bin <branch,r_type>                          |        7 |        1 | Covered
|
#     | bin <branch,i_type>                          |        7 |        1 | Covered
|
#     | bin <branch,load>                            |        4 |        1 | Covered
|
#     | bin <branch,store>                           |        3 |        1 | Covered
|
```

```
#     | bin <branch,branch>                                |       47 |        1 | Covered
|
#     | bin <branch,jal>                                   |        4 |        1 | Covered
|
#     | bin <branch,lui>                                   |       16 |        1 | Covered
|
#     | bin <jal,r_type>                                   |        6 |        1 | Covered
|
#     | bin <jal,i_type>                                   |       11 |        1 | Covered
|
#     | bin <jal,load>                                     |        4 |        1 | Covered
|
#     | bin <jal,store>                                    |        1 |        1 | Covered
|
#     | bin <jal,branch>                                   |        6 |        1 | Covered
|
#     | bin <jal,jal>                                      |       29 |        1 | Covered
|
#     | bin <jal,lui>                                      |       10 |        1 | Covered
|
#     | bin <lui,r_type>                                   |        3 |        1 | Covered
|
#     | bin <lui,i_type>                                   |        9 |        1 | Covered
|
#     | bin <lui,load>                                     |        3 |        1 | Covered
|
#     | bin <lui,store>                                    |        1 |        1 | Covered
|
#     | bin <lui,branch>                                   |       11 |        1 | Covered
|
#     | bin <lui,jal>                                      |        7 |        1 | Covered
|
#     | bin <lui,lui>                                      |      470 |        1 | Covered
|
#
# ================================================================================
#     | TYPE /riscv_coverage/cov_data_dep                  | 100.000% | 100.000% | Covered
|
#
# ================================================================================
#     | INSTANCE <UNNAMED1>                                | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_raw_rs1                  | 100.000% | 100.000% | Covered
|
```

```
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin no_dep                                    |     1894 |        1 | Covered
|
#     | bin dep                                       |      130 |        1 | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_raw_rs2             | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin no_dep                                    |     1977 |        1 | Covered
|
#     | bin dep                                       |       47 |        1 | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_raw_both            | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin no_dep                                    |     2019 |        1 | Covered
|
#     | bin dep                                       |        5 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_corner               | 100.000% | 100.000% | Covered
|
#
================================================================================
#     | INSTANCE <UNNAMED1>                           | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd_zero             | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin non_zerp                                  |      776 |        1 | Covered
|
#     | bin rd_zero                                   |       26 |        1 | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
```

```
#     | COVERPOINT <UNNAMED1>::cp_redirect_after_stall | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin no                                         |     2026 |        1 | Covered
|
#     | ignore bin impossible                          |        0 |    -     | Zero
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_branch_with_fwd      | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin no_fwd                                     |       56 |        1 | Covered
|
#     | bin has_fwd                                    |       24 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_memory                |  83.333% | 100.000% |
Uncovered |
#
================================================================================
#     | INSTANCE <UNNAMED1>                            |  83.333% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_load_addr            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin low_addr                                   |       58 |        1 | Covered
|
#     | bin mid_addr                                   |      180 |        1 | Covered
|
#     | bin high_addr                                  |      198 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_store_addr           | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin low_addr                                   |       22 |        1 | Covered
|
```

```
#     | bin mid_addr                                    |       92 |        1 | Covered
|
#     | bin high_addr                                   |      118 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_store_then_load       |  50.000% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin no                                          |     2026 |        1 | Covered
|
#     | bin yes                                         |        0 |        1 | Zero
|
#
================================================================================================
#     | TYPE /riscv_coverage/cov_alu_result             |  85.000% | 100.000% |
Uncovered |
#
================================================================================================
#     | INSTANCE <UNNAMED1>                             |  85.000% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_shamt                 |  80.000% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                        |        0 |        1 | Zero
|
#     | bin low                                         |       26 |        1 | Covered
|
#     | bin mid                                         |       28 |        1 | Covered
|
#     | bin high                                        |        4 |        1 | Covered
|
#     | bin max                                         |        2 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_shamt_imm             |  75.000% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                        |        0 |        1 | Zero
|
```

```
#     | bin low                                          |       18 |        1 | Covered
|
#     | bin mid                                          |       40 |        1 | Covered
|
#     | bin high                                         |       16 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_slt_result             | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin low                                          |        6 |        1 | Covered
|
#     | bin mid                                          |       26 |        1 | Covered
|
#     | bin high                                         |       36 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_branch_direction        |  66.666% | 100.000% |
Uncovered |
#
================================================================================
#     | INSTANCE <UNNAMED1>                              |  66.666% | 100.000% |
Uncovered |
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_direction              |  50.000% | 100.000% |
Uncovered |
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin forward                                      |       80 |        1 | Covered
|
#     | bin backward                                     |        0 |        1 | Zero
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_taken_dir              | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin not_taken                                    |       56 |        1 | Covered
|
#     | bin taken                                        |       24 |        1 | Covered
|
```

```
#     |-----------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::direction_outcome           |  50.000% | 100.000% |
Uncovered |
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin <forward,not_taken>                       |       56 |        1 | Covered
|
#     | bin <forward,taken>                           |       24 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_flush_source         | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                           | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_redirect_source     | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin branch                                    |       24 |        1 | Covered
|
#     | bin jal                                       |       26 |        1 | Covered
|
#     | bin jalr                                      |       27 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_writeback            | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                           | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_wb_source           | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------|----------|----------|--------
---|
#     | bin alu_wb[19]                                |      302 |        1 | Covered
|
```

```
#     | bin alu_wb[23]                                  |       44 |        1 | Covered
|
#     | bin alu_wb[51]                                  |      250 |        1 | Covered
|
#     | bin alu_wb[55]                                  |      526 |        1 | Covered
|
#     | bin alu_wb[103]                                 |       52 |        1 | Covered
|
#     | bin alu_wb[111]                                 |       52 |        1 | Covered
|
#     | bin mem_wb                                      |      414 |        1 | Covered
|
#
================================================================================
#
#
# ++++++++++++++++++++++++++++++++++++++++++++
# ++++++++++       DESIGN UNITS      ++++++++++
# ++++++++++++++++++++++++++++++++++++++++++++
#
#
# CUMULATIVE SUMMARY
# ============================================
# |    Coverage Type    | Weight | Hits/Total |
# ============================================
# | Covergroup Coverage |      1 |    96.010% |
# |---------------------|--------|------------|
# | Types               |        |    13 / 19 |
# ============================================
# CUMULATIVE DESIGN-BASED COVERAGE: 96.010%
# COVERED DESIGN UNITS: 0 / 1
# FILES: 1
#
#
# CLASS - work.riscv_coverage
#
#
#     SUMMARY
#     ============================================
#     |    Coverage Type    | Weight | Hits/Total |
#     ============================================
#     | Covergroup Coverage |      1 |    96.010% |
#     |---------------------|--------|------------|
#     | Types               |        |    13 / 19 |
#     ============================================
#     WEIGHTED AVERAGE: 96.010%
```

```
#
#
#     COVERGROUP COVERAGE
#
================================================================================================
#     |                    Covergroup                    |   Hits   |  Goal /  |  Status
|
#     |                                                  |          | At Least |
|
#
================================================================================================
#     | TYPE /riscv_coverage/cov_opcode                  | 100.000% | 100.000% | Covered
|
#
================================================================================================
#     | INSTANCE <UNNAMED1>                              | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_opcode                 | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin R_TYPE                                       |      266 |        1 | Covered
|
#     | bin I_TYPE                                       |      324 |        1 | Covered
|
#     | bin LOAD_TYPE                                    |      436 |        1 | Covered
|
#     | bin STORE_TYPE                                   |      232 |        1 | Covered
|
#     | bin BRANCH_TYPE                                  |       80 |        1 | Covered
|
#     | bin JAL_TYPE                                     |       52 |        1 | Covered
|
#     | bin JALR_TYPE                                    |       54 |        1 | Covered
|
#     | bin LUI_TYPE                                     |      536 |        1 | Covered
|
#     | bin AUIPC_TYPE                                   |       46 |        1 | Covered
|
#     | illegal default bin illegal_opcode               |        0 |    -     | Zero
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_funct3                 | 100.000% | 100.000% | Covered
```

```
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin f3_vals[0]                                  |      236 |        1 | Covered
|
#     | bin f3_vals[1]                                  |      168 |        1 | Covered
|
#     | bin f3_vals[2]                                  |      804 |        1 | Covered
|
#     | bin f3_vals[3]                                  |      148 |        1 | Covered
|
#     | bin f3_vals[4]                                  |      158 |        1 | Covered
|
#     | bin f3_vals[5]                                  |      156 |        1 | Covered
|
#     | bin f3_vals[6]                                  |      170 |        1 | Covered
|
#     | bin f3_vals[7]                                  |      186 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::opcode_funct3_cross           | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin <R_TYPE,f3_vals[0]>                         |       46 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[1]>                         |       34 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[2]>                         |       38 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[3]>                         |       32 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[4]>                         |       28 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[5]>                         |       26 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[6]>                         |       26 |        1 | Covered
|
#     | bin <R_TYPE,f3_vals[7]>                         |       36 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[0]>                         |       30 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[1]>                         |       34 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[2]>                         |       40 |        1 | Covered
```

```
|
#     | bin <I_TYPE,f3_vals[3]>                          |       44 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[4]>                          |       38 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[5]>                          |       40 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[6]>                          |       46 |        1 | Covered
|
#     | bin <I_TYPE,f3_vals[7]>                          |       52 |        1 | Covered
|
#     | bin <LOAD_TYPE,f3_vals[2]>                       |      436 |        1 | Covered
|
#     | bin <STORE_TYPE,f3_vals[2]>                      |      232 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[0]>                     |       10 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[1]>                     |       18 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[4]>                     |       12 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[5]>                     |       14 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[6]>                     |       12 |        1 | Covered
|
#     | bin <BRANCH_TYPE,f3_vals[7]>                     |       14 |        1 | Covered
|
#     | bin <JALR_TYPE,f3_vals[0]>                       |        4 |        1 | Covered
|
#     | ignore bin no_f3_jal                             |       52 |    -     |
Occurred  |
#     | ignore bin no_f3_lui                             |      536 |    -     |
Occurred  |
#     | ignore bin no_f3_auipc                           |       46 |    -     |
Occurred  |
#     | ignore bin jalr_f1                               |        8 |    -     |
Occurred  |
#     | ignore bin jalr_f2                               |        2 |    -     |
Occurred  |
#     | ignore bin jalr_f3                               |       12 |    -     |
Occurred  |
#     | ignore bin jalr_f4                               |       10 |    -     |
Occurred  |
#     | ignore bin jalr_f5                               |        8 |    -     |
Occurred  |
#     | ignore bin jalr_f6                               |        2 |    -     |
```

```
Occurred  |
#     | ignore bin jalr_f7                                |        8 |    -     |
Occurred  |
#
================================================================================================
#     | TYPE /riscv_coverage/cov_decode                   | 100.000% | 100.000% | Covered
|
#
================================================================================================
#     | INSTANCE <UNNAMED1>                               | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_funct3                  | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | bin ADD_SUB                                       |       46 |        1 | Covered
|
#     | bin SLL                                           |       34 |        1 | Covered
|
#     | bin SLT                                           |       38 |        1 | Covered
|
#     | bin SLTU                                          |       32 |        1 | Covered
|
#     | bin XOR                                           |       28 |        1 | Covered
|
#     | bin SR                                            |       26 |        1 | Covered
|
#     | bin OR                                            |       26 |        1 | Covered
|
#     | bin AND                                           |       36 |        1 | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_funct7                  | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | bin base                                          |      228 |        1 | Covered
|
#     | bin alt                                           |       38 |        1 | Covered
|
#     |---------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_f3_f7                     | 100.000% | 100.000% | Covered
```

```
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | bin <ADD_SUB,base>                          |       28 |        1 | Covered
|
#     | bin <ADD_SUB,alt>                           |       18 |        1 | Covered
|
#     | bin <SLL,base>                              |       34 |        1 | Covered
|
#     | bin <SLT,base>                              |       38 |        1 | Covered
|
#     | bin <SLTU,base>                             |       32 |        1 | Covered
|
#     | bin <XOR,base>                              |       28 |        1 | Covered
|
#     | bin <SR,base>                               |        6 |        1 | Covered
|
#     | bin <SR,alt>                                |       20 |        1 | Covered
|
#     | bin <OR,base>                               |       26 |        1 | Covered
|
#     | bin <AND,base>                              |       36 |        1 | Covered
|
#
==========================================================================================
#     | TYPE /riscv_coverage/cov_registers          | 100.000% | 100.000% | Covered
|
#
==========================================================================================
#     | INSTANCE <UNNAMED1>                         | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rs1               | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | bin zero                                    |      824 |        1 | Covered
|
#     | bin low                                     |      214 |        1 | Covered
|
#     | bin mid                                     |      528 |        1 | Covered
|
#     | bin high                                    |      460 |        1 | Covered
|
#     |---------------------------------------------|----------|----------|--------
```

```
---|
#     | COVERPOINT <UNNAMED1>::cp_rs2                  | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                       |      634 |        1 | Covered
|
#     | bin low                                        |      210 |        1 | Covered
|
#     | bin mid                                        |      728 |        1 | Covered
|
#     | bin high                                       |      454 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd                   | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                       |       98 |        1 | Covered
|
#     | bin low                                        |      278 |        1 | Covered
|
#     | bin mid                                        |     1004 |        1 | Covered
|
#     | bin high                                       |      646 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_rs1_rd                 | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin <zero,zero>                                |       50 |        1 | Covered
|
#     | bin <zero,low>                                 |      108 |        1 | Covered
|
#     | bin <zero,mid>                                 |      408 |        1 | Covered
|
#     | bin <zero,high>                                |      258 |        1 | Covered
|
#     | bin <low,zero>                                 |        4 |        1 | Covered
|
#     | bin <low,low>                                  |       36 |        1 | Covered
|
#     | bin <low,mid>                                  |      108 |        1 | Covered
```

```
|
#     | bin <low,high>                                 |       66 |        1 | Covered
|
#     | bin <mid,zero>                                 |       28 |        1 | Covered
|
#     | bin <mid,low>                                  |       66 |        1 | Covered
|
#     | bin <mid,mid>                                  |      242 |        1 | Covered
|
#     | bin <mid,high>                                 |      192 |        1 | Covered
|
#     | bin <high,zero>                                |       16 |        1 | Covered
|
#     | bin <high,low>                                 |       68 |        1 | Covered
|
#     | bin <high,mid>                                 |      246 |        1 | Covered
|
#     | bin <high,high>                                |      130 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_rs2_rd                 | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin <zero,zero>                                |       16 |        1 | Covered
|
#     | bin <zero,low>                                 |      102 |        1 | Covered
|
#     | bin <zero,mid>                                 |      310 |        1 | Covered
|
#     | bin <zero,high>                                |      206 |        1 | Covered
|
#     | bin <low,zero>                                 |       22 |        1 | Covered
|
#     | bin <low,low>                                  |       24 |        1 | Covered
|
#     | bin <low,mid>                                  |      100 |        1 | Covered
|
#     | bin <low,high>                                 |       64 |        1 | Covered
|
#     | bin <mid,zero>                                 |       36 |        1 | Covered
|
#     | bin <mid,low>                                  |       90 |        1 | Covered
|
#     | bin <mid,mid>                                  |      358 |        1 | Covered
```

```
|
#     | bin <mid,high>                                  |      244 |        1 | Covered
|
#     | bin <high,zero>                                 |       24 |        1 | Covered
|
#     | bin <high,low>                                  |       62 |        1 | Covered
|
#     | bin <high,mid>                                  |      236 |        1 | Covered
|
#     | bin <high,high>                                 |      132 |        1 | Covered
|
#
# ================================================================================
#     | TYPE /riscv_coverage/cov_imm                    | 100.000% | 100.000% | Covered
|
#
# ================================================================================
#     | INSTANCE <UNNAMED1>                             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_imm                   | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                        |      286 |        1 | Covered
|
#     | bin small_pos                                   |      132 |        1 | Covered
|
#     | bin mid_pos                                     |      480 |        1 | Covered
|
#     | bin large_pos                                   |      398 |        1 | Covered
|
#     | bin mid_neg                                     |       76 |        1 | Covered
|
#     | bin large_neg                                   |       84 |        1 | Covered
|
#     | ignore bin small_neg                            |        8 |    -     |
Occurred  |
#
# ================================================================================
#     | TYPE /riscv_coverage/cov_branch                 | 100.000% | 100.000% | Covered
|
#
# ================================================================================
#     | INSTANCE <UNNAMED1>                             | 100.000% | 100.000% | Covered
```

```
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_branch              | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | bin BEQ                                     |       10 |        1 | Covered
|
#     | bin BNE                                     |       18 |        1 | Covered
|
#     | bin BLT                                     |       12 |        1 | Covered
|
#     | bin BGE                                     |       14 |        1 | Covered
|
#     | bin BLTU                                    |       12 |        1 | Covered
|
#     | bin BGEU                                    |       14 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_forward              | 100.000% | 100.000% | Covered
|
#
================================================================================
#     | INSTANCE <UNNAMED1>                         | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_forward_a           | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | bin normal                                  |     1887 |        1 | Covered
|
#     | bin mem                                     |      105 |        1 | Covered
|
#     | bin ex                                      |       34 |        1 | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_forward_b           | 100.000% | 100.000% | Covered
|
#     |---------------------------------------------|----------|----------|--------
---|
#     | bin normal                                  |     1963 |        1 | Covered
```

```
|
#     | bin mem                                          |       12 |        1 | Covered
|
#     | bin ex                                           |       51 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_ab                       | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin <normal,normal>                              |     1830 |        1 | Covered
|
#     | bin <normal,mem>                                 |        8 |        1 | Covered
|
#     | bin <normal,ex>                                  |       49 |        1 | Covered
|
#     | bin <mem,normal>                                 |      102 |        1 | Covered
|
#     | bin <mem,mem>                                    |        3 |        1 | Covered
|
#     | bin <ex,normal>                                  |       31 |        1 | Covered
|
#     | bin <ex,ex>                                      |        2 |        1 | Covered
|
#     | ignore bin rare_ex_mem                           |        1 |    -     |
Occurred  |
#
=================================================================================================
#     | TYPE /riscv_coverage/cov_hazard                  | 100.000% | 100.000% | Covered
|
#
=================================================================================================
#     | INSTANCE <UNNAMED1>                              | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_stall                  | 100.000% | 100.000% | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin no_stall                                     |     1929 |        1 | Covered
|
#     | bin stall                                        |       97 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
```

```
---|
#     | COVERPOINT <UNNAMED1>::cp_flush                | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin no_flush                                   |     1929 |        1 | Covered
|
#     | bin flush                                      |       97 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::cross_stall_flush            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin <no_stall,no_flush>                        |     1929 |        1 | Covered
|
#     | bin <stall,flush>                              |       97 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_redirect              | 100.000% | 100.000% | Covered
|
#
================================================================================
#     | INSTANCE <UNNAMED1>                            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_redirect             | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin no_redirect                                |     1949 |        1 | Covered
|
#     | bin redirect                                   |       77 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_branch_outcome        |  97.222% | 100.000% |
Uncovered |
#
================================================================================
#     | INSTANCE <UNNAMED1>                            |  97.222% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
```

```
---|
#     | COVERPOINT <UNNAMED1>::cp_branch_funct3        | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin BEQ                                        |       10 |        1 | Covered
|
#     | bin BNE                                        |       18 |        1 | Covered
|
#     | bin BLT                                        |       12 |        1 | Covered
|
#     | bin BGE                                        |       14 |        1 | Covered
|
#     | bin BLTU                                       |       12 |        1 | Covered
|
#     | bin BGEU                                       |       14 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_taken                | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin not_taken                                  |       56 |        1 | Covered
|
#     | bin taken                                      |       24 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::branch_outcome_cross         |  91.666% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin <BEQ,not_taken>                            |       10 |        1 | Covered
|
#     | bin <BNE,not_taken>                            |        9 |        1 | Covered
|
#     | bin <BNE,taken>                                |        9 |        1 | Covered
|
#     | bin <BLT,not_taken>                            |        9 |        1 | Covered
|
#     | bin <BLT,taken>                                |        3 |        1 | Covered
|
#     | bin <BGE,not_taken>                            |       10 |        1 | Covered
|
#     | bin <BGE,taken>                                |        4 |        1 | Covered
```

```
|
#     | bin <BLTU,not_taken>                              |         8 |         1 | Covered
|
#     | bin <BLTU,taken>                                  |         4 |         1 | Covered
|
#     | bin <BGEU,not_taken>                              |        10 |         1 | Covered
|
#     | bin <BGEU,taken>                                  |         4 |         1 | Covered
|
#
================================================================================================
#     | TYPE /riscv_coverage/cov_hazard_source          |  93.333% | 100.000% |
Uncovered |
#
================================================================================================
#     | INSTANCE <UNNAMED1>                               |  93.333% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_stall_opocde          | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin load_caused                                   |        97 |         1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_fwd_a_opcode          | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                        |        89 |         1 | Covered
|
#     | bin i_type                                        |        20 |         1 | Covered
|
#     | bin lui                                           |        16 |         1 | Covered
|
#     | bin auipc                                         |         1 |         1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_fwd_b_opcode          |  80.000% | 100.000% |
Uncovered |
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                        |        23 |         1 | Covered
```

```
|
#     | bin i_type                                          |        8 |        1 | Covered
|
#     | bin load                                            |        9 |        1 | Covered
|
#     | bin auipc                                           |        1 |        1 | Covered
|
#     | bin jal                                             |        0 |        1 | Zero
|
#
================================================================================================
#     | TYPE /riscv_coverage/cov_reg_hazard                 | 100.000% | 100.000% | Covered
|
#
================================================================================================
#     | INSTANCE <UNNAMED1>                                 | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd_eq_rs1                 | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | bin no_match                                        |      566 |        1 | Covered
|
#     | bin match                                           |       24 |        1 | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd_eq_rs2                 | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | bin no_match                                        |      258 |        1 | Covered
|
#     | bin match                                           |        8 |        1 | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rs1_eq_rs2                | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | bin no_match                                        |      262 |        1 | Covered
|
#     | bin match                                           |        4 |        1 | Covered
```

```
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_instr_sequence        |  98.639% | 100.000% |
Uncovered |
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                            |  98.639% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_prev_type            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                     |      172 |        1 | Covered
|
#     | bin i_type                                     |      306 |        1 | Covered
|
#     | bin load                                       |      526 |        1 | Covered
|
#     | bin store                                      |      231 |        1 | Covered
|
#     | bin branch                                     |       93 |        1 | Covered
|
#     | bin jal                                        |       73 |        1 | Covered
|
#     | bin lui                                        |      516 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_curr_type            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin r_type                                     |      266 |        1 | Covered
|
#     | bin i_type                                     |      324 |        1 | Covered
|
#     | bin load                                       |      436 |        1 | Covered
|
#     | bin store                                      |      232 |        1 | Covered
|
#     | bin branch                                     |       80 |        1 | Covered
|
#     | bin jal                                        |       52 |        1 | Covered
```

```
|
#     | bin lui                                          |      534 |        1 | Covered
|
#     |--------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::seq_cross                      |  95.918% | 100.000% |
Uncovered |
#     |--------------------------------------------------|----------|----------|--------
---|
#     | bin <r_type,r_type>                              |      142 |        1 | Covered
|
#     | bin <r_type,i_type>                              |        7 |        1 | Covered
|
#     | bin <r_type,load>                                |        5 |        1 | Covered
|
#     | bin <r_type,store>                               |        2 |        1 | Covered
|
#     | bin <r_type,branch>                              |        6 |        1 | Covered
|
#     | bin <r_type,jal>                                 |        2 |        1 | Covered
|
#     | bin <r_type,lui>                                 |        6 |        1 | Covered
|
#     | bin <i_type,r_type>                              |       10 |        1 | Covered
|
#     | bin <i_type,i_type>                              |      269 |        1 | Covered
|
#     | bin <i_type,load>                                |        2 |        1 | Covered
|
#     | bin <i_type,store>                               |        5 |        1 | Covered
|
#     | bin <i_type,branch>                              |        4 |        1 | Covered
|
#     | bin <i_type,jal>                                 |        2 |        1 | Covered
|
#     | bin <i_type,lui>                                 |       11 |        1 | Covered
|
#     | bin <load,r_type>                                |       87 |        1 | Covered
|
#     | bin <load,i_type>                                |       12 |        1 | Covered
|
#     | bin <load,load>                                  |      415 |        1 | Covered
|
#     | bin <load,store>                                 |        3 |        1 | Covered
|
#     | bin <load,jal>                                   |        1 |        1 | Covered
```

|
| bin <load,lui> | 5 | 1 | Covered
|
| bin <store,r_type> | 2 | 1 | Covered
|
| bin <store,i_type> | 3 | 1 | Covered
|
| bin <store,store> | 216 | 1 | Covered
|
| bin <store,branch> | 2 | 1 | Covered
|
| bin <store,jal> | 3 | 1 | Covered
|
| bin <store,lui> | 3 | 1 | Covered
|
| bin <branch,r_type> | 7 | 1 | Covered
|
| bin <branch,i_type> | 7 | 1 | Covered
|
| bin <branch,load> | 4 | 1 | Covered
|
| bin <branch,store> | 3 | 1 | Covered
|
| bin <branch,branch> | 47 | 1 | Covered
|
| bin <branch,jal> | 4 | 1 | Covered
|
| bin <branch,lui> | 16 | 1 | Covered
|
| bin <jal,r_type> | 6 | 1 | Covered
|
| bin <jal,i_type> | 11 | 1 | Covered
|
| bin <jal,load> | 4 | 1 | Covered
|
| bin <jal,store> | 1 | 1 | Covered
|
| bin <jal,branch> | 6 | 1 | Covered
|
| bin <jal,jal> | 29 | 1 | Covered
|
| bin <jal,lui> | 10 | 1 | Covered
|
| bin <lui,r_type> | 3 | 1 | Covered
|
| bin <lui,i_type> | 9 | 1 | Covered

```
|
#     | bin <lui,load>                                  |        3 |        1 | Covered
|
#     | bin <lui,store>                                 |        1 |        1 | Covered
|
#     | bin <lui,branch>                                |       11 |        1 | Covered
|
#     | bin <lui,jal>                                   |        7 |        1 | Covered
|
#     | bin <lui,lui>                                   |      470 |        1 | Covered
|
#
# ------------------------------------------------------------------------------------
#     | TYPE /riscv_coverage/cov_data_dep               | 100.000% | 100.000% | Covered
|
#
# ====================================================================================
#     | INSTANCE <UNNAMED1>                             | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_raw_rs1               | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin no_dep                                      |     1894 |        1 | Covered
|
#     | bin dep                                         |      130 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_raw_rs2               | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin no_dep                                      |     1977 |        1 | Covered
|
#     | bin dep                                         |       47 |        1 | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_raw_both              | 100.000% | 100.000% | Covered
|
#     |-------------------------------------------------|----------|----------|--------
---|
#     | bin no_dep                                      |     2019 |        1 | Covered
```

```
|
#     | bin dep                                              |        5 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_corner                      | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                                  | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_rd_zero                    | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------------|----------|----------|--------
---|
#     | bin non_zerp                                         |      776 |        1 | Covered
|
#     | bin rd_zero                                          |       26 |        1 | Covered
|
#     |------------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_redirect_after_stall       | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------------|----------|----------|--------
---|
#     | bin no                                               |     2026 |        1 | Covered
|
#     | ignore bin impossible                                |        0 |    -     | Zero
|
#     |------------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_branch_with_fwd            | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------------|----------|----------|--------
---|
#     | bin no_fwd                                           |       56 |        1 | Covered
|
#     | bin has_fwd                                          |       24 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_memory                      |  83.333% | 100.000% |
Uncovered |
#
```

```
=============================================================================================
#     | INSTANCE <UNNAMED1>                                |  83.333% | 100.000% |
Uncovered |
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_load_addr                | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin low_addr                                       |       58 |        1 | Covered
|
#     | bin mid_addr                                       |      180 |        1 | Covered
|
#     | bin high_addr                                      |      198 |        1 | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_store_addr               | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin low_addr                                       |       22 |        1 | Covered
|
#     | bin mid_addr                                       |       92 |        1 | Covered
|
#     | bin high_addr                                      |      118 |        1 | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_store_then_load          |  50.000% | 100.000% |
Uncovered |
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin no                                             |     2026 |        1 | Covered
|
#     | bin yes                                            |        0 |        1 | Zero
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_alu_result                |  85.000% | 100.000% |
Uncovered |
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                                |  85.000% | 100.000% |
Uncovered |
#     |----------------------------------------------------|----------|----------|--------
```

```
---|
#     | COVERPOINT <UNNAMED1>::cp_shamt                |  80.000% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                       |        0 |        1 | Zero
|
#     | bin low                                        |       26 |        1 | Covered
|
#     | bin mid                                        |       28 |        1 | Covered
|
#     | bin high                                       |        4 |        1 | Covered
|
#     | bin max                                        |        2 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_shamt_imm            |  75.000% | 100.000% |
Uncovered |
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin zero                                       |        0 |        1 | Zero
|
#     | bin low                                        |       18 |        1 | Covered
|
#     | bin mid                                        |       40 |        1 | Covered
|
#     | bin high                                       |       16 |        1 | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_slt_result           | 100.000% | 100.000% | Covered
|
#     |------------------------------------------------|----------|----------|--------
---|
#     | bin low                                        |        6 |        1 | Covered
|
#     | bin mid                                        |       26 |        1 | Covered
|
#     | bin high                                       |       36 |        1 | Covered
|
#
================================================================================
#     | TYPE /riscv_coverage/cov_branch_direction      |  66.666% | 100.000% |
Uncovered |
#
```

```
=============================================================================================
#     | INSTANCE <UNNAMED1>                                |  66.666% | 100.000% |
Uncovered |
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_direction                |  50.000% | 100.000% |
Uncovered |
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin forward                                        |       80 |        1 | Covered
|
#     | bin backward                                       |        0 |        1 | Zero
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_taken_dir                | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin not_taken                                      |       56 |        1 | Covered
|
#     | bin taken                                          |       24 |        1 | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | CROSS <UNNAMED1>::direction_outcome                |  50.000% | 100.000% |
Uncovered |
#     |----------------------------------------------------|----------|----------|--------
---|
#     | bin <forward,not_taken>                            |       56 |        1 | Covered
|
#     | bin <forward,taken>                                |       24 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_flush_source             | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                                | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_redirect_source          | 100.000% | 100.000% | Covered
|
#     |----------------------------------------------------|----------|----------|--------
```

```
---|
#     | bin branch                                          |       24 |        1 | Covered
|
#     | bin jal                                             |       26 |        1 | Covered
|
#     | bin jalr                                            |       27 |        1 | Covered
|
#
=============================================================================================
#     | TYPE /riscv_coverage/cov_writeback                  | 100.000% | 100.000% | Covered
|
#
=============================================================================================
#     | INSTANCE <UNNAMED1>                                 | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | COVERPOINT <UNNAMED1>::cp_wb_source                 | 100.000% | 100.000% | Covered
|
#     |-----------------------------------------------------|----------|----------|--------
---|
#     | bin alu_wb[19]                                      |      302 |        1 | Covered
|
#     | bin alu_wb[23]                                      |       44 |        1 | Covered
|
#     | bin alu_wb[51]                                      |      250 |        1 | Covered
|
#     | bin alu_wb[55]                                      |      526 |        1 | Covered
|
#     | bin alu_wb[103]                                     |       52 |        1 | Covered
|
#     | bin alu_wb[111]                                     |       52 |        1 | Covered
|
#     | bin mem_wb                                          |      414 |        1 | Covered
|
#
=============================================================================================
```