8-Bit Computer-ALU

ALU Team:2

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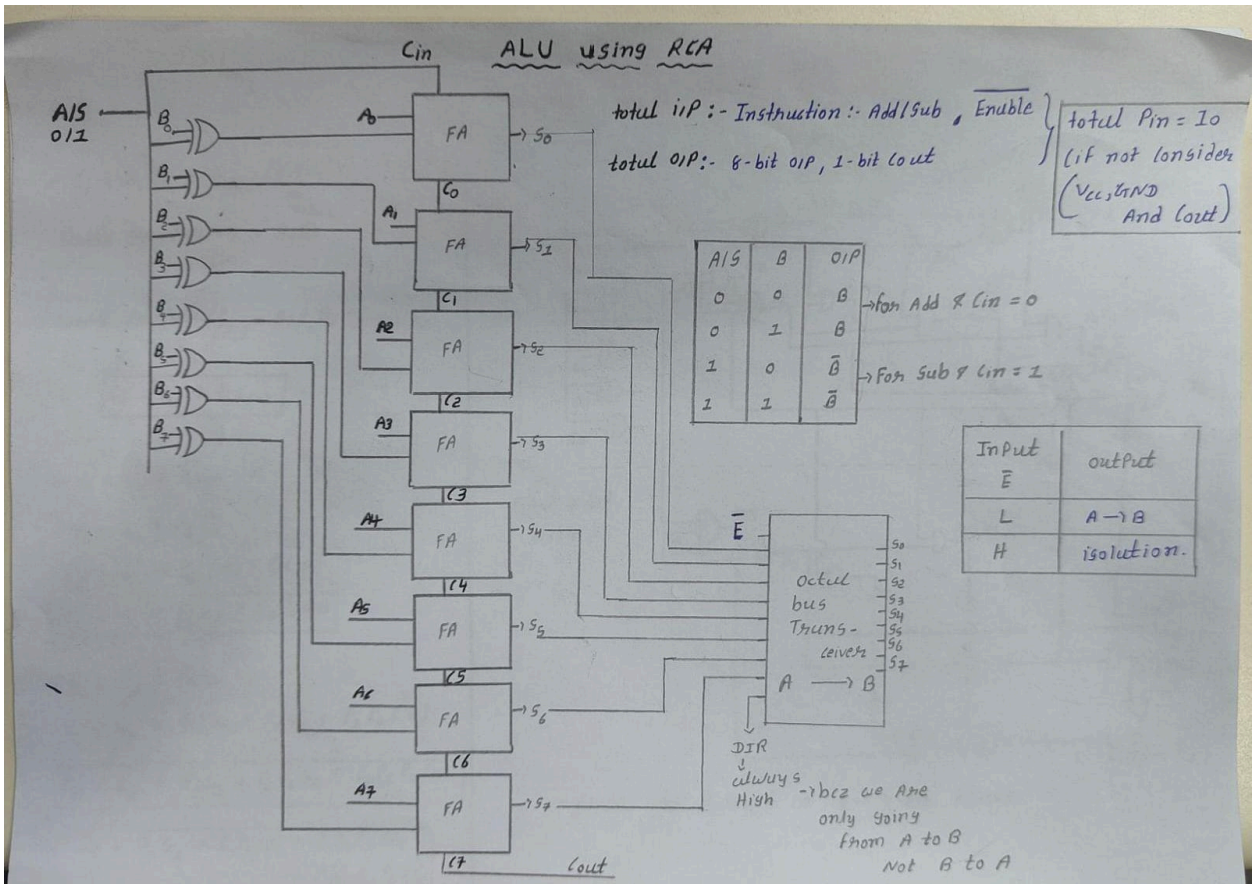
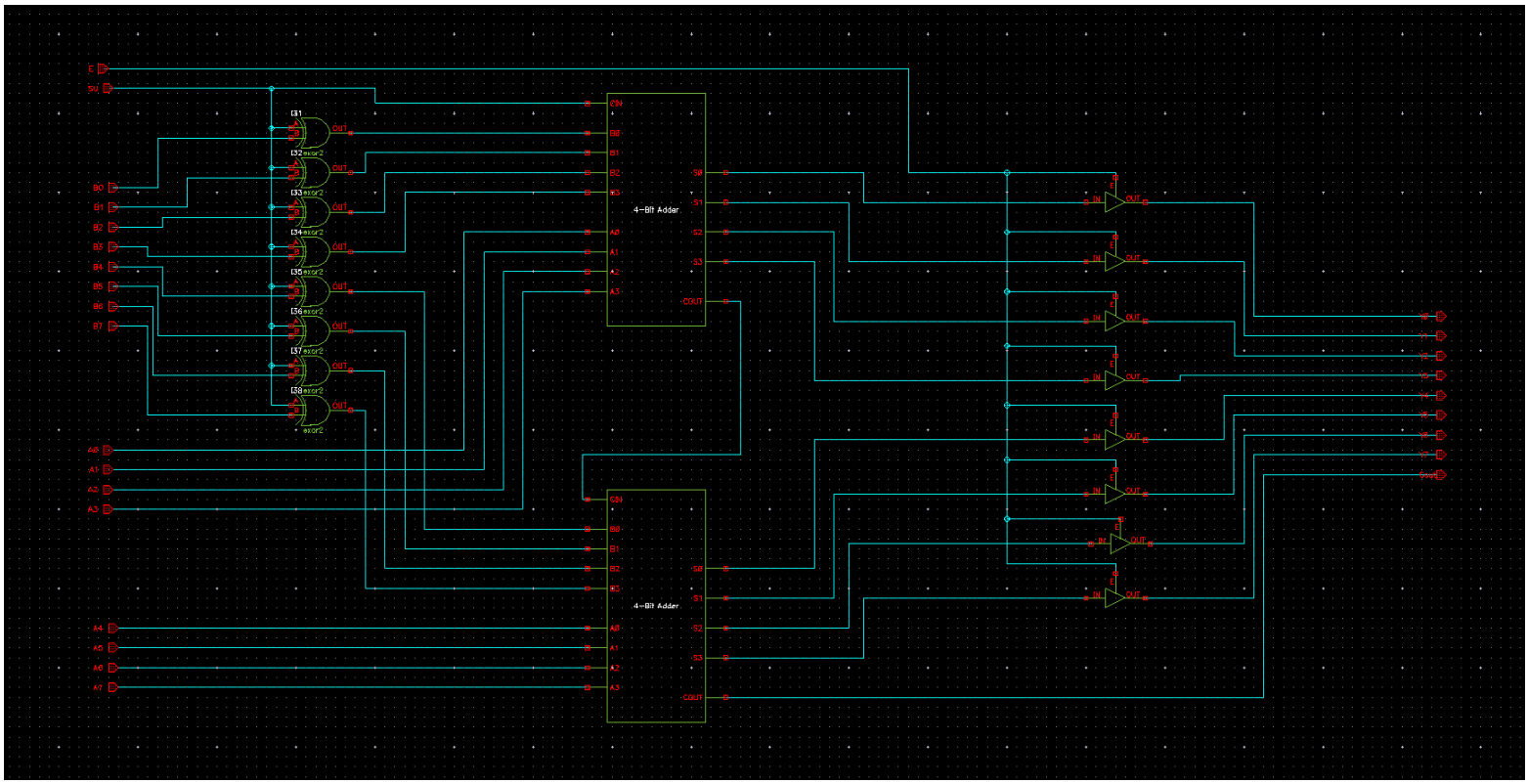
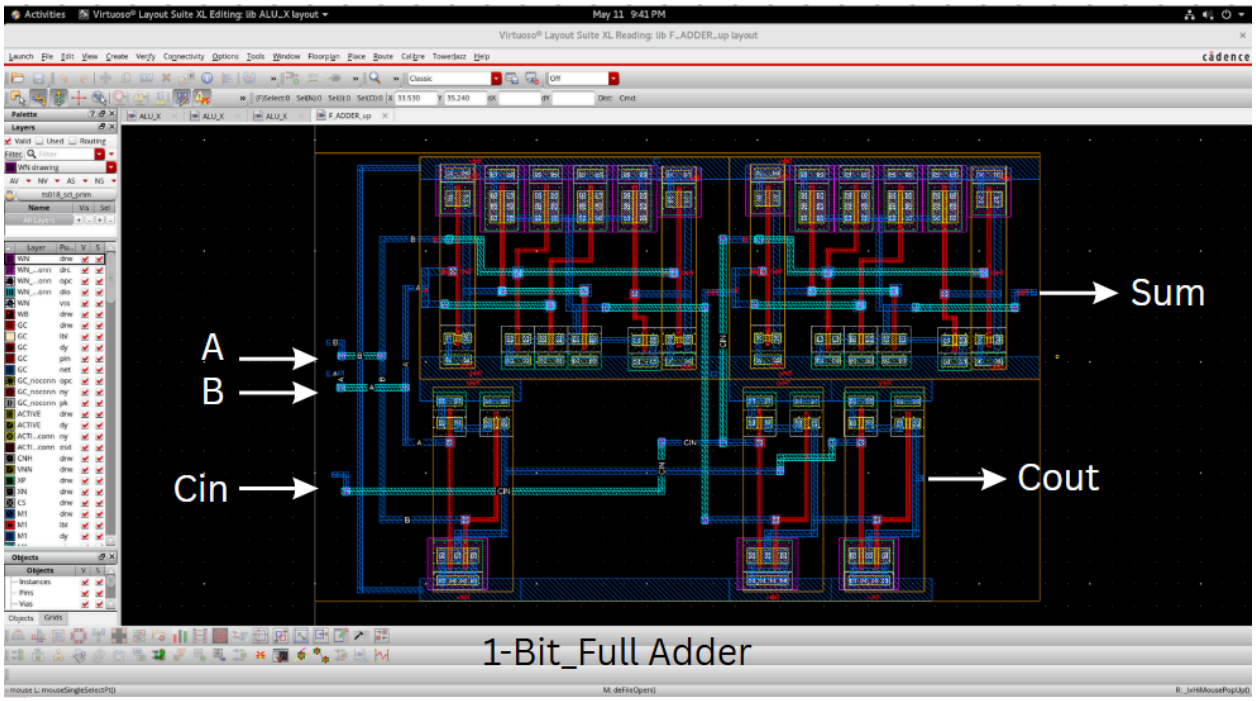
Schematic of ALU:



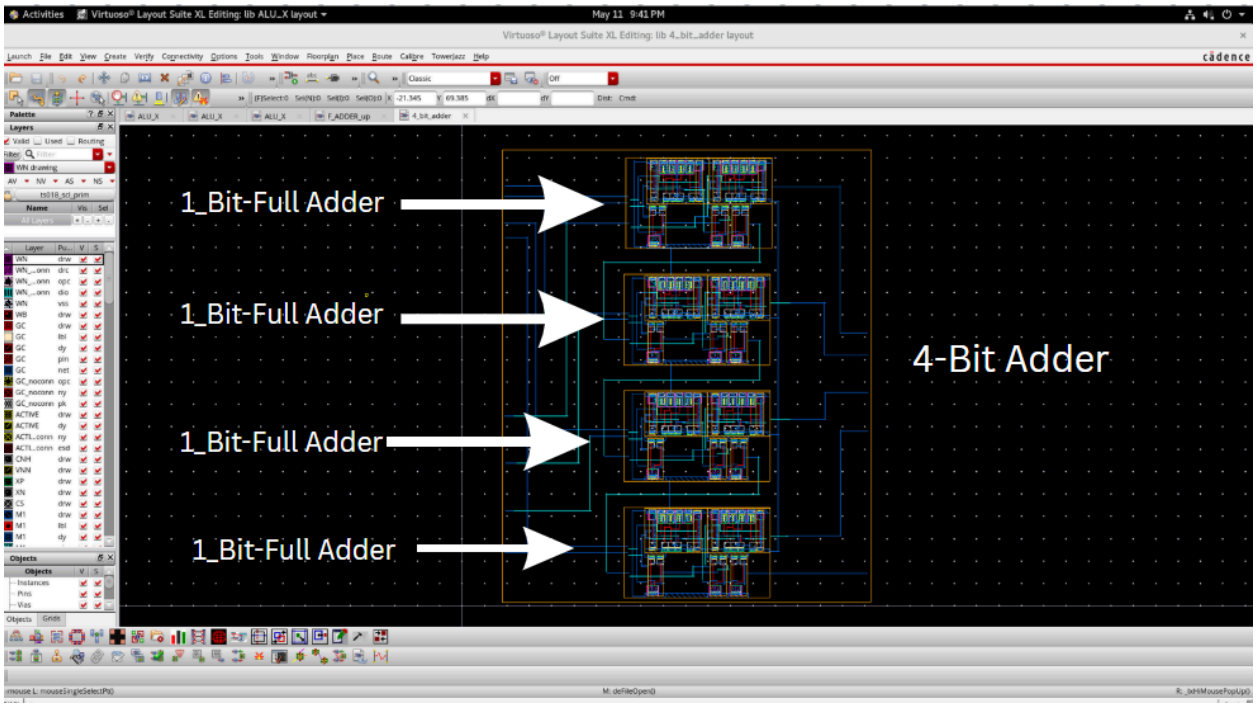


Layout of ALU:

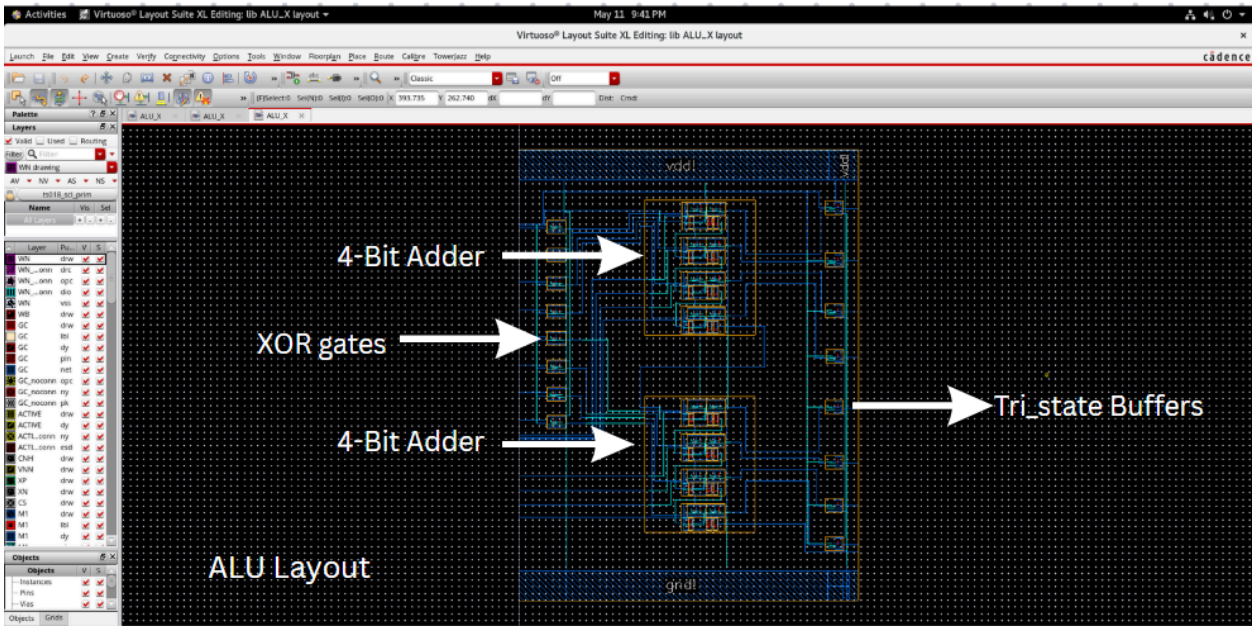
In Layout, first of all, we make the layout of a 1-bit full adder, and then we make the layout of a 4-bit full adder, and then we make the final layout of the ALU.



This is the Layout of a 1-bit Full adder that is shown above. In this, the input is A, B, and Cin on the left side, and the output is Sum and Cout on the right side.

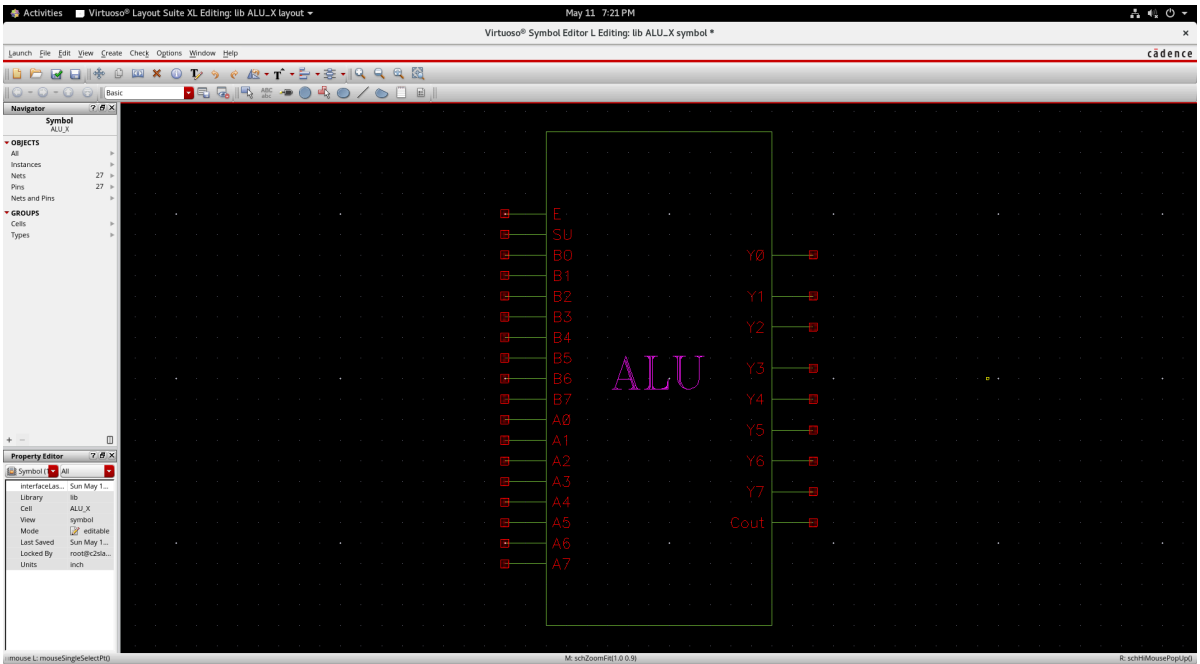


This is the layout of a 4-bit Full adder that is shown above. In this, we use the four 1-bit Full adders to design it.



This is the final Layout of ALU. In this, we use two 4-bit adders to implement it. Also, there are XOR gates and Tri-state Buffers in the layout of the ALU.

Input/Output Pins:



This is the symbol of ALU, and in this :

E: Enable signal for the ALU. (Active High)

SU: Select signal – 0 for addition, 1 for subtraction.

A0–A7: 8-bit input A.

B0–B7: 8-bit input B.

Y0–Y7: 8-bit output result.

Cout: Carry-out (for addition) or borrow (for subtraction).

Timings and Delay :

● After performing post-layout simulation, the propagation delay of the ALU was found to be 0.68425 ns.
● The maximum current the ALU can provide is 535 μA, and it can charge a 50-pF capacitor in 0.2 μs.