report5

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Target Specifications:

- Output Voltage = 0.5V ± 1%
- Supply Voltage = 1.8V ± 10%
- Power Consumption < 1mW
- Temperature Range: −40 °C to 125 °C

Characteristics:

Mosfets:

- Model: TSMC 65nm GP nch,pch.

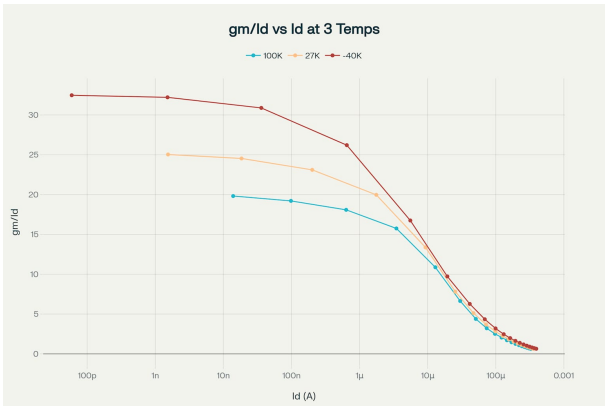

Figure 1: NMOS characteristics

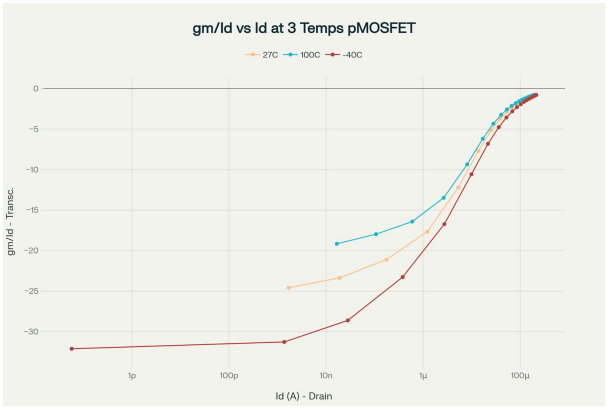

Figure 2: PMOS characteristics

Diodes:

- Model: TSMC 65nm `ndio_25`
- Non-ideality factor (η): 0.84.
- CTAT slope: -1.72mv/C .

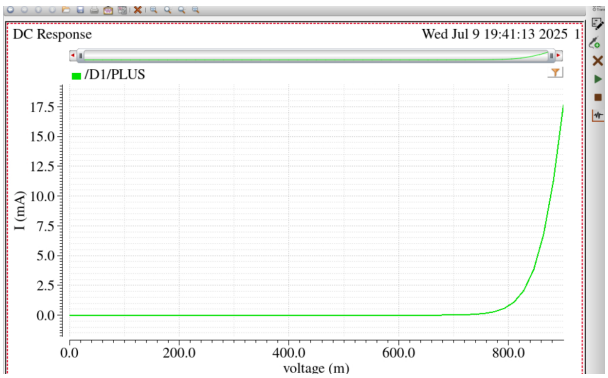

Figure 3: Diode characteristics

Bias Currents:

$$(I_{\text{total}})_{\max} = \frac{1000\,\mu\text{W}}{1.8\,\text{V}} = 566.6\,\mu\text{A}$$

Current Division

- Opamp used in regulated cascode: $25\,\mu\text{A} + 5\,\mu\text{A} = 30\,\mu\text{A}$
- Regular Opamp: $45\,\mu\text{A} + 5\,\mu\text{A} = 50\,\mu\text{A}$
- Bias stage: $5\,\mu\text{A}$
- Branch current in core bandgap: $100\,\mu\text{A} + 100\,\mu\text{A} + 100\,\mu\text{A} = 300\,\mu\text{A}$

Design Equations

- $$\begin{aligned} \frac{\frac{k}{q}\ln(n)\eta}{R_1} &= \frac{0.00174}{R_2} \\ \Rightarrow \frac{R_2}{R_1} &\approx 11.58 \end{aligned} \tag{1}$$
- $$100\mu = \frac{\frac{k}{q}(300)\ln(n)\eta}{R_1} + \frac{0.709}{R_2} \tag{2}$$

Solving:

$$R_1 = 1063.76\ \Omega, \quad R_2 \approx 12,310\ \Omega$$

$$\begin{aligned} R_3 &= \frac{0.5}{100\mu A} \\ &= 5k\ \Omega \end{aligned}$$

Bandgap Reference:

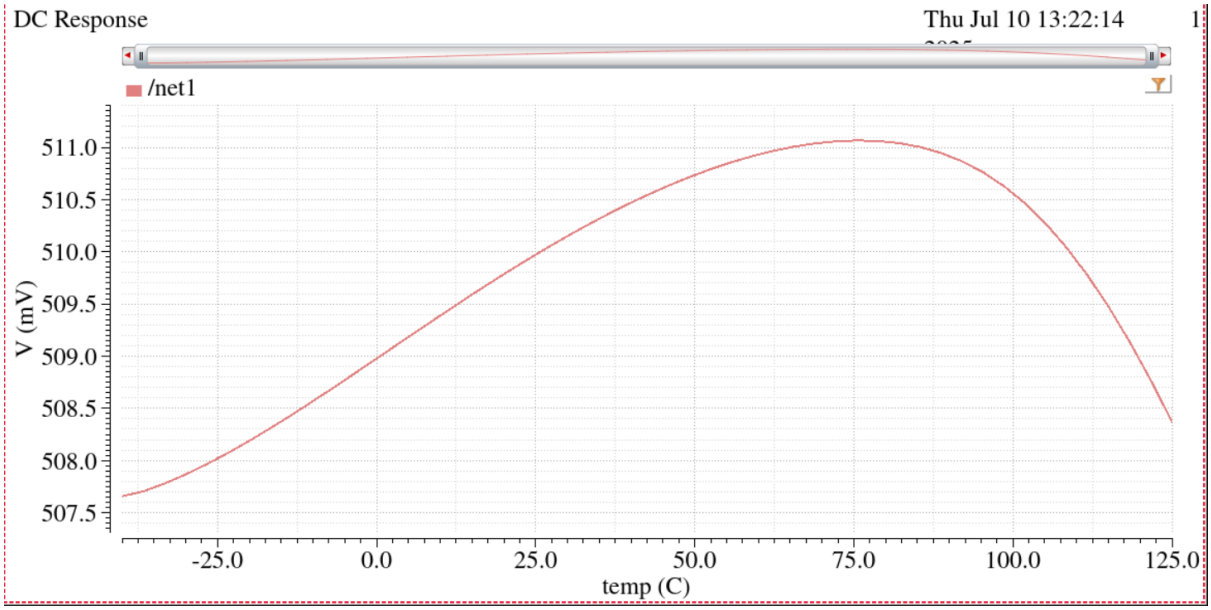

Figure 4: Output voltage

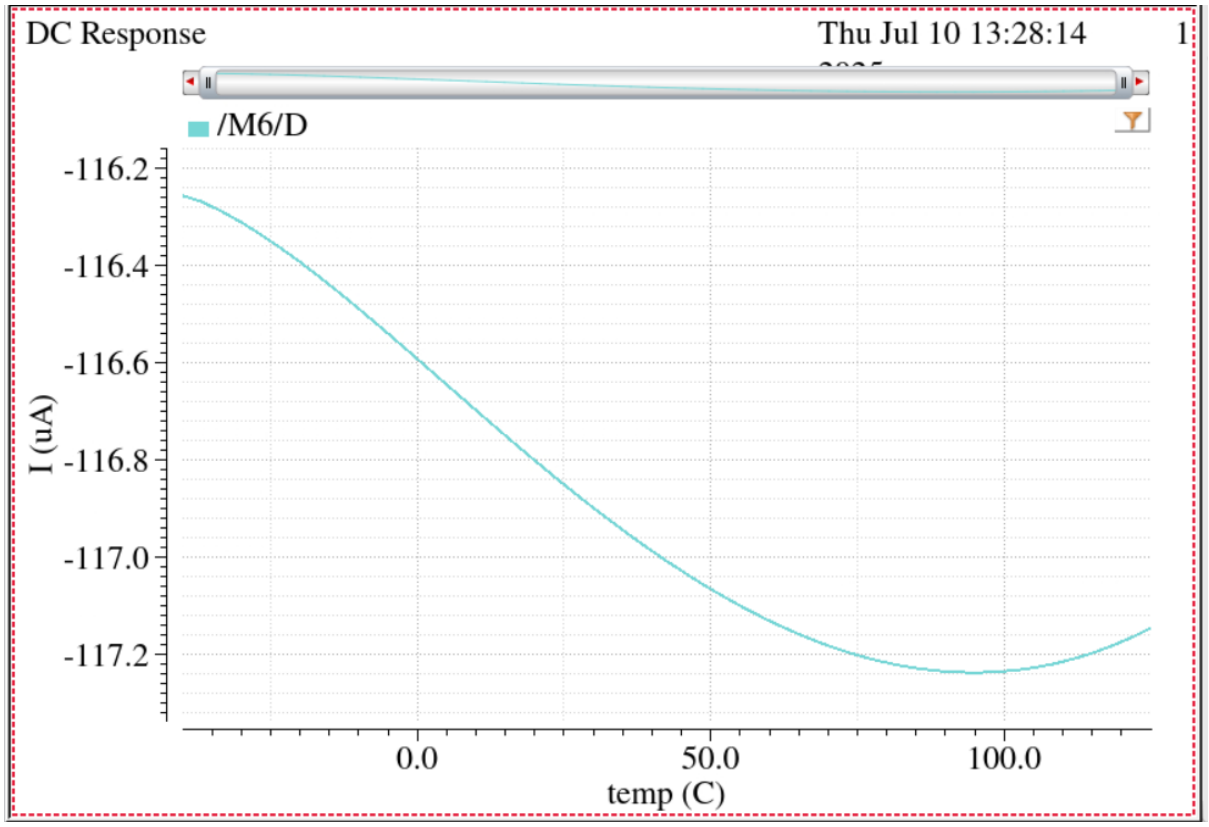

Figure 5: ZTAT current

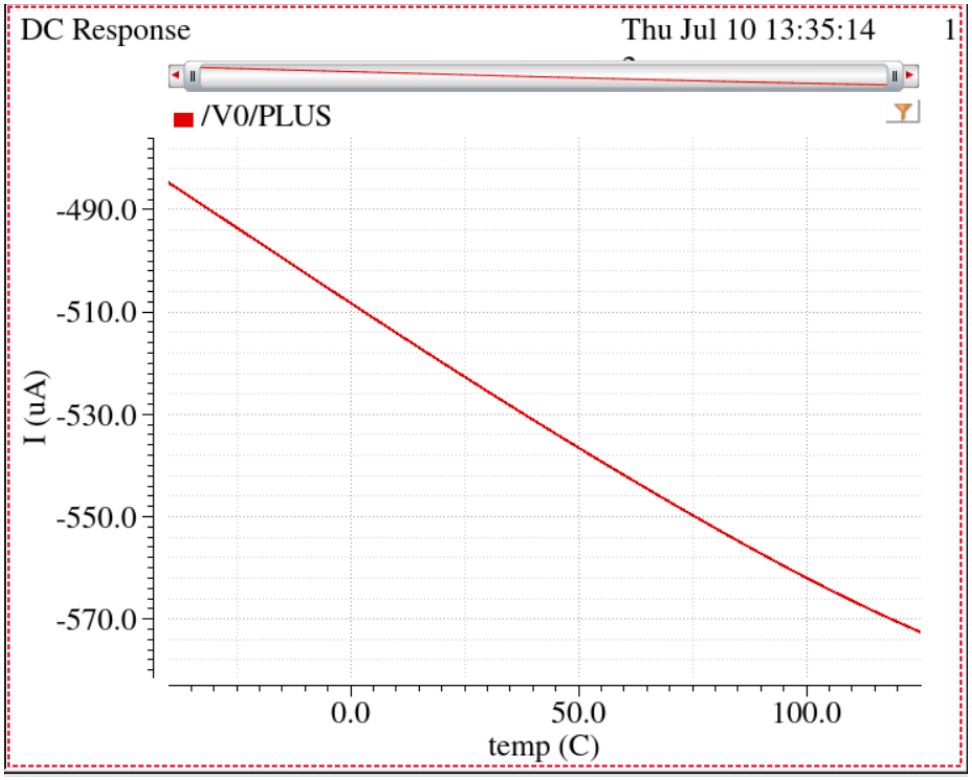

Figure 6: total current

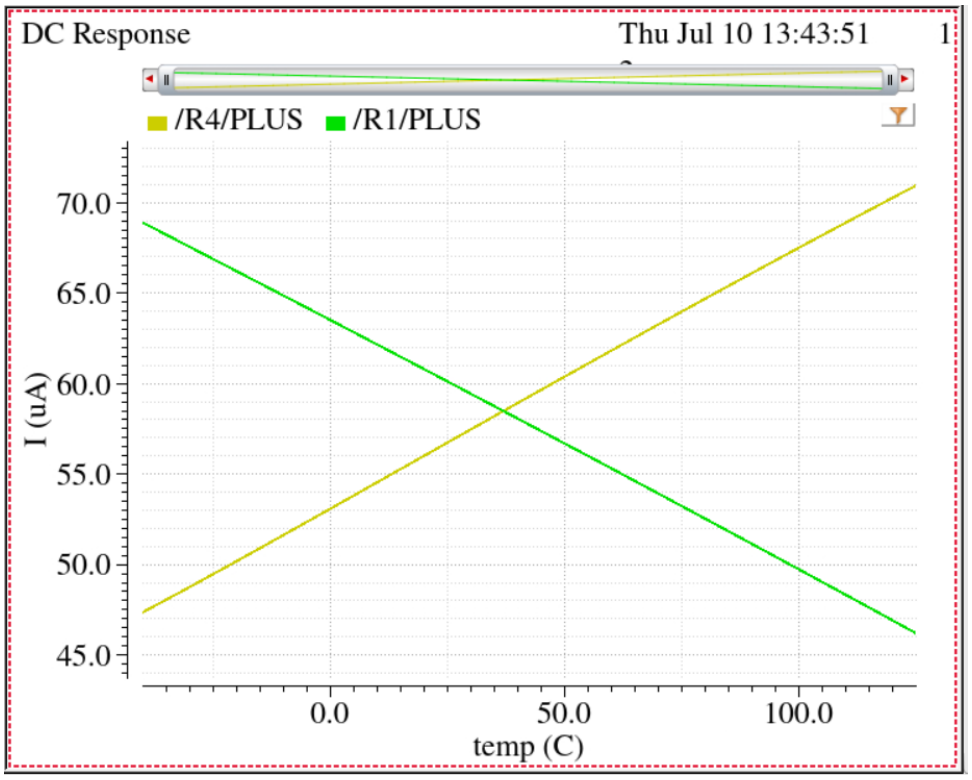

Figure 7: CTAT and PTAT current

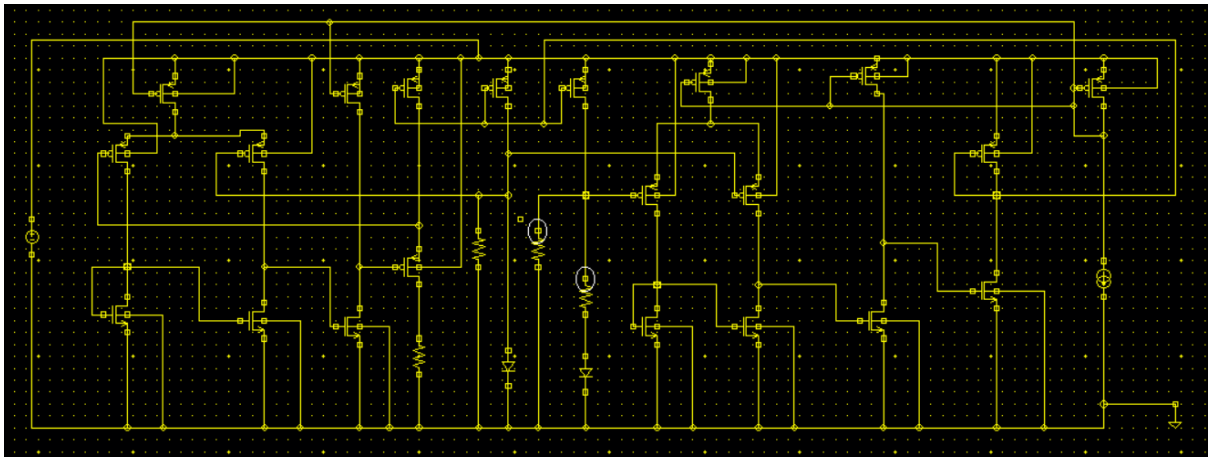

Figure 8: bandgap circuit

Observations:

- Reference voltage at 27C: 0.510mV.
- Maximum current used: 572.5 uA.