REPORT-2

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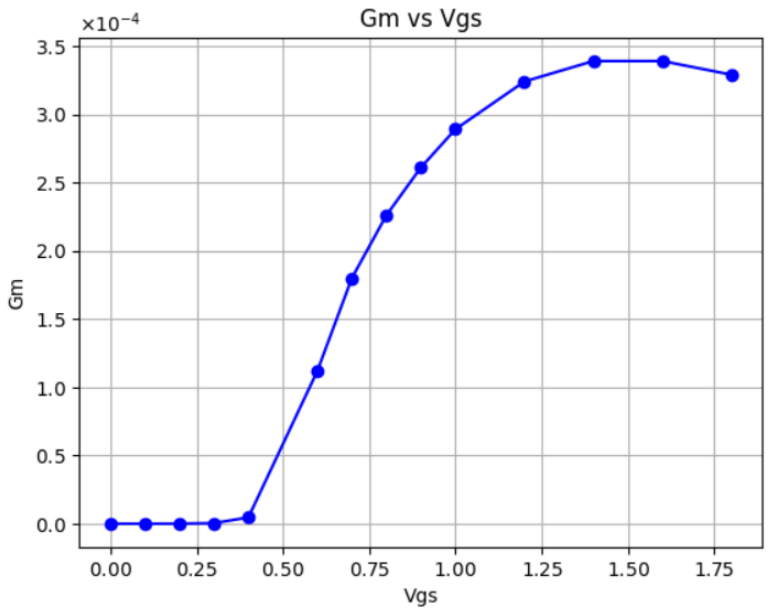
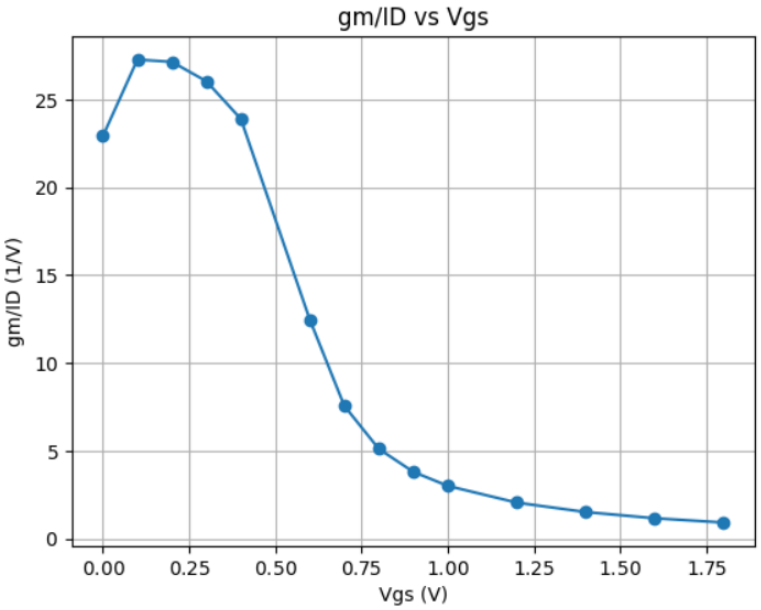
Contents:

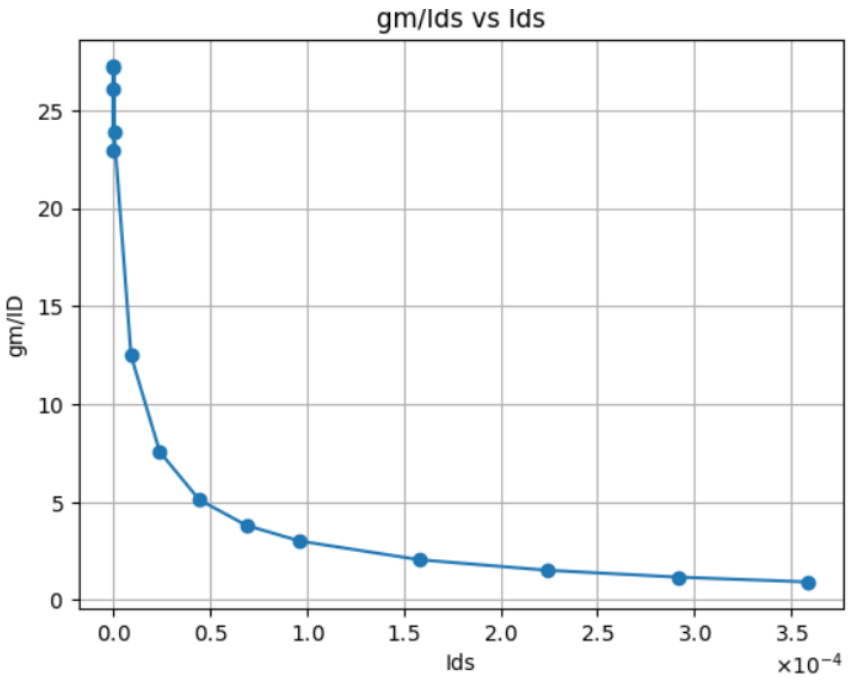
MOS Characterization :

- Gm/Id parameter is used as a key design parameter because it is independent of the size of the MOSFET and the range of values is limited to **1-30**.
- More suited for small channel mosfets as well.

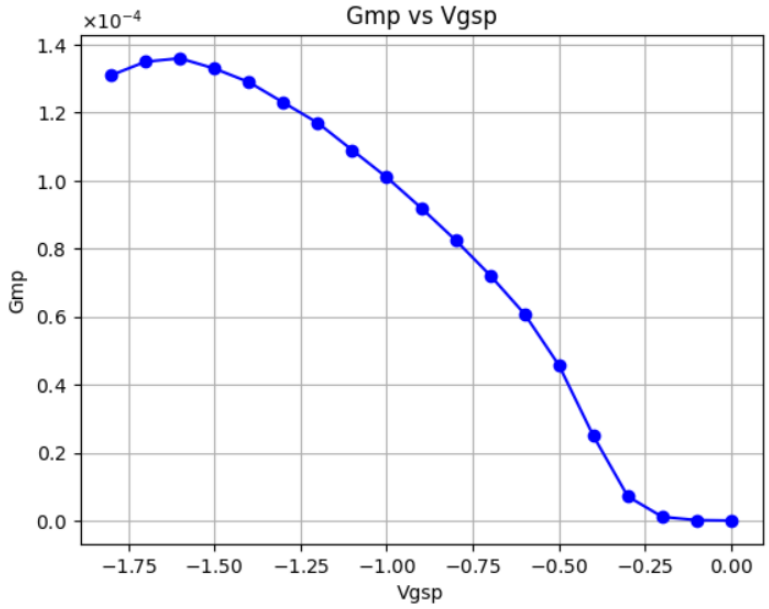
TSMC 180nm Nmos:

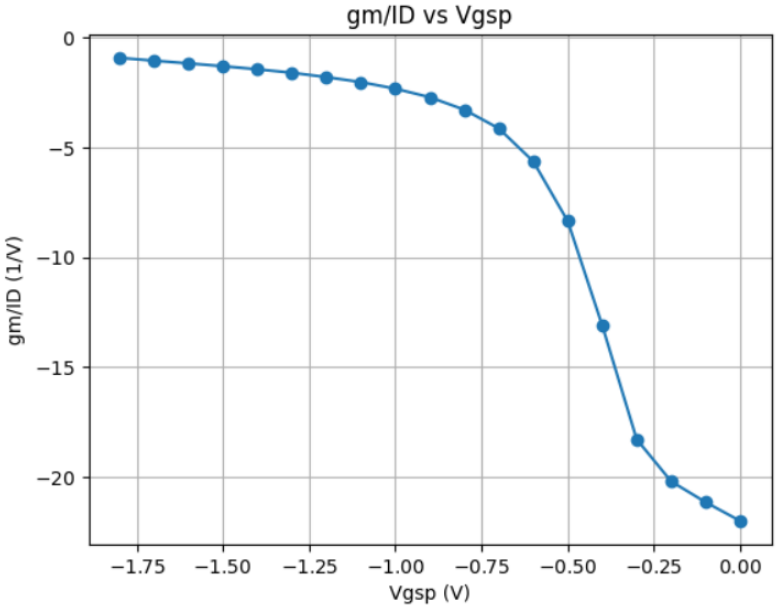


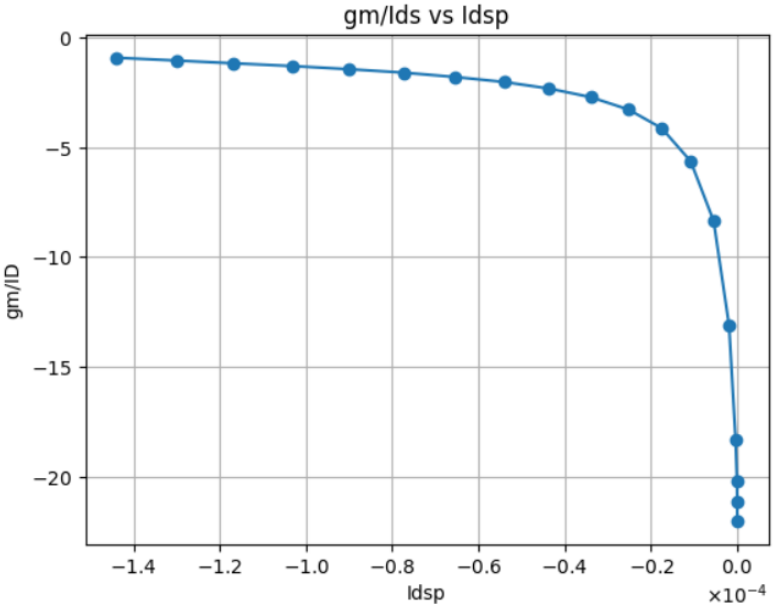

gm/ID vs Vgs
gm/ID (1/V)
Vgs (V)
0
5
10
15
20
25
0.00
0.25
0.50
0.75
1.00
1.25
1.50
1.75

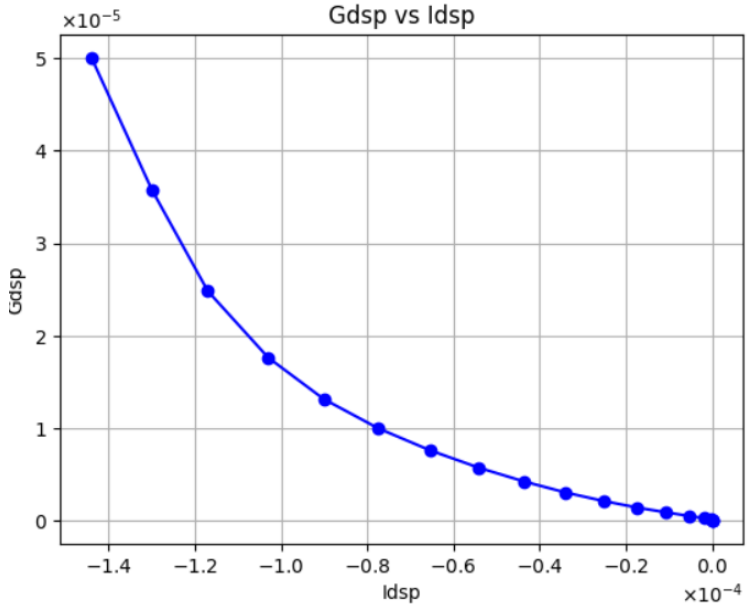

gm/Ids vs Ids
gm/ID
Ids
×10⁻⁴
0
5
10
15
20
25
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5

TSMC 180nm Pmos:






gm/Ids vs Idsp
gm/ID
0
−5
−10
−15
−20
−1.4
−1.2
−1.0
−0.8
−0.6
−0.4
−0.2
0.0
Idsp
×10−4


Gdsp vs Idsp
×10−5
Gdsp
5
4
3
2
1
0
−1.4
−1.2
−1.0
−0.8
−0.6
−0.4
−0.2
0.0
Idsp
×10−4

Opamp Design:

Bias current:

$$f_{\text{UGB}} = \frac{g_{m_1}}{2\pi C_c} = \frac{\left(\frac{g_{m_1}}{I_D}\right) \cdot I_D}{2\pi C_c}$$

- Assume the Bandwidth needed for the Opamp used in bandgap reference circuit is **40 MHz**.
- To have a higher gain the mosfets are to be biased to operate in moderate inversion ie. **Gm/Id between 15 to 20** for the input Nmos.
- Let the miller capacitor be 1pF.

$$I_d \approx \frac{40 \times 10^6 \times 2\pi \times 10^{-12}}{15}$$
$$\approx 16.75\mu A$$
$$I_{\text{tail}} = 2 \times I_d$$
$$\approx 33.5\mu A$$

- Acceptable Gm/Id range for **Tail Mosfet**: **17–23**. This corresponds to weak-to-moderate inversion, providing higher output resistance (more accurate differential stage) and lower power consumption.
- From the plots above the preferred Ids per unit width :

$$\approx 1.5625\mu A$$

- No. of fingers:

$$m \approx \frac{33.5\mu}{1.5625\mu} = 22$$

1. Observed Tail Current $28.9\mu A$.
2. Observed Gm/Id = 22.076 .
3. No.of fingers used 30.

- For nmos active load at bias stage Gm/Id preferred : 17-20.
- Current per unit width is the same as that of the tail: $1.5625\,\mu A$. Thus for $m = 3$, $I_{\text{bias}} \approx 3 \times 1.5625\,\mu A \approx 4.6875\,\mu A$.
- The bias current used is $\boxed{\mathbf{5}\,\mu\mathbf{A}}$.

Mosfet Sizing:

1. 2nd Stage (Method -1):

   - The DC gain obtained from 1st stage designed is $\approx 56dB$.Gain needed from the 2nd stage :$\approx 30dB$.

$$
\begin{aligned}
A_v &= 30\,\text{dB} \\
\frac{g_{m10}}{g_{ds10}+g_{ds11}} &\approx 3.32 \\
\left(\frac{g_{m10}}{I_D}\right) I_D &\approx 3.32 \times (g_{ds10}+g_{ds11}) \\
I_D &\approx \frac{3.32 \times 10^{-4}}{15} \\
&\approx 23\,\mu\text{A} \\
\text{current per finger} &= 1.5625\,\mu\text{A} \\
\text{No. of fingers for 2nd stage active load} &\approx \frac{23}{1.5625} \\
&\approx 15
\end{aligned}
$$

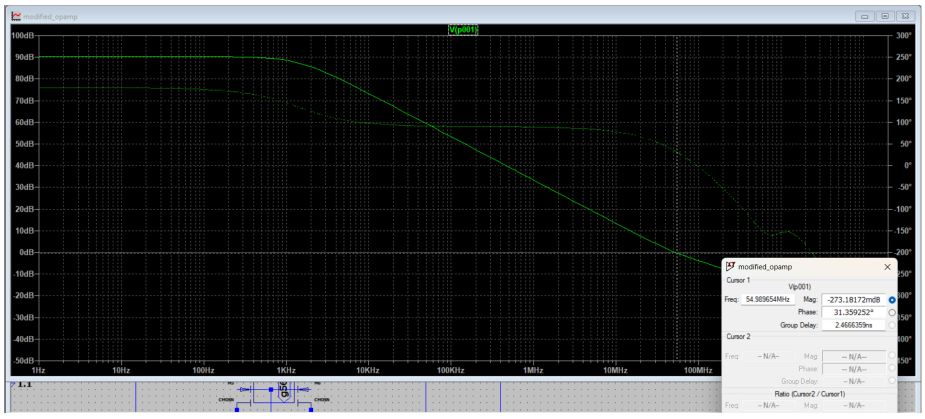


Figure 1: DC gain achieved but PM is only 30 degrees

   - This is because of lower value of Gm10, the Zero is at lower frequency.To push the zero away a zero-canceling resistor of value 2K is added.

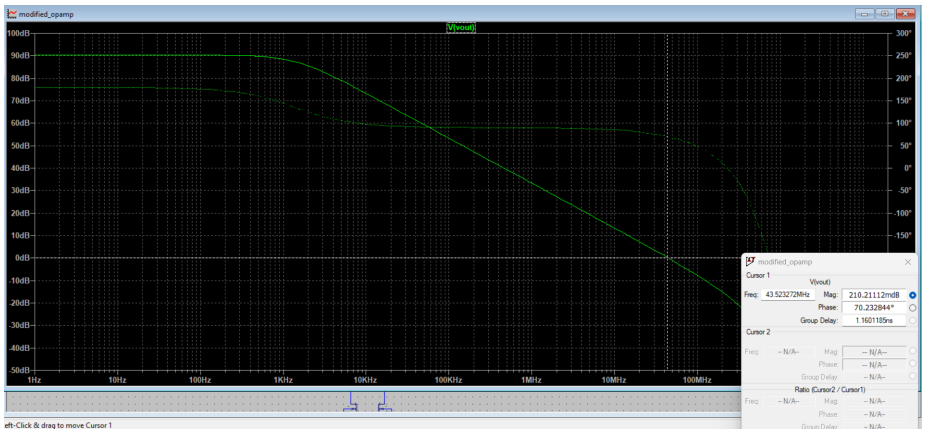


Figure 2: PM after adding Zero cancelling resistor = 70 degrees.

- **disadvantages**: Presence of a resistor, lower current at 2nd stage (Very poor Slew Rate).

2. 2nd Stage (Method -2):

- Instead of adding a zero-cancelling resistor,we can increase the current in the 2nd stage, maintaining the Gm/Id ratio the same(DC gain depends on Gm/Id), to increase Gm10 and push Zero away until PM is 70 degrees.
- Observed Current is 286 μA current.

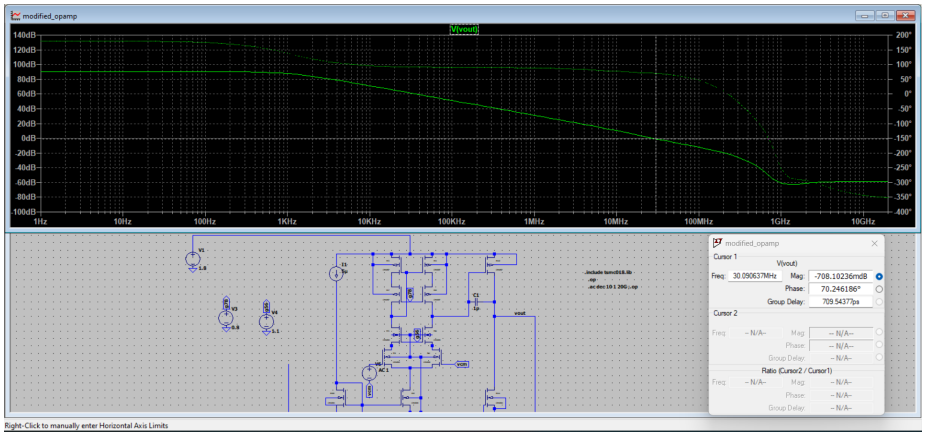


Figure 3: 2-nd stage biased from Method -2

Diode and Resistors:

- We can assume Vref to be 1.11v and plot diode characteristics at an average temperature of 40 degrees.

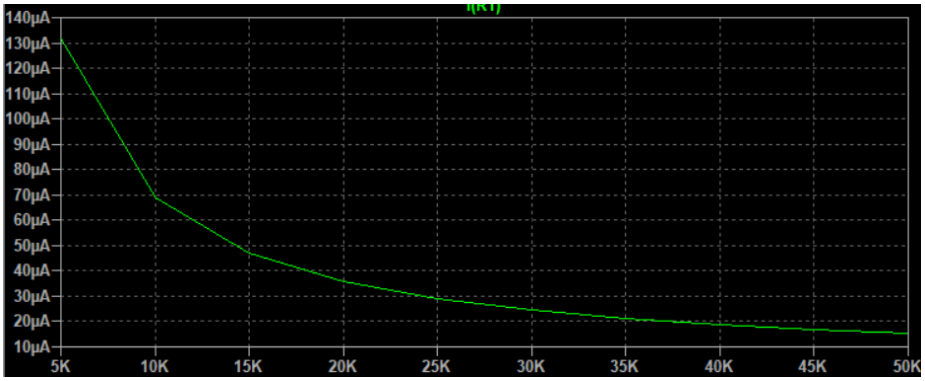


Figure 4: Current in 1N4148 vs R2

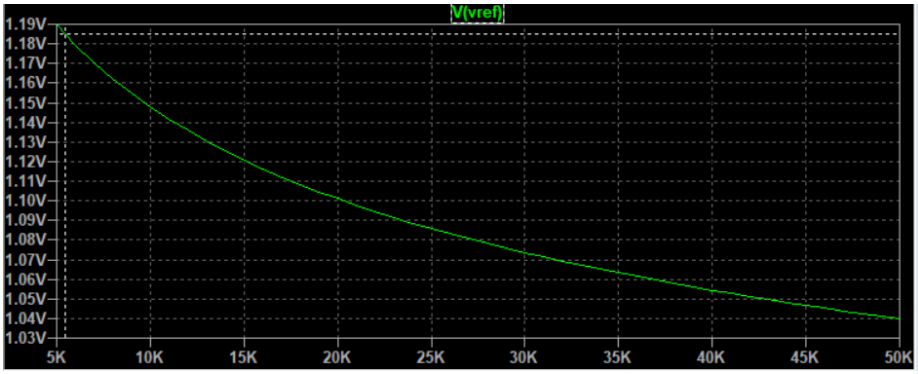


Figure 5: V_{ref} obtained vs R_2 at 40°C

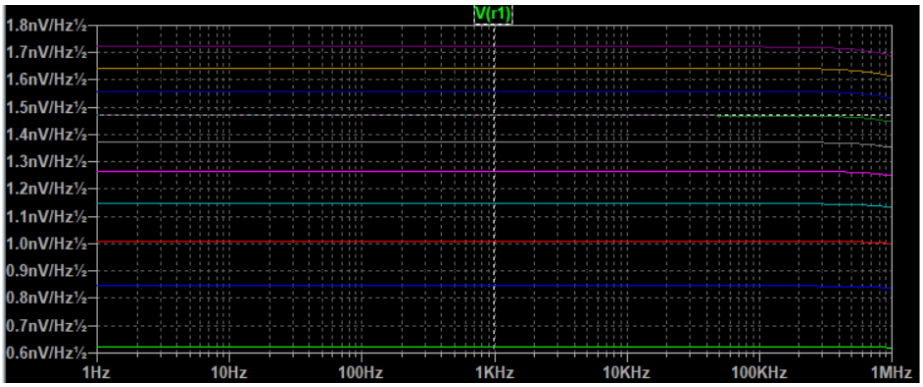


Figure 6: noise PSD vs R2

- There is a trade-off between Power consumed, noise and Vref obtained.
- So to balance the effects, **R2 is taken around 20k** which corresponds to current of about $40\mu A$.

Current Mirrors:

- Operate in weak to moderate inversion, leading to higher output resistance and better current matching.Required Gm/Id:17-22.
- From the g_m/I_D vs Ids plot of PMOS, the current per unit width is approximately $1.25\,\mu A$.
- No.of fingers:

$$m \approx \frac{40\mu}{1.25\mu} = 32$$

Bandgap reference voltage generator:

- Temperature Coefficient of resistors used: 0.0001 ppm/C (only linear term considered).

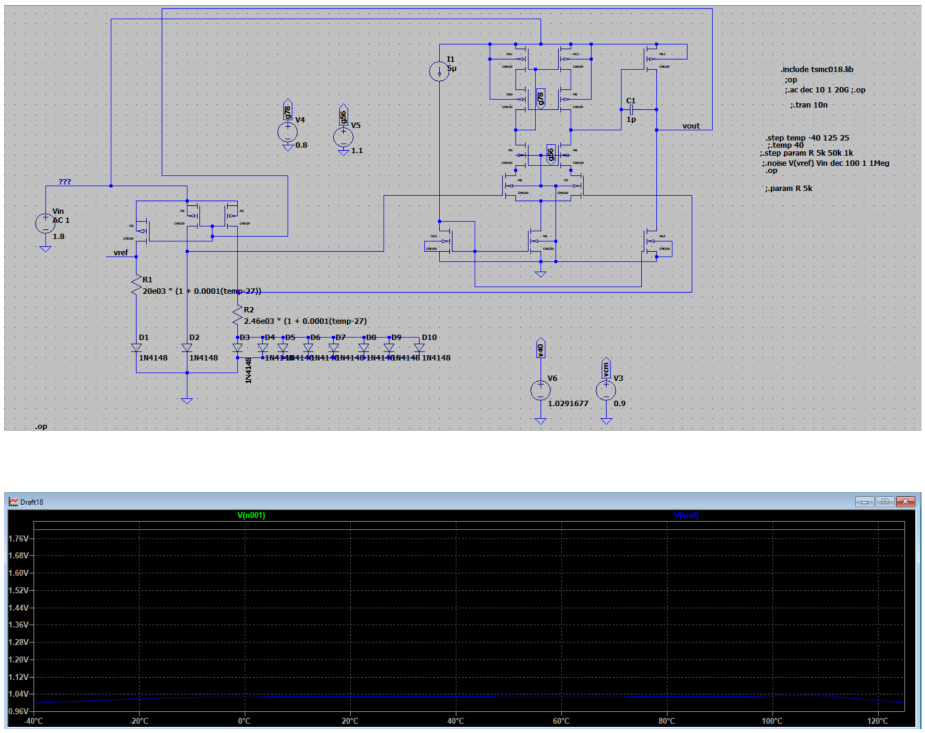


Figure 7: Reference voltage generated

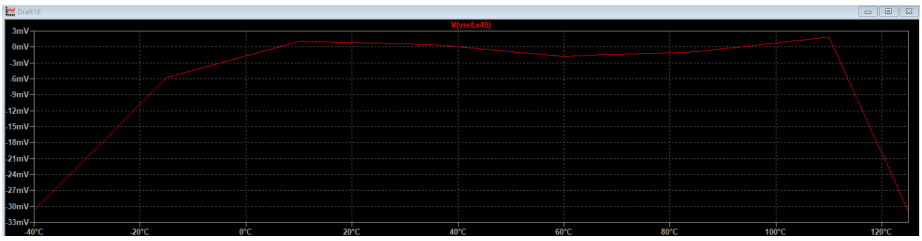


Figure 8: Error in Vref wrt values at 40°C

Calculations:

$$|\text{slope of PTAT}| = |\text{slope of CTAT}|$$

$$\frac{k\ln(N)}{q} \cdot \frac{R_2}{R_1} = 2 \times 10^{-3}$$

$$\frac{R_2}{R_1} = \frac{2 \times 10^{-3}}{\frac{k\ln(8)}{q}} = \frac{2 \times 10^{-3}}{86 \times 10^{-6} \cdot \ln(8)}$$

$$\approx 11.184$$

Observations:

- From earlier analysis, R2=20 K.
- To balance the slopes R1=2.46 K.
- CTAT slope observed: -2.34mV/C.
- Vref = 1.0289 V.Range of errors: (-30mV to 3mV).