report6

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Target Specifications:

- Output Voltage = 0.5V ± 1%
- Supply Voltage = 1.2V ± 10%
- Power Consumption < 1mW
- Temperature Range: −40 °C to 125 °C

PMOS characteristic

- Model: TSMC 65nm GP pch length = 180nm.

	voltage	gm/id27	id27	gm/id125	id125
1	0.000	1.425	-46.67E-6	1.374	-39.25E-6
2	50.00E-3	1.574	-43.48E-6	1.485	-36.68E-6
3	100.0E-3	1.740	-40.19E-6	1.610	-34.09E-6
4	150.0E-3	1.925	-36.82E-6	1.752	-31.46E-6
5	200.0E-3	2.130	-33.39E-6	1.911	-28.81E-6
6	250.0E-3	2.360	-29.94E-6	2.091	-26.16E-6
7	300.0E-3	2.622	-26.52E-6	2.293	-23.51E-6
8	350.0E-3	2.926	-23.16E-6	2.522	-20.91E-6
9	400.0E-3	3.285	-19.90E-6	2.785	-18.36E-6
10	450.0E-3	3.718	-16.76E-6	3.092	-15.90E-6
11	500.0E-3	4.250	-13.79E-6	3.461	-13.53E-6
12	550.0E-3	4.922	-11.01E-6	3.912	-11.29E-6
13	600.0E-3	5.792	-8.464E-6	4.480	-9.182E-6
14	650.0E-3	6.950	-6.190E-6	5.211	-7.232E-6
15	700.0E-3	8.523	-4.233E-6	6.177	-5.463E-6
16	750.0E-3	10.67	-2.640E-6	7.470	-3.902E-6
17	800.0E-3	13.51	-1.454E-6	9.201	-2.587E-6
18	850.0E-3	16.95	-683.5E-9	11.43	-1.553E-6
19	900.0E-3	20.47	-269.0E-9	14.06	-825.3E-9
20	950.0E-3	23.56	-89.49E-9	16.67	-383.5E-9
21	1.000	26.32	-25.74E-9	18.74	-158.2E-9
22	1.050	28.74	-6.521E-9	20.23	-59.69E-9
23	1.100	30.47	-1.522E-9	21.44	-21.10E-9
24	1.150	31.47	-375.8E-12	22.47	-7.079E-9
25	1.200	31.91	-141.6E-12	23.19	-2.315E-9

Figure 1: gmid vs ids Yellow:27 White:125

	voltage	gm/id27	id27	gm/id125	id125
1	0.000	1.423	-2.039E-6	1.288	-1.541E-6
2	50.00E-3	1.605	-1.891E-6	1.424	-1.441E-6
3	100.0E-3	1.816	-1.738E-6	1.581	-1.338E-6
4	150.0E-3	2.059	-1.578E-6	1.764	-1.232E-6
5	200.0E-3	2.329	-1.415E-6	1.976	-1.123E-6
6	250.0E-3	2.615	-1.251E-6	2.218	-1.011E-6
7	300.0E-3	2.910	-1.090E-6	2.486	-899.7E-9
8	350.0E-3	3.218	-935.2E-9	2.768	-789.2E-9
9	400.0E-3	3.559	-789.7E-9	3.061	-682.4E-9
10	450.0E-3	3.952	-654.7E-9	3.375	-581.1E-9
11	500.0E-3	4.422	-531.2E-9	3.729	-486.8E-9
12	550.0E-3	4.997	-420.0E-9	4.147	-399.9E-9
13	600.0E-3	5.723	-321.5E-9	4.657	-321.1E-9
14	650.0E-3	6.666	-236.1E-9	5.300	-250.6E-9
15	700.0E-3	7.925	-164.2E-9	6.130	-188.5E-9
16	750.0E-3	9.650	-106.0E-9	7.233	-135.2E-9
17	800.0E-3	12.02	-61.85E-9	8.719	-90.93E-9
18	850.0E-3	15.15	-31.47E-9	10.71	-56.12E-9
19	900.0E-3	18.86	-13.48E-9	13.26	-30.92E-9
20	950.0E-3	22.55	-4.806E-9	16.16	-14.86E-9
21	1.000	25.81	-1.459E-9	18.86	-6.202E-9
22	1.050	28.91	-405.0E-12	20.86	-2.322E-9
23	1.100	31.58	-132.0E-12	22.37	-825.4E-12
24	1.150	33.27	-79.90E-12	23.65	-308.8E-12
25	1.200	34.08	-80.70E-12	24.63	-151.0E-12

Figure 2: gmid vs ids Yellow:27 White:125 Length = 5u

Channel Length (nm)	**λ (1/V)**
60	0.705
180	0.236
300	0.191
420	0.148
540	0.125
660	0.108
780	0.097
900	0.088
1020	0.082
1500	0.062
2000	0.05
2500	0.034
3000	0.037

NMOS characteristics:

- Model: TSMC 65nm GP nch length = 5u.

	voltage	id27	gm/id27	id125	gm/id125
1	0.000	66.17E-12	32.91	280.0E-12	24.00
2	50.00E-3	101.5E-12	32.43	779.7E-12	23.35
3	100.0E-3	316.7E-12	31.37	2.349E-9	22.47
4	150.0E-3	1.316E-9	29.38	6.930E-9	21.15
5	200.0E-3	5.230E-9	26.32	18.87E-9	18.84
6	250.0E-3	17.49E-9	21.93	44.61E-9	15.54
7	300.0E-3	46.41E-9	17.29	89.22E-9	12.31
8	350.0E-3	100.2E-9	13.74	154.4E-9	9.808
9	400.0E-3	186.2E-9	11.22	240.4E-9	8.032
10	450.0E-3	310.5E-9	9.348	347.1E-9	6.762
11	500.0E-3	476.9E-9	7.888	474.5E-9	5.815
12	550.0E-3	686.3E-9	6.728	622.2E-9	5.078
13	600.0E-3	937.6E-9	5.797	789.4E-9	4.484
14	650.0E-3	1.228E-6	5.042	974.8E-9	3.994
15	700.0E-3	1.555E-6	4.423	1.177E-6	3.581
16	750.0E-3	1.914E-6	3.908	1.394E-6	3.225
17	800.0E-3	2.300E-6	3.473	1.624E-6	2.911
18	850.0E-3	2.709E-6	3.100	1.864E-6	2.619
19	900.0E-3	3.136E-6	2.767	2.107E-6	2.334
20	950.0E-3	3.571E-6	2.457	2.349E-6	2.054
21	1.000	4.005E-6	2.154	2.582E-6	1.790
22	1.050	4.423E-6	1.859	2.801E-6	1.556
23	1.100	4.814E-6	1.587	3.006E-6	1.353
24	1.150	5.173E-6	1.348	3.194E-6	1.180
25	1.200	5.496E-6	1.144	3.365E-6	1.031

Figure 3: gmid vs ids Yellow:27 White:125

Diode Characteristics

- Model: TSMC 65nm GP ndio-25.
- η, non-ideality factor = 0.84.

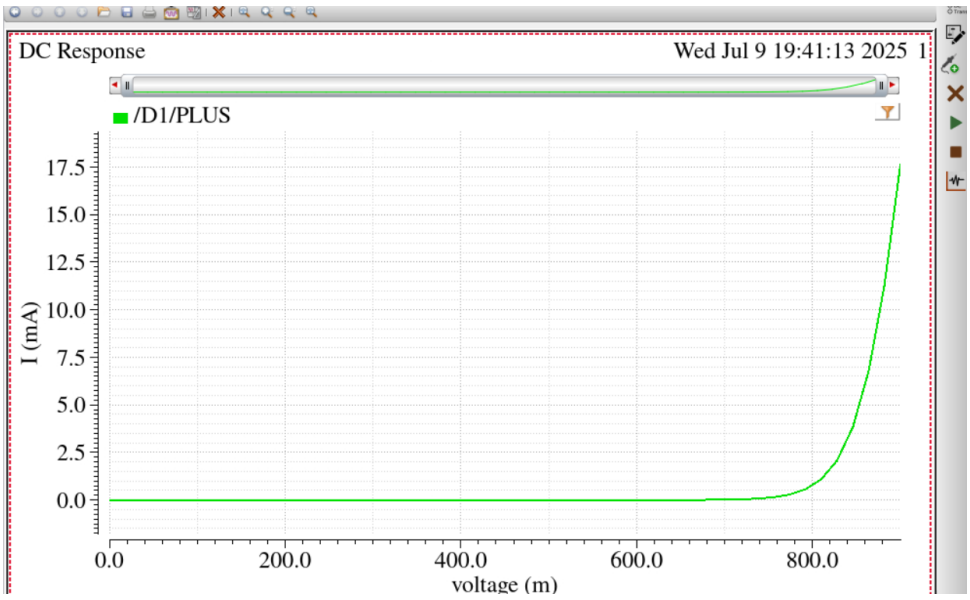

Figure 4:

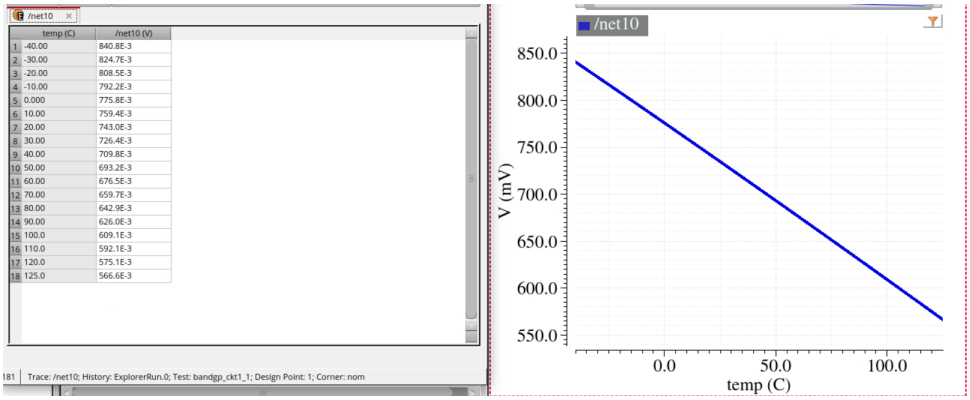

Figure 5:

The small-signal resistance r_d of a diode is given by:

$$r_d = \frac{\eta V_T}{I_D}$$

$$r_d = \frac{\eta V_T R_1}{\eta V_T ln(n)}$$

$$r_d = \frac{1063.76}{2.008}$$

$$g_{\text{res}} = \frac{2.008}{1063.76} = 1887.644\mu S$$

Bias Currents:

$$(I_{\text{total}})_{\max} = \frac{1000\,\mu\text{W}}{1.8\,\text{V}} = 566.6\,\mu\text{A}$$

Current Division

- Bias stage: $5\,\mu$A
- Branch current in core bandgap: $100\,\mu\text{A} + 100\,\mu\text{A} + 100\,\mu\text{A} = 300\,\mu\text{A}$
- Maximum power consumption of opamp: 100 μW ; Current of opamp = 55.56 μA .

Design Equations

- $$\frac{\frac{k}{q}\ln(n)\eta}{R_1} = \frac{0.00164}{R_2}$$
$$\Rightarrow \frac{R_2}{R_1} \approx 10.9 \tag{1}$$
- $$100\mu = \frac{\frac{k}{q}(300)\ln(n)\eta}{R_1} + \frac{0.737}{R_2} \tag{2}$$

Solving for R1,R2 and R3:

$$R_1 = 1063.76\ \Omega, \quad R_2 \approx 12,310\ \Omega$$

$$R_3 = \frac{0.5}{100\mu A}$$
$$= 5k\ \Omega$$

Current Mirrors:

- Channel length: 180n
- minimum supply :1.2 - 10% = 1.08V.
- voltage at drain 0.85V.
- For good operation VDS greater VDSAT by 50mV.(Assumption)
- $\frac{g_m}{I_d} = \frac{2}{V_{\text{ds}} - 50mV} = \frac{2}{1.08 - 0.85 - 0.05} = \frac{2}{0.18} = 11.1111$
- Number of fingers = $\frac{100\,\mu\text{A}}{2.3\,\mu\text{A}} = 43.47$ (rounded to 43)

Gain Calculations:

- $$\Delta Vout = \frac{R_3}{R_2}(1 + \frac{R_2}{R_1})(Vos + Verr)$$

  Here R2 = 12.310 kohm [Resistor that creates CTAT current] and R1 = 1.063 kohm.
- From target specification, maximum error acceptable in Vout = 5mV.
- Maximum Error in inputs of opamp:

$$Vos + Verr = \frac{\Delta Vout}{R_L(g_1 + g_2)} = \frac{0.005}{5000(0.0000812348 + 0.0009407338)} = 0.978mV. \quad (1)$$

$$Vos \approx Verr = 0.978/2 = 0.489mV.$$

- Voltage at gate of PMOS (branch) = Vdd - Vsg.

$$Voverdrive \approx \frac{2}{\frac{g_m}{I_d}}$$

$$Vgate = 1.2 - \frac{2}{\frac{g_m}{I_d}} - Vth = 1.2 - \frac{2}{11.111} - 0.45 = 0.57V \quad (2)$$

- Gain of opamp needed to create the necessary gate voltage:

$$A = \frac{Vgate}{Verr} = \frac{0.57 \times 1000}{0.489} = 1165 = 61.33dB \quad (3)$$

- Error in CTAT current:

$$\frac{Verr}{R_2} = \frac{0.489m}{12310} = 0.0397\mu A.$$

- Error in PTAT current:

$$\frac{Verr}{R_1} = \frac{0.489m}{1063} = 0.46\mu A. \quad (4)$$

Opamp design:

Opamp Design:

$$A(s) = \frac{g_m}{g_{\text{ds\_nmos}} + g_{\text{ds\_pmos}}}$$

$$A(S) \approx \frac{g_m}{2\lambda I_d}$$

- A(S) = 1165.
- Maximum possible gm/Id = 30 (say).

- $$\lambda = \frac{gm/id}{A(S) \times 2} = \frac{30}{2330} = 0.0128.$$
- Length of MOSFETs used: 4u.

$$\frac{g_m}{i_d} = 2\lambda A(S) = 0.7 \times 8.41 \times 2 = 11.774$$

- channel length = 90nM
- No. of fingers in input stage of opamp : $22.5/7 \approx 3$
- No. of fingers in tail = 27

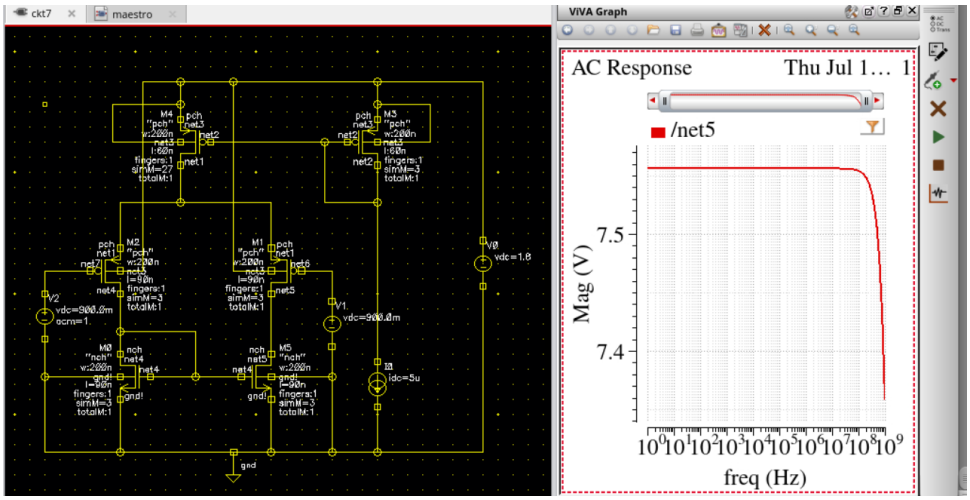

Figure 6:

Voltage reference:

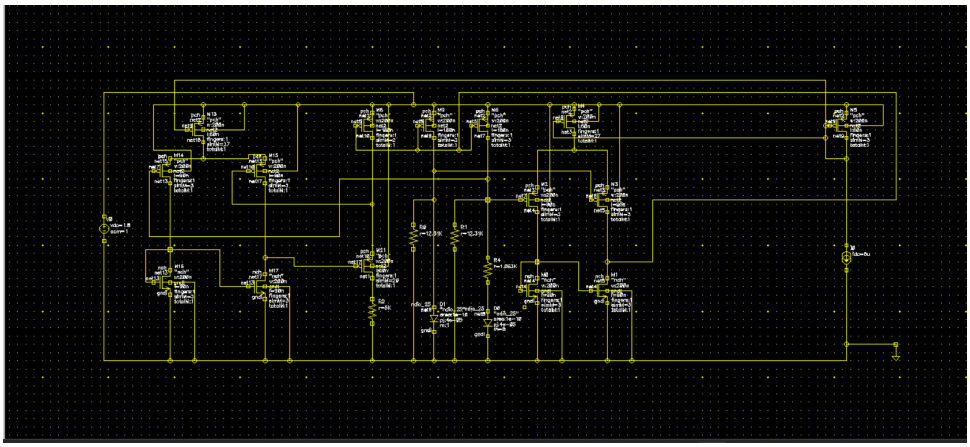

Figure 7:

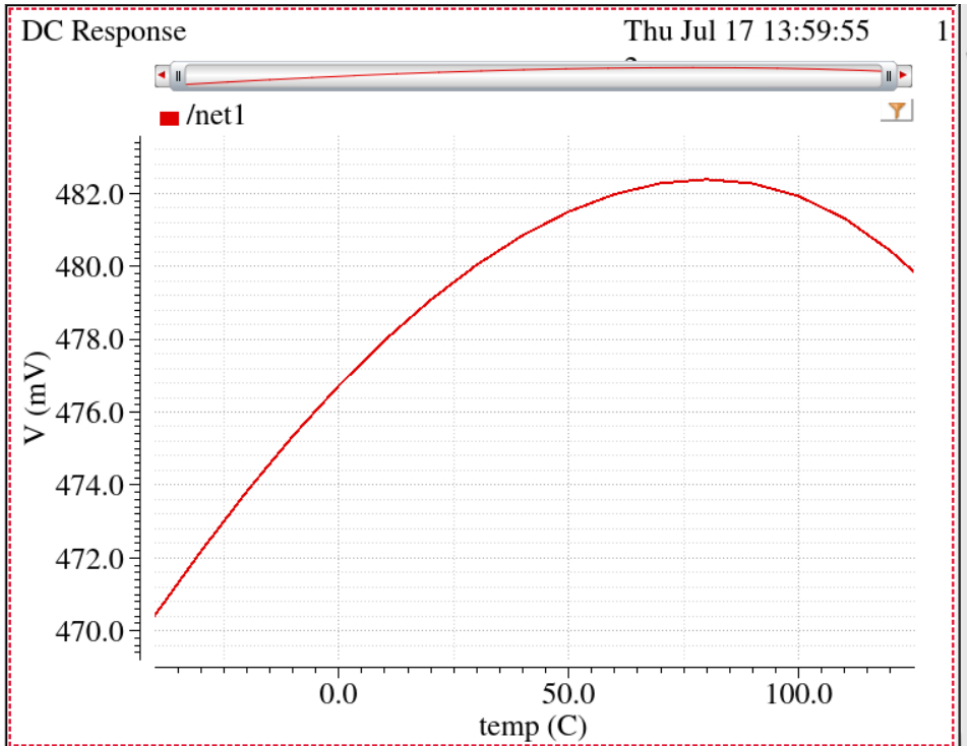

Figure 8: Output voltage

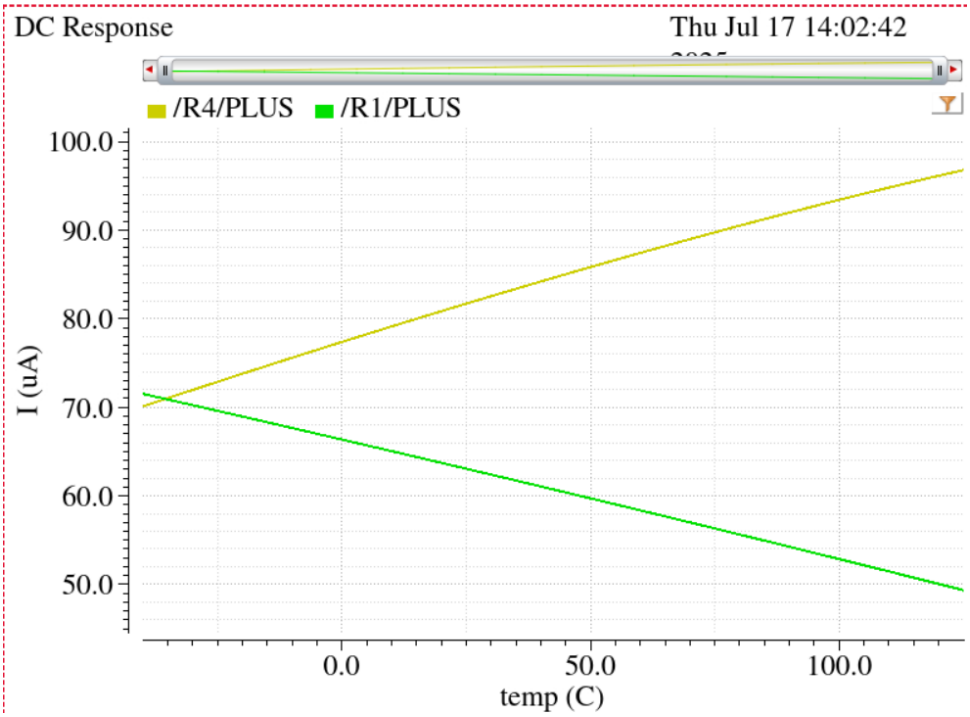

Figure 9: CTAT and PTAT currents

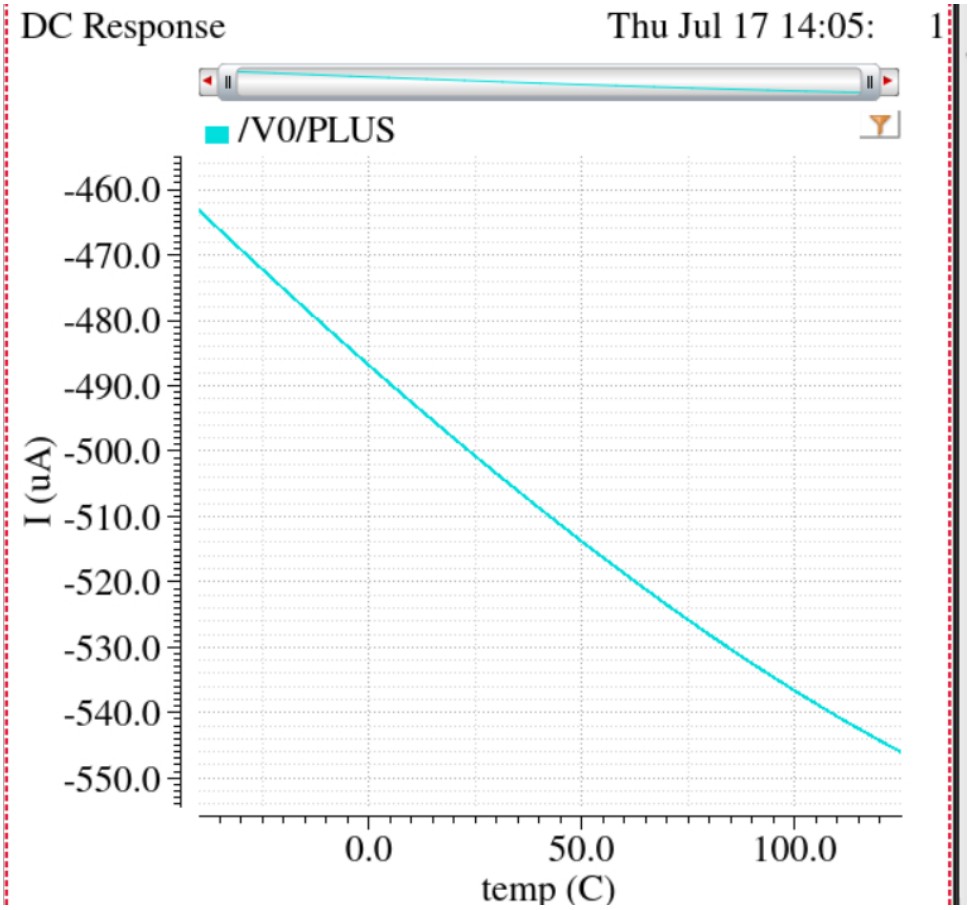

Figure 10: total current