report4

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Target Specifications

- Output Voltage = 1.2V ± 1%
- Supply Voltage = 1.8V ± 10%
- Power Consumption < 500μW
- Temperature Range: $-40\,^\circ$C to $125\,^\circ$C

Bias Currents

$$(I_{\text{total}})_{\max} = \frac{500\,\mu\text{W}}{1.8\,\text{V}} = 277.8\,\mu\text{A}$$

Current Division

$$85\mu A + 85\mu A + 85\mu A + 20\mu A \quad \text{(approx. 10\%)}$$

Design Equations

- $$\begin{aligned} \frac{\frac{k}{q}\ln(n)}{R_1} &= \frac{0.002}{R_2} \\ \Rightarrow \frac{R_2}{R_1} &\approx 11.18 \end{aligned} \tag{1}$$
- $$85\mu = \frac{\frac{k}{q}(233)\ln n + V_{\text{OS}}}{R_1} + \frac{0.6}{R_2} \tag{2}$$

Solving:

$$R_1 = 1239.76\ \Omega, \quad R_2 \approx 14,000\ \Omega$$

Current Mirrors

$$\begin{aligned} R_3 &= \frac{1.2}{85\mu A} \\ &= 14,117.6\ \Omega \end{aligned}$$

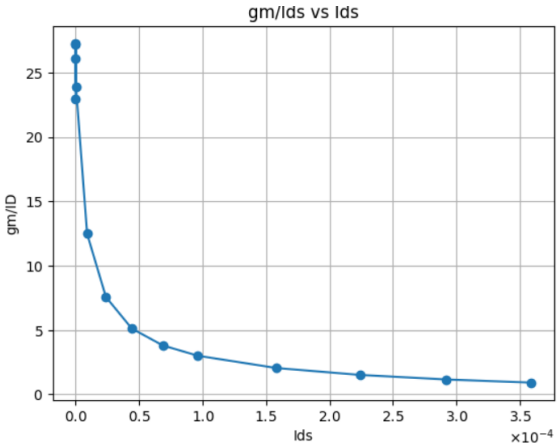

Figure 1: NMOS characteristics

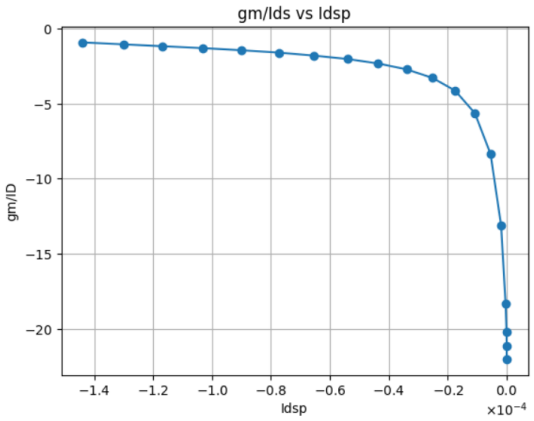

Figure 2: PMOS characteristics

- The PMOS for Output Voltage has the lowest headroom available.

$$[1.8 - 10\%] - [1.2 + 1\%]$$

$$\frac{g_m}{I_D} = \frac{2}{V_{\text{DSAT}}} = \frac{2}{400 \text{ mV}} = 5$$

$$I_{\text{per unit width}} \approx 15 \ \mu A$$

- Due to CLM, current is lower here than other branches.

$$m = \frac{85}{15} = 5.666 \Rightarrow \text{Round off to 5 (lower)}$$

Observations

$$R_1 = 2,200 \ \Omega$$
$$R_2 = 15,000 \ \Omega$$

Currents

$$74\ \mu A, \quad 80\ \mu A, \quad 80\ \mu A, \quad 30\ \mu A \quad (11.4\%)$$

$$\begin{aligned} R_3 &= \frac{1.2}{74\mu A} \\ &= 16.2k\ \Omega \end{aligned}$$

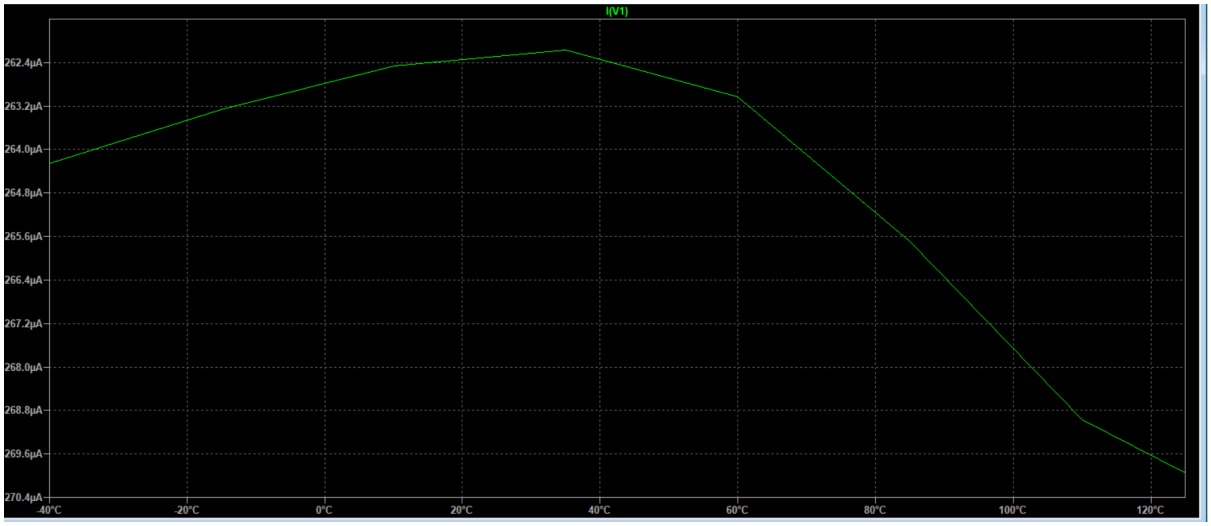

Figure 3: Total Current consumed

Bandgap Reference :

- Voltage Output at 27 degrees:1.1947398V.
- Range of errors : +9 to -12 mV (within 1 percent of 1.2 volt).
- Maximum power : 486.72μ W.

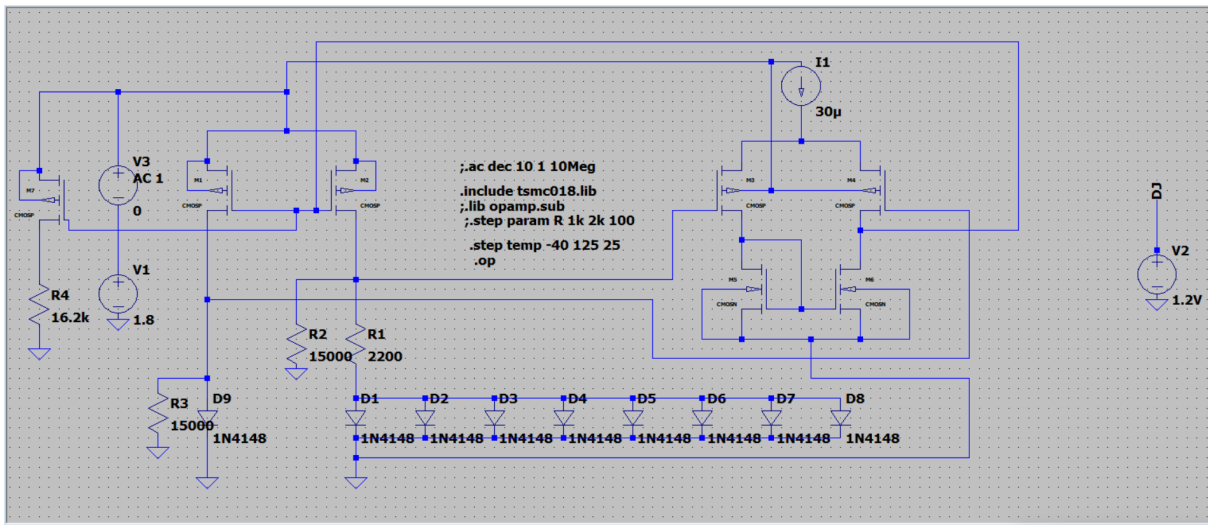

Figure 4:

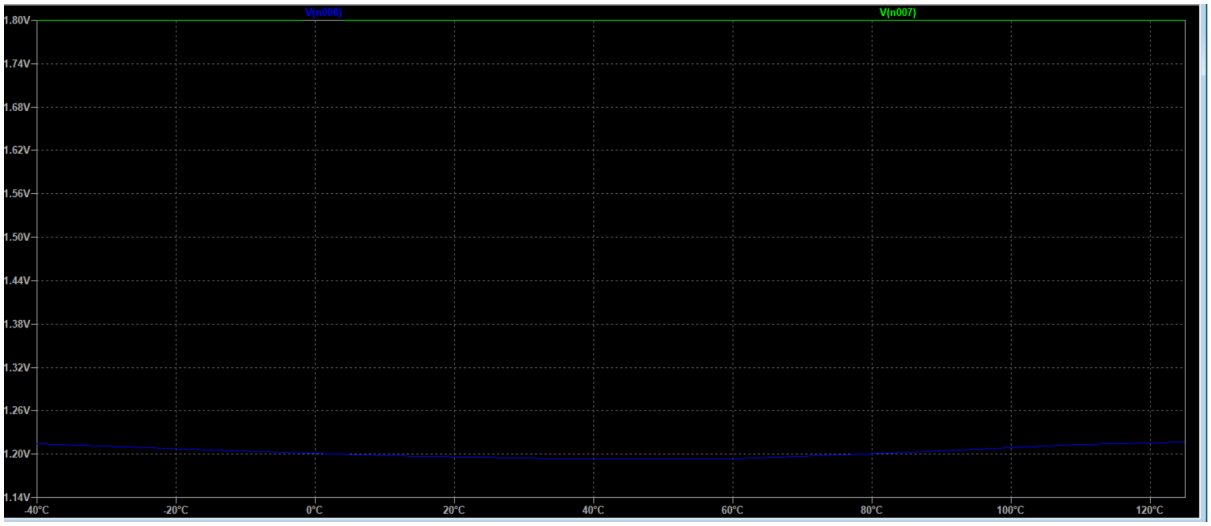

Figure 5: Output voltage

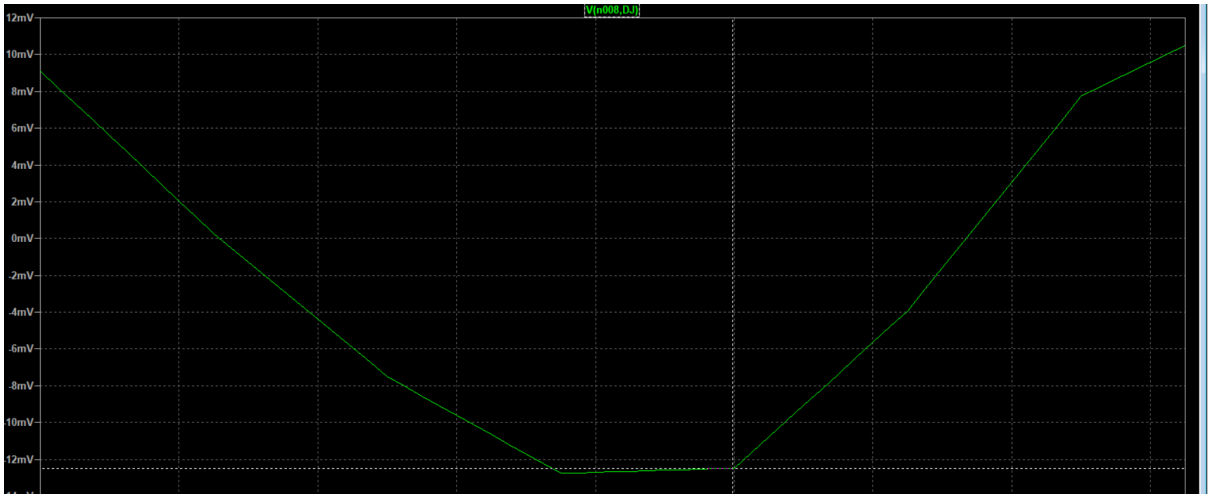

Figure 6: errors in output voltage

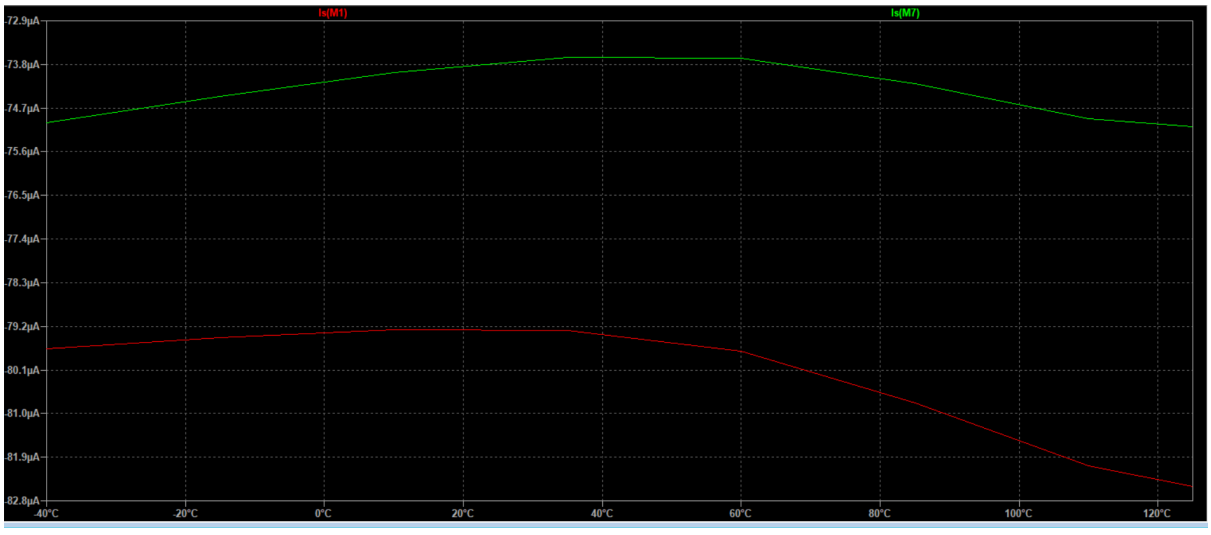

Figure 7: Current values