C V RAMAN GLOBAL UNIVERSITY, BHUBANESWAR
SIXTH SEMESTER
RE-MIDSEM EXAMINATION-2021

SUBJECT: Advance Computer Architecture
SUBJECT CODE: CS30144
TIME: 90 MINS **FULL MARK: 60**
BRANCH: CSE AND CSIT

1. Answer all**.** **(8x2.5=20)**

a) Discuss data Hazard reduction using NOP instruction in the pipeline.
b) Explain need of hierarchy in memory organization.
c) Explain Instruction pipeline.
d) Show True dependency in MIPS with proper example.
e) Compare Machine cycle and Memory cycle.
f) Draw a space-time diagram for a six segmented pipeline showing the time it takes to process eight task.
g) Explain Cache Coherence.
h) The following transfer statements specify a memory. Explain the memory operation in each case.
1. R2 ← M [AR]
2. M [AR] ← R3
3. R5 ← M [R5]

2. Answer any FOUR **(10x4=40)**

(a) Consider the addressing modes in MIPS and find the sequence of operations to the instructions given.
1. LDR r0, [r1] (2.5)
2. LDMIA r0, (r1, r2, r4) (2.5)
3. LOOP: MOV $s0, 10 (5)
ADD $s0, s1
SUB $s0, 1
BNE LOOP

(b) Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessors with proper diagram from the viewpoint of hardware organization and programming techniques. (5+5)

(c) In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)$ $(C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for I = 1 through 6. (5+5)

(d) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K × 32. Formulate all pertinent information required to construct the cache memory. What is the size of the cache memory? (5+5)

(e) Consider the following sequence of instructions:
Add R1, R2, R3
Mul #3, R4, R3
Sub R4, R2, R5
Add #20, R2, R5
Show the content of different stages at different clock pulses in a 4 stage pipelined processor, by considering the Space Time diagram. Show the content of inter-stage buffers from clock pulse 2 to 8. The contents of registers R1, R2 and R4 are 10, 20 and 30 respectively. (Outer most operator is the destination operand) (2.5+2.5+5)