**CAST CPET-563 Embedded Systems Design II** **Dr. Kaputa**
**Spring 2019**
**Lab 1**

**Student Name: _____ Section #:_____**

**Introduction:**

You are to create a PWM module in VHDL that accepts a period and duty cycle and generates a PWM pulse train output. The module shall be fully verified via simulation in Modelsim. Verify the module for all corner cases. Assume the input clock frequency is 100 MHz.

**Requirements for the PWM module:**

- shall have an enable pulse.
- shall be able to control both the duty cycle and the period of the PWM pulse train.
- shall use basic entity inputs and not use 'generics' for the period and duty inputs.

**Module Report:**

Create a tech memo for the module describing the module's functionality and limitations. Also include all necessary verification information such as screen shots, input/output files, etc. Assume that this module is an essential component of the engine control system of the 747 you will be flying to Disney World on.

**Lab Submission:**

1. Print out this lab description with your name on the front and attach all code and the tech memo. Hand this packet in at the start of the following lab session. This printed out packet can be shown at a job interview.
2. Submit a single zip file with all code and the tech memo by 9:00 am one week after the lab date at: https://www.dropbox.com/request/SRTXrlf25mVgKY9PllK6

**Grading:**

| | Score | Pts |
|---|---|---|
| **Code**<br>No tabs please. Proper spacing and formatting. Adequate variable names. Consistency. | | /2 |
| **Comments**<br>Proper header and comments throughout | | /1 |
| **Demonstration**<br>To be performed within lab week. Can show after due date with time stamped code. | | /2 |
| **Tech Memo**<br>To be performed within lab week. Can show after due date with time stamped code. | | /5 |
| **Final Grade** | | /10 |