Analog to Digital Conversion and Digital to Analog Conversion (ADC and DAC)

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EEET-425

Key Points From Chapter

- Analog to digital conversion adds noise.
- The noise is called quantization noise.
- When the quantization noise is high, the signal to noise ratio is low.
- A useful approximation is that the signal to noise ratio of an A/D converter is 6 dB times the number of bits used in the A/D conversion process.**
  - ** Note this approximation is for sinusoidal inputs, not for dc inputs.
- You can get high resolution data from a low resolution A/D converter if you use dithering and averaging.

Key Points From Chapter

- Signals in the analog domain are converted to the digital domain through the processes of sampling and quantization.
- Sampling at too low of a rate can lose or distort information in the signal (aliasing)
- Signals are broken into discrete numerical values (levels) by a process of quantization.
- Using more bits to represent these discrete numbers gives you more accuracy (less error) or less quantization error.
- (e.g. 8 bits = 256 levels, 10 bit number = 1024 levels)

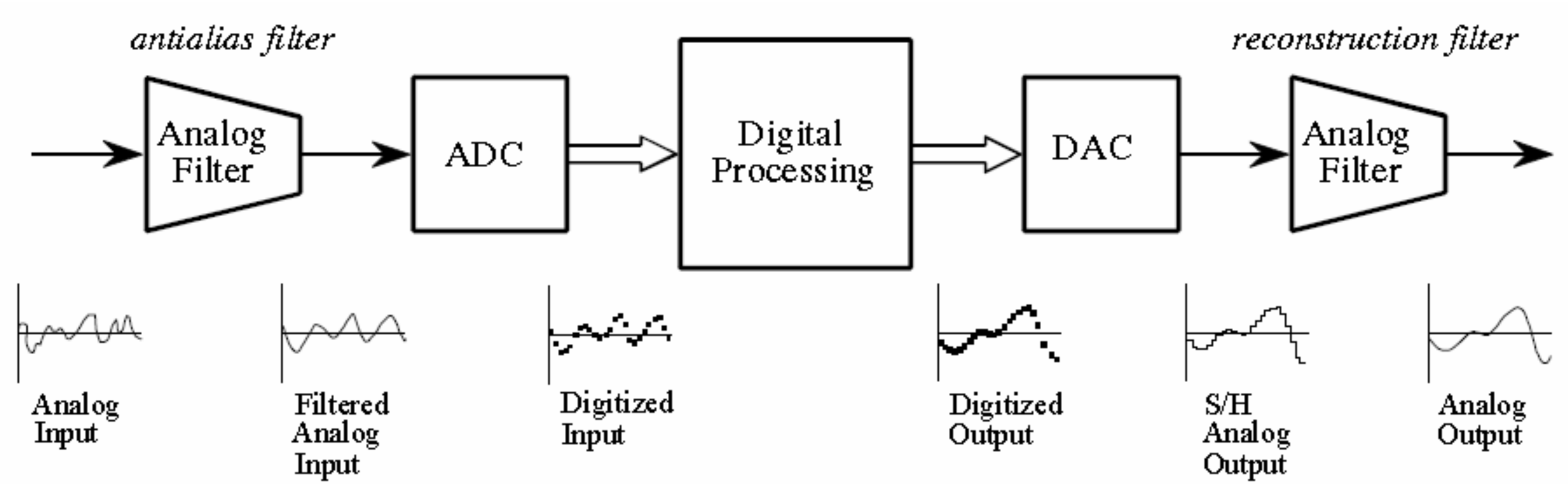
Key Points From Chapter

- The quantization error from analog to digital conversion can be treated as a noise source, (quantization noise)
- When the quantization noise is high, the signal to noise ratio is low.
- A useful approximation is that the signal to noise ratio of an A/D converter is 6 dB times the number of bits used in the A/D conversion process.**
  - ** Note this approximation is for sinusoidal inputs, not for dc inputs.

Key Points From Chapter

- One way to lower quanitization noise is to use more bits to represent the digital number, but this requires a more expensive/slower A/D converter.
- Another way to lower quantization noise is to average a large number of samples
  - Averaging reduces random noise, but leaves the mean value (true signal) unchanged.
  - Think typical error formula: More samples (N) reduces the error in your estimate the true signal.
- You can get high resolution data from a low resolution A/D converter if you use dithering and averaging.

Overview of ADC/DSP/DAC System



In Class Example

- LSB definition
- Quantization Example
- Materials: ruler, yardstick, whiteboard

Quantization Noise Formulas

- Quantization noise is uniformly distributed with a standard deviation of 0.29 LSB

$$\sigma_{qn} = 0.29\ LSB$$

$$\sigma_{qn} = 0.29 \left[(Full\ Scale\ ADC\ Range) \frac{1}{2^{n_{bits}}} \right]$$

- Example:
- Full scale A/D range of 5 volts, nbits=10:

$$\sigma_{qn} = 0.29 \left[(5\ V) \frac{1}{2^{10}} \right] = 1.41\ mV$$

In Class Problem (Part 1 of 2)

- Draw/ sketch a uniform distribution that represents quantization noise of the A/D conversion process. Assume the range of quantization error is from -1/2 LSB to +1/2 LSB
- Refer back to chapter 2, what is the standard deviation of a uniform distributed noise source whose amplitude has a maximum of -1/2 to +1/2.

- Note: The noise amplitude ranges from -1/2 to +1/2, its average amplitude is given by the standard deviation since the noise is a <u>random variable</u>

In Class Problem (Part 2 of 2)

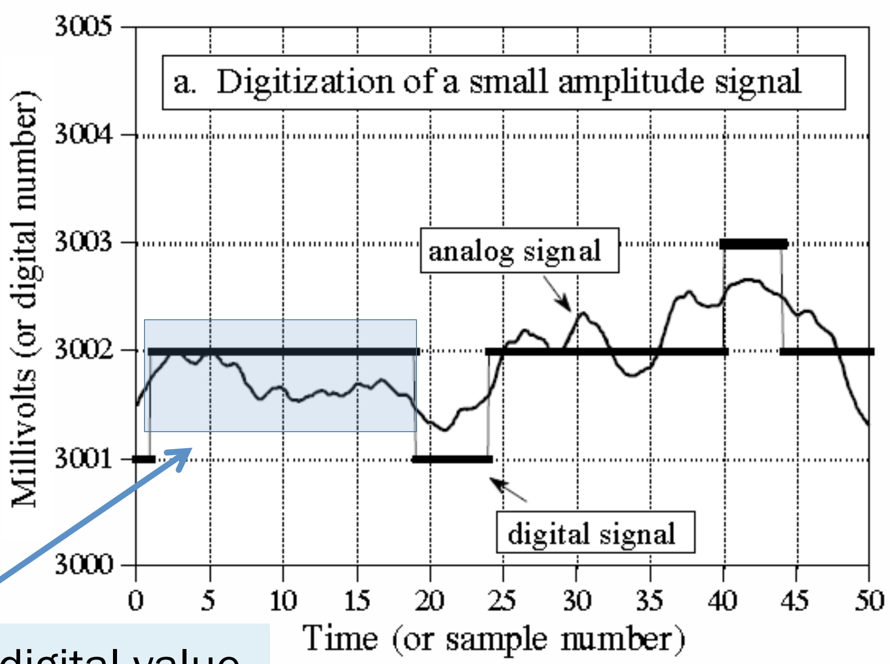
- Let's say to you take just one sample from the A/D converter. How much error is in that sample due to quantization noise? (Hint: Use the quantization noise amplitude you just found to describe it and recall that the error is expressed in terms of a fraction of an LSB.)

- What if you take 100 samples from the A/D converter and average them together. How much error will there be in this average value. (Hint: Think of how much random error you had in one sample. Each sample has this error, but after average 100 samples, the random error is reduced. How much is it reduced? Use the typical error formula.

Limitations of the Quantization Error Model

- While the quantization error is often modeled as a uniform noise source with σ =~ 0.29 LSB, there are times when this model fails.

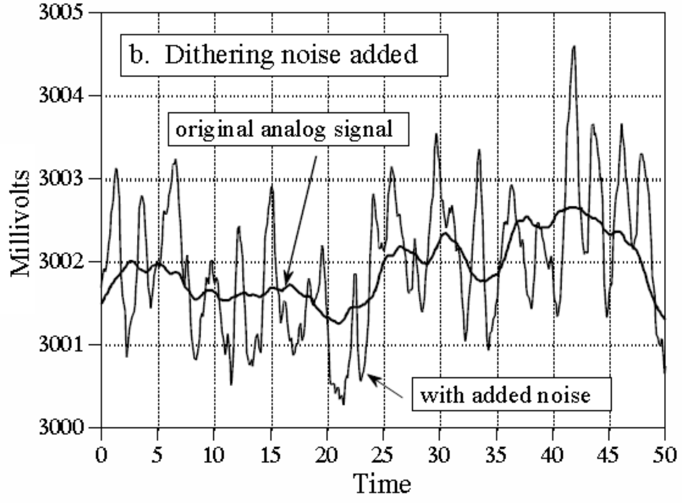
- This can occur when there is not enough noise in the system to cause the bit value of the quantized voltage to change over time.

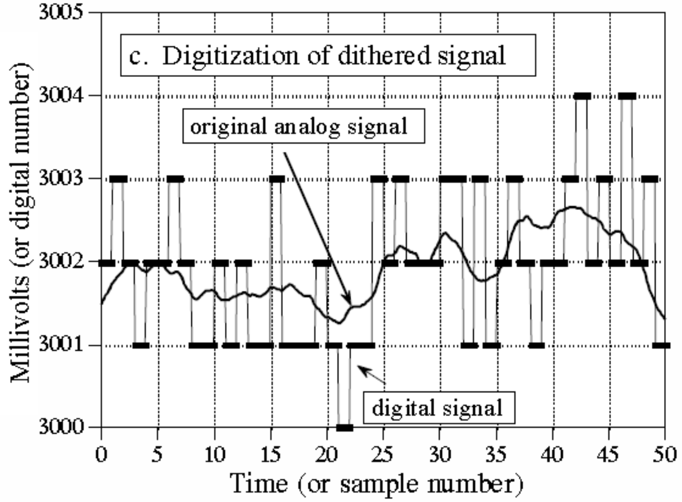


Many samples, but no change in digital value

Addition of Dithering Noise to Improve Resolution

- By adding a small amount of random noise, called dithering, the quantization error can be made uniformly distributed.
- Adding dithering can increase the resolution of the signal measure if many samples are averaged.
- Dithering noise can come from analog noise in the system or be added digitally using a DAC.



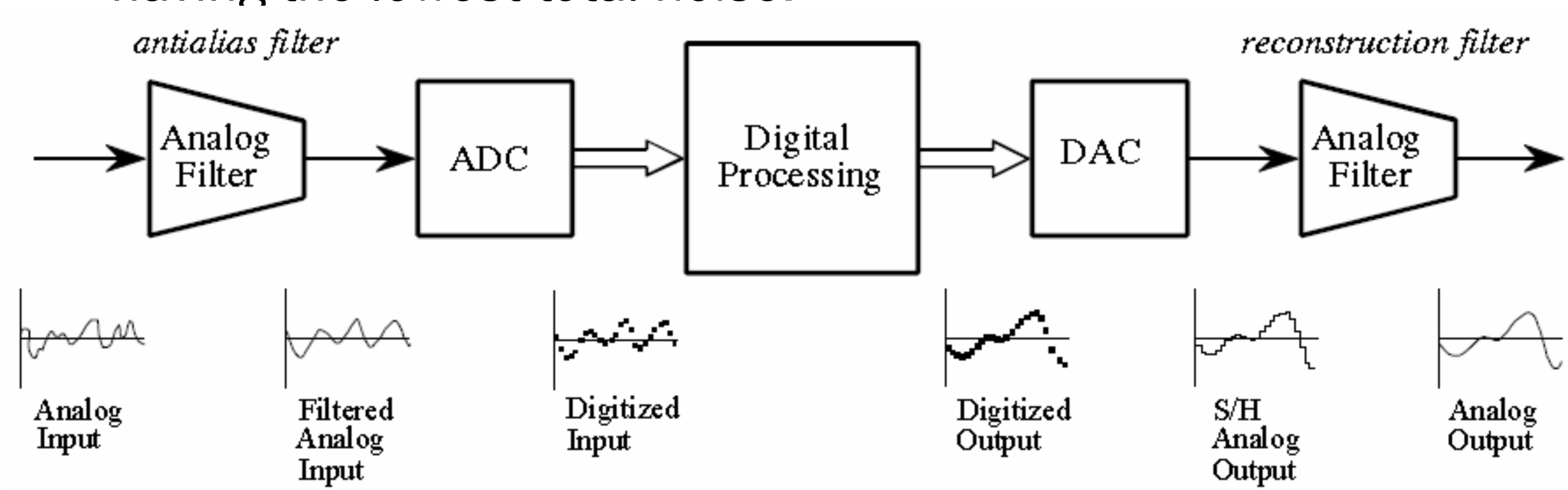


Detailed Chapter Summary

- Analog to Digital Conversion
  - Quantization Effects and Noise
    - In Class Probem: Quantization Noise vs Number of Bits
    - In Class Team Problem: Choosing Number of Bits
  - Sampling: Aliasing and Nyquist
- Digital to Analog Conversion
  - In Class Problem:
- Overall A/D->DSP->D/A System
- Analog Filters for Anti-aliasing and Reconstruction
- Multi-rate methods
- Summary

Overview of ADC/DSP/DAC System

- Analog to Digital Conversion (ADC) is used to get data into a DSP, Digital to Analog Conversion (DAC) is used to digital signals out to the analog world.
- The input and output conversion process needs to be designed to introduce as little distortion as possible to the <u>information of interest</u>. Note this may not be same as having the lowest total noise.



Analog to Digital Conversion

- Analog to Digital conversion consists of two steps
  - 1) Sampling and holding of the analog signal.
  - 2) Quantization of the analog signal

- <u>Sampling and holding</u> converts the continuous domain independent variable (e.g. time) into a discrete variable (e.g. time = 0.1, 0.2, 0.3 seconds)
- <u>Quantization</u> converts the continuous range dependent variable (e.g. voltage) into a discrete variable (e.g. voltage = 4092, 4093, 4094 bits)

Analog to Digital Conversion (1/2)

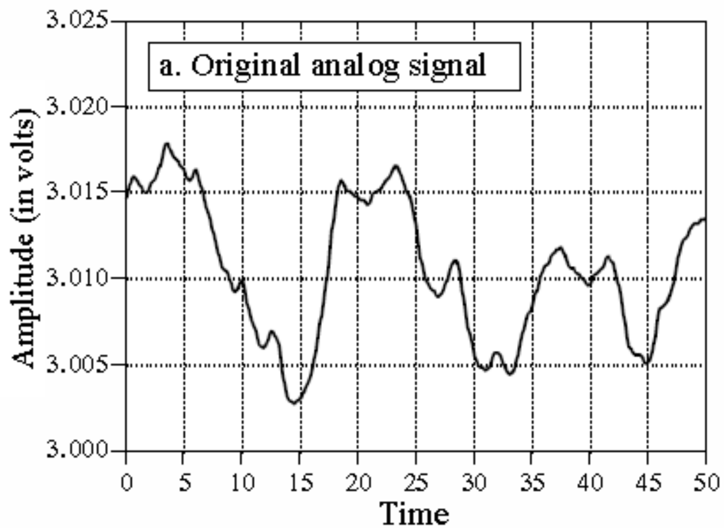
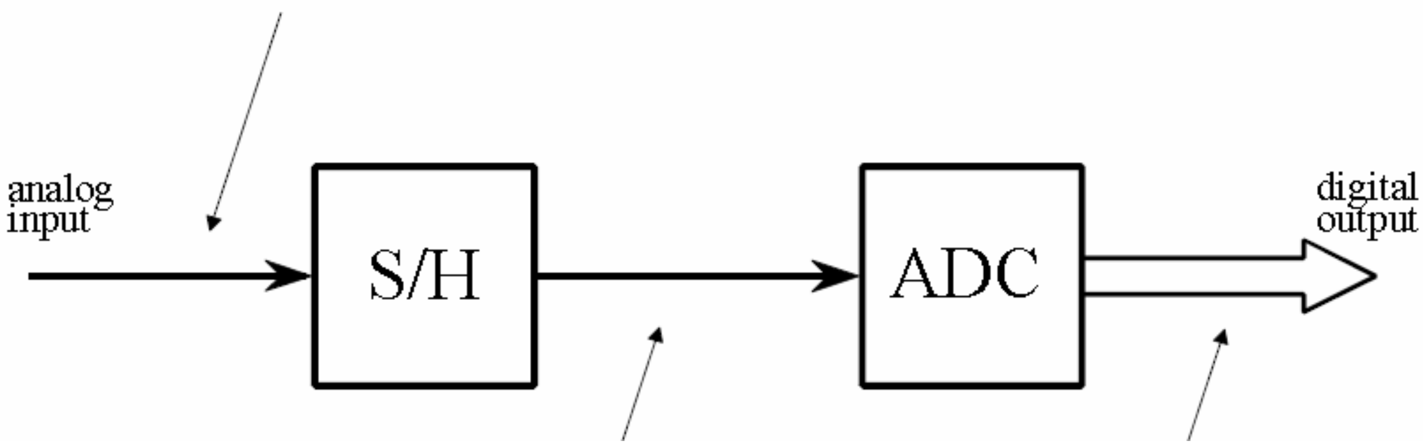
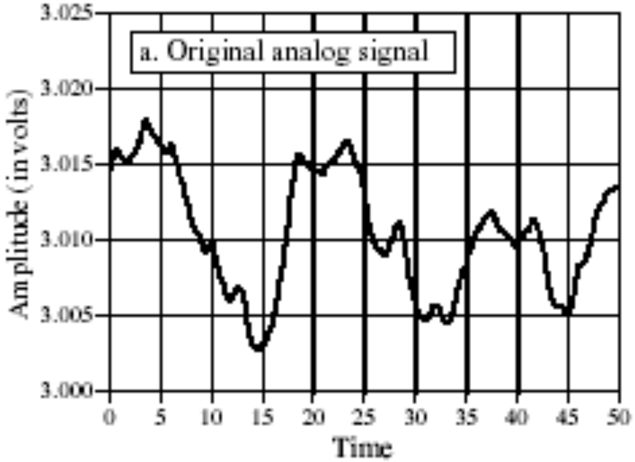


FIGURE 3-1
Waveforms illustrating the digitization process. The conversion is broken into two stages to allow the effects of *sampling* to be separated from the effects of *quantization*. The first stage is the sample-and-hold (S/H), where the only information retained is the instantaneous value of the signal when the periodic sampling takes place. In the second stage, the ADC converts the voltage to the nearest integer number. This results in each sample in the digitized signal having an error of up to ±½ LSB, as shown in (d). As a result, quantization can usually be modeled as simply adding noise to the signal.



Analog to Digital Conversion (2/2)



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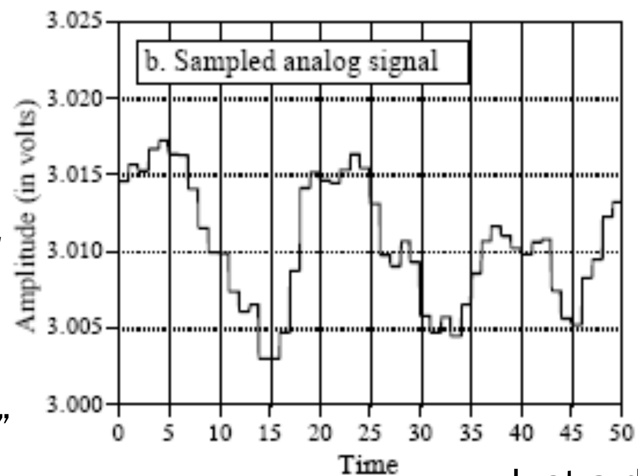
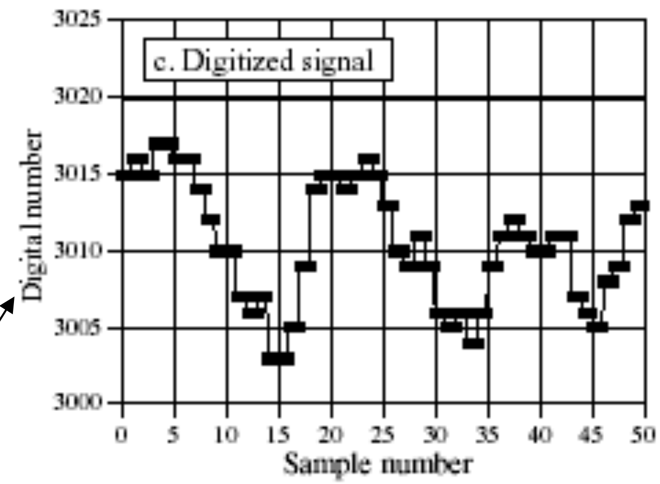
- Sample signal and hold it for a while so that it may be quantized (Analog to digital conversion)





Voltage
or "Amplitude"

Just a digital
number

Time

Sample

Quantization Effects

- Quantization refers to taking an continuous real number and binning it into discrete, quantized levels e.g. bins of 1 to 4096 for a 12bit A/D converter.
- Quantization results in error – actual value of the signal must be placed into nearest allowed value (e.g. out of 4096 values).
- Error looks like an additive noise is that is uniformly distributed from ±½ LSB (Least Significant Bit), has a mean of zero, and a standard deviation of $1/\sqrt{12}$ LSB (approx 0.29 LSB of noise)

Quantization Noise Formulas

- Quantization noise is uniformly distributed with a standard deviation of 0.29 LSB

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- Example:
- Full scale A/D range of 5 volts, nbits=10:

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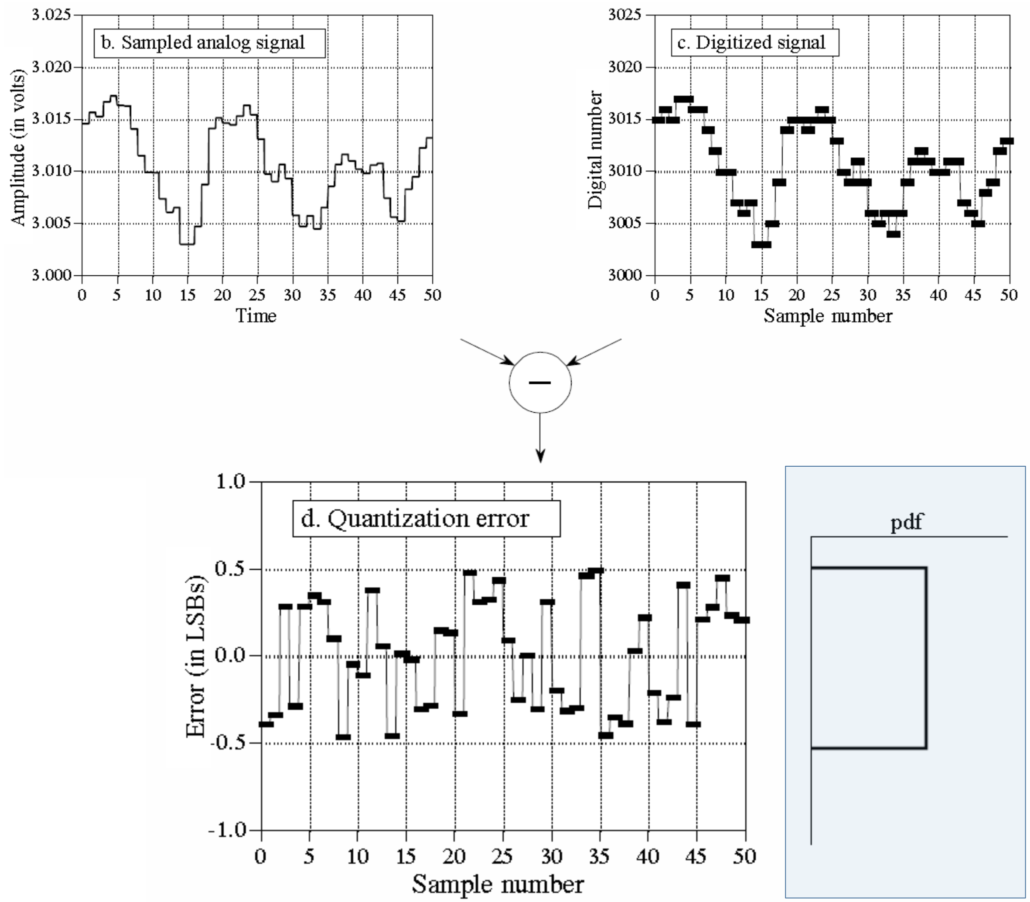
Quantization Adds Uniform Noise

- Quantization Error is found by taking difference of analog signal and digitized signal.

- Note uniform distribution (equal likelihood for all values from -1/2 LSB to +1/2 LSB)



Recall From Chapter 2 That Noise Sources Add in Quadrature

- The noise from quantization adds to any pre-existing noise.
- The noises add in quadrature so that the total noise is:

$$Total\ Noise = \sqrt{(QN^2 + AN^2)}$$

where

QN = the rms quantization noise

AN = the rms analog noise

In Class Problem: Quantization Noise vs Number of Bits

- Quantization Noise vs Number of Bits.
  - Consider a System with an A/D converter input voltage range of - 3 to +3 volts.
  - The analog noise in the system is measured to be Gaussian with a standard deviation of 6 mV.
  - What number of ADC bits is required to have the quantization error equal the existing analog noise?

In Class Problem - Solution

- (0.29)*LSB = 6mV
- LSB = 20.69mV

In Class Team Problem: Choosing Number of Bits

- Specify how many bits are needed to appropriately digitize the following signal. Choose from 6 bits, 8 bits, 10 bits, 12 bits, 14 bits or 16 bits.
  - A. a signal where the maximum amplitude is 0-1 volt and the rms noise is 1.5 milivolts.

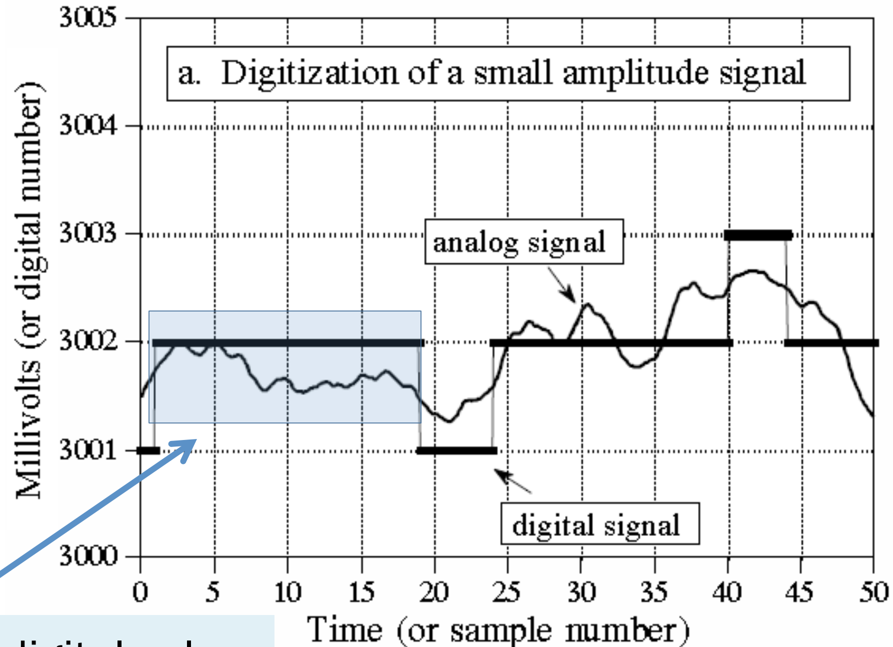
- Assume that you do not want to add significant noise during the quantization process.
  - You define what is significant and what is not. Hint: think percent increase over the given rms noise.

Team Problem - Solution

Limitations of the Quantization Error Model

- While the quantization error is often modeled as a uniform noise source with σ =~ 0.29 LSB, there are times when this model fails.

- This can occur when there is not enough noise in the system to cause the bit value of the quantized voltage to change over time.



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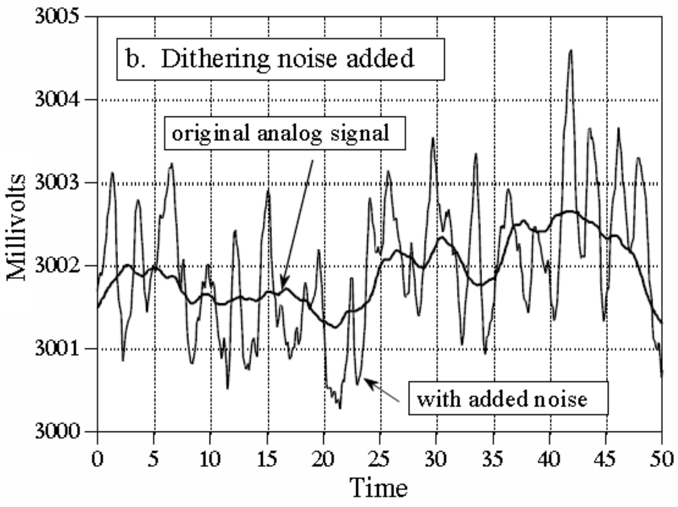
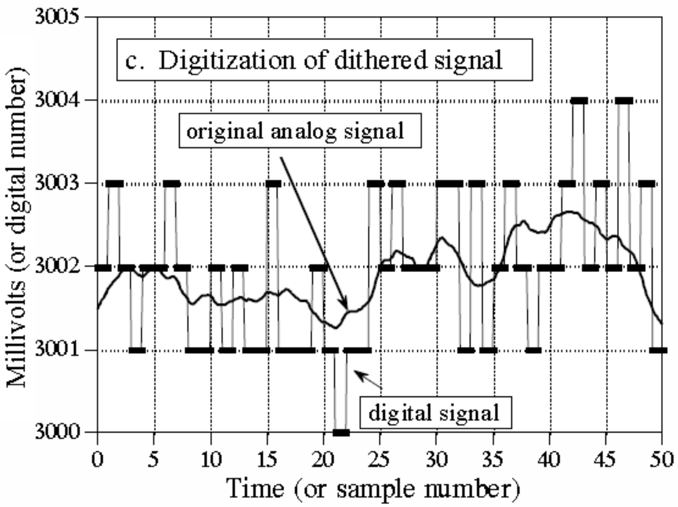




Example : Increasing A/D Converter Resolution by Averaging

- Consider a 10 bit A/D converter that has a full scale voltage range of 0-10 volt and that has adequate analog noise to provide dithering.
- What is the quantization noise in rms volts of the ideal 10 bit A/D converter?

$$QN_{10bit} = 0.29 * \left(\frac{10V}{1024}\right) = 0.002832\ V$$

- If you average 16 samples from the A/D converter, what is noise rms voltage? (Use the typical error formula to find the effect of averaging)

$$TE = \frac{\sigma}{\sqrt{N}} = \frac{0.002832\ V}{\sqrt{16}} = 0.000708\ V$$

- Compare this to the quantization noise arising from using a 12 bit A/D converter.

$$QN_{12bit} = 0.29 * \left(\frac{10\ V}{4096}\right) = \ 0.000708\ V$$

Advanced Dithering – Noise Shaping

- By adding a small amount of random noise, the quantization error can be made uniformly distributed.
- It is also possible to shape the noise so that it is not white noise, but has lower spectral energy in certain bands (e.g. where the desired signal is) and higher energy in other bands (e.g. where the anti-aliasing filter is).
- Noise shaping is used in Sigma Delta modulators (typically for audio signals) to get better dynamic range and a higher signal to noise ratio.

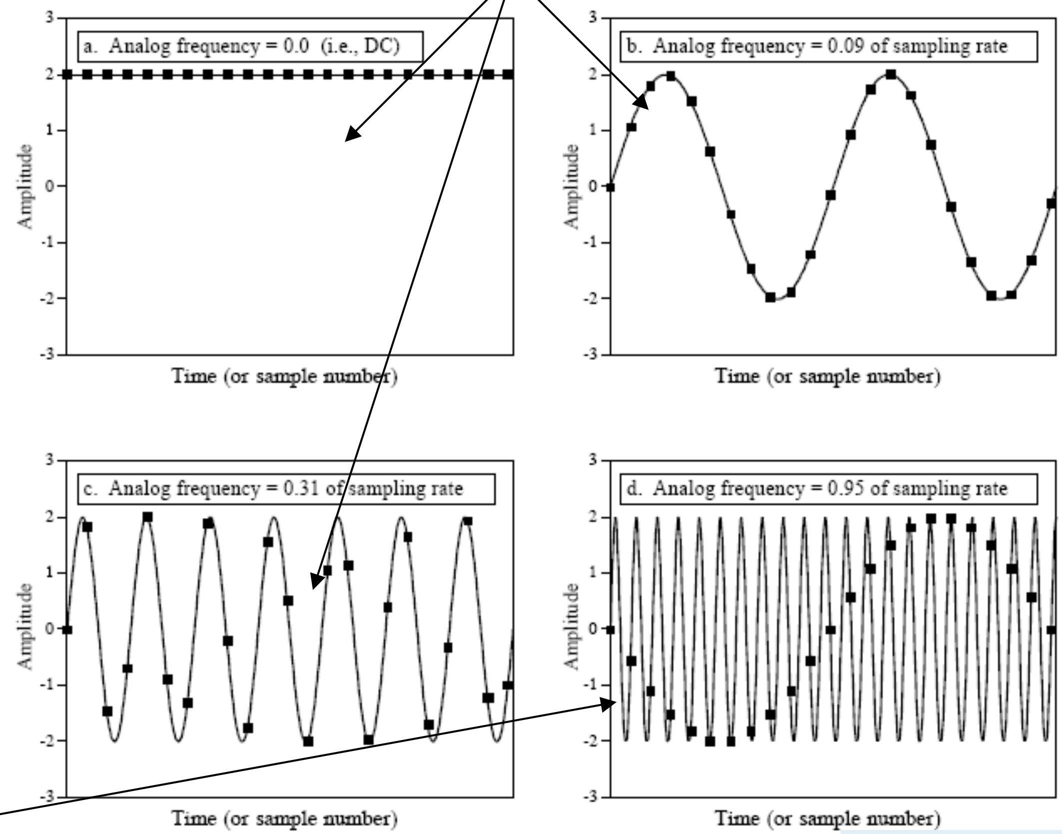
Stretch Break

-

Sampling: Aliasing and Nyquist (1/2)

- Sampling at too low of a rate can result in false signal information
- How fast do we have to sample a given analog signal?

Oversampled

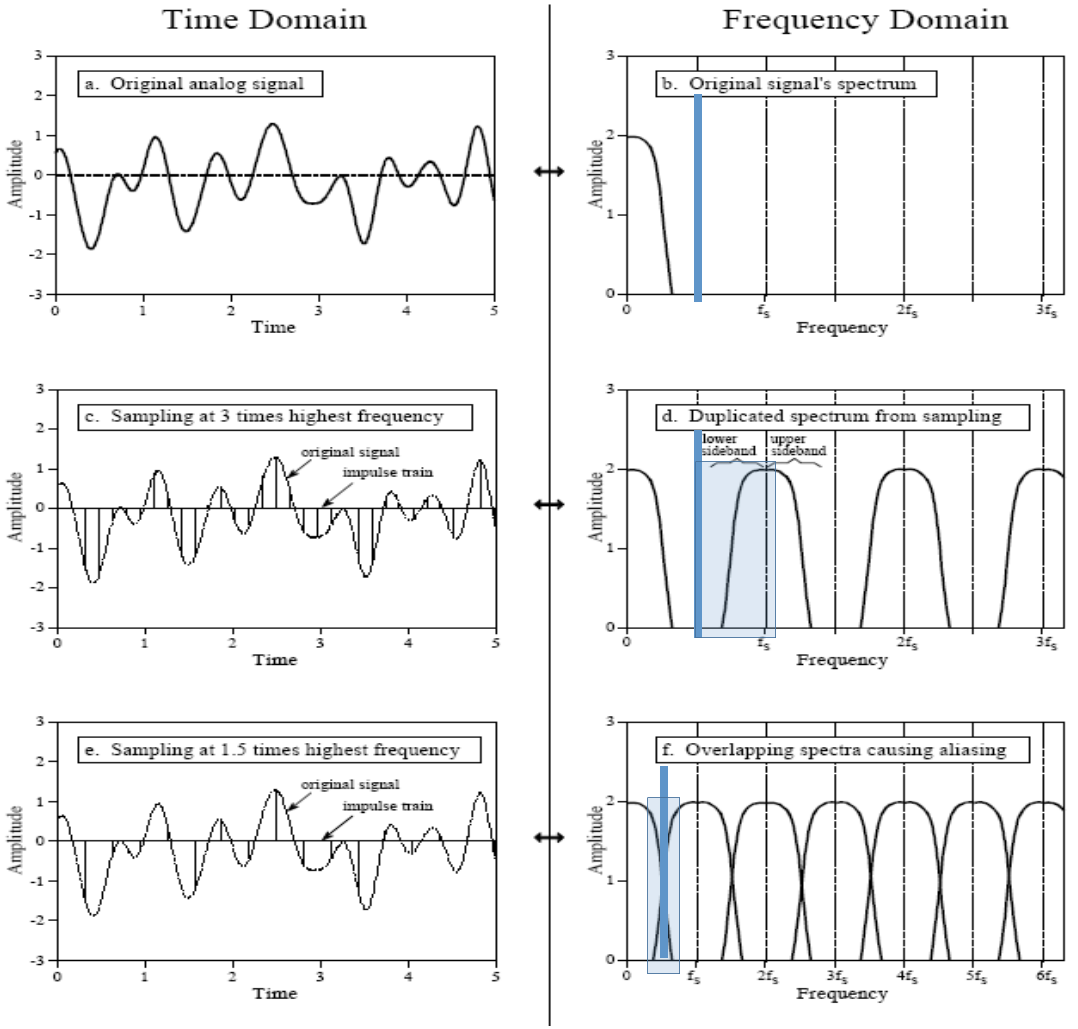


Undersampled = Aliasing

- ○ Nyquist: We must sample at or 2*Fh, where Fh is the highest frequency in the sampled signal

Note phase Inversion in time domain

Sampling: Aliasing and Nyquist (2/2)



Fs/2 = The folding frequency

Note the spectrum inversion

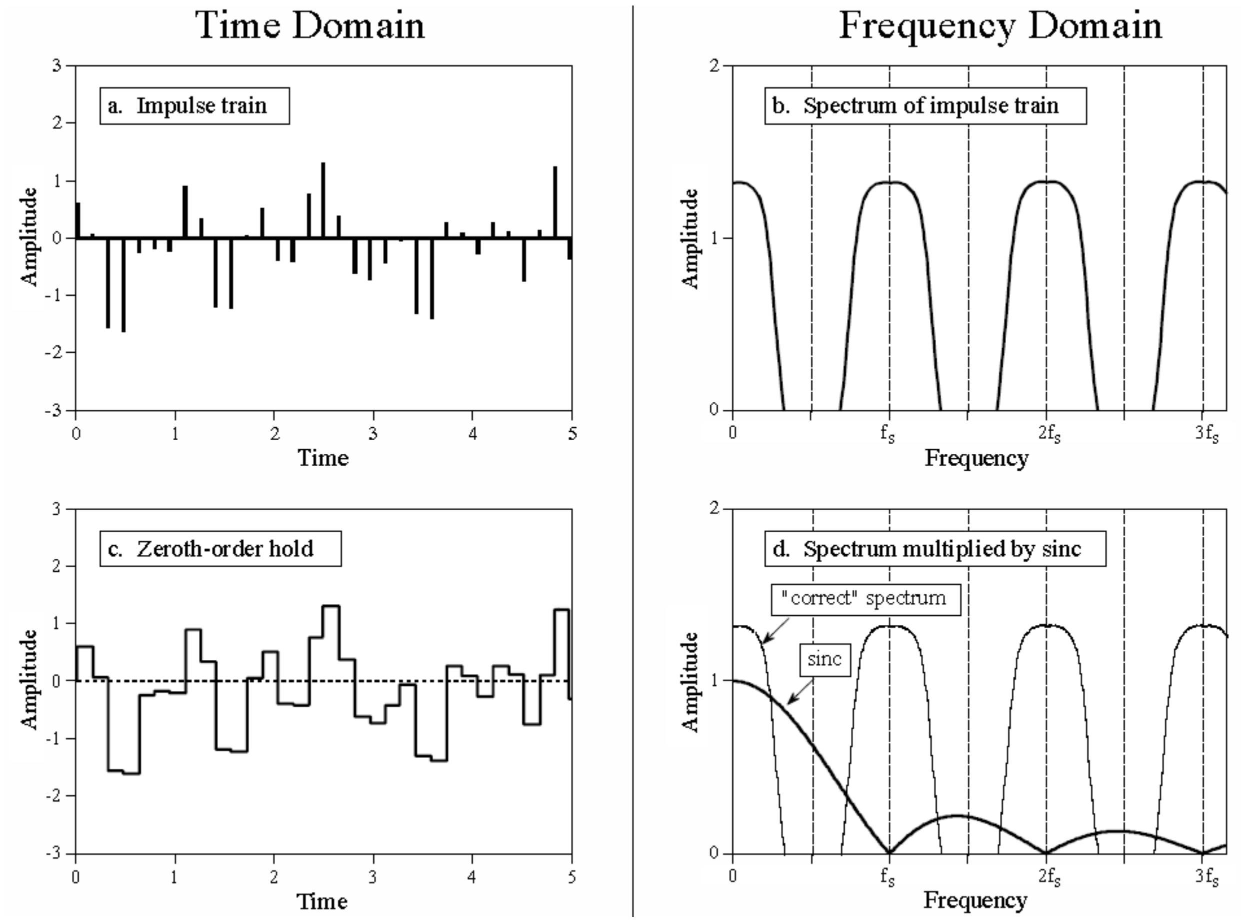
Note the aliasing (information lost) due to collision of frequency content

Note: Closely spaced samples in time give widely spaced spectrums in frequency (ts=1/fs)

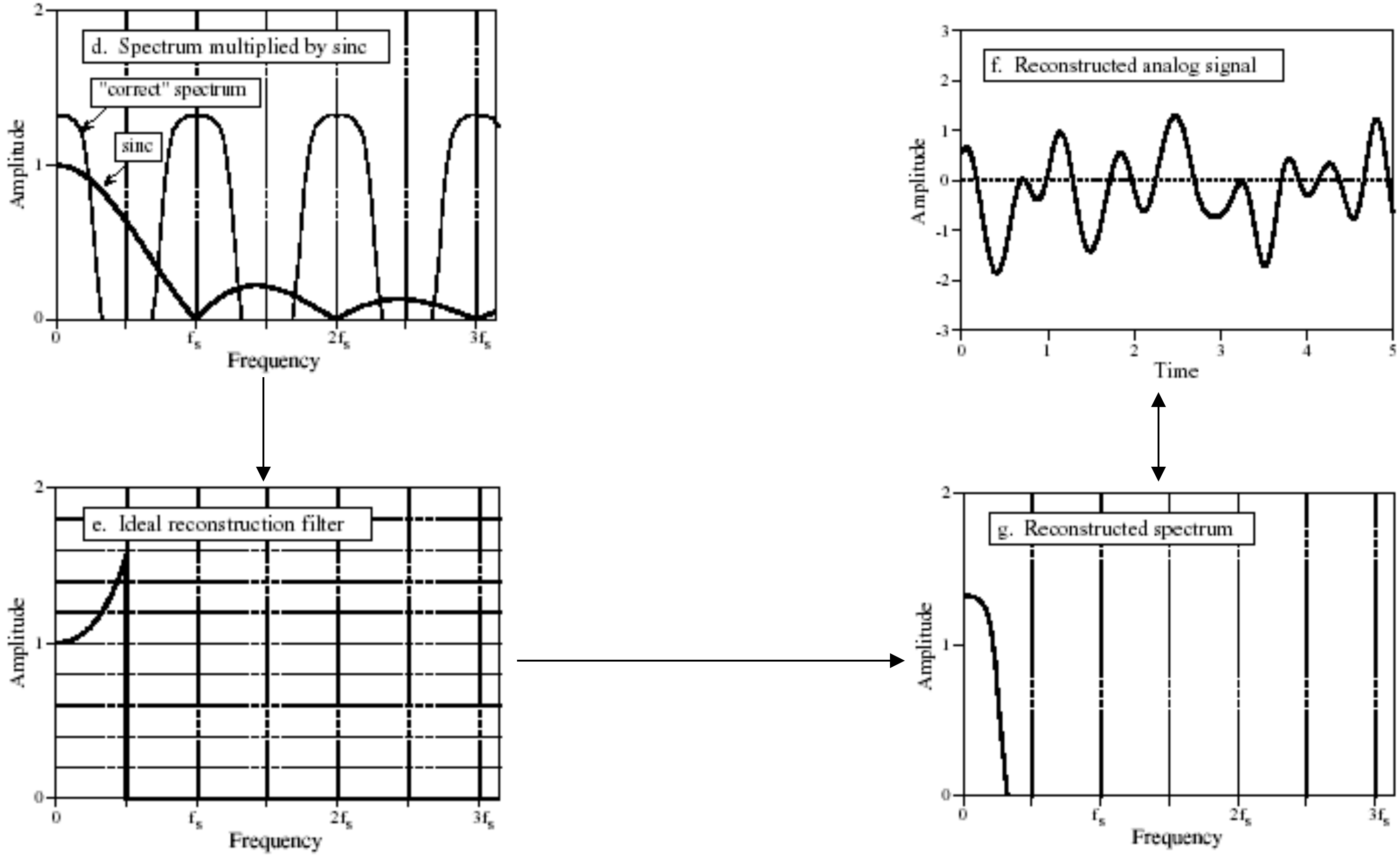
Digital to Analog Conversion (1/2)

Ideal digital output and spectrum

Realistic digital output using a zeroth order hold and spectrum



Digital to Analog Conversion (2/2)



Frequency Domain Effect of Zero Order Hold on Sampled Signal

- The Zero Order Hold (ZOH) has an effect on the frequency spectrum of the sampled signal.
- The ZOH effect can be understood by considering the ZOH as the convolution of the impulse train with a rectangular pulse, with the pulse having a width equal to the sampling period. This results in the frequency domain being *multiplied by the Fourier transform of the* rectangular pulse, i.e., the sinc function.

EQUATION 3-1
High frequency amplitude reduction due to the zeroth-order hold. This curve is plotted in Fig. 3-6d. The sampling frequency is represented by f_S. For $f = 0$, $H(f) = 1$.

$$H(f) = \left| \frac{\sin(\pi f / f_s)}{\pi f / f_s} \right|$$

Effect of ZOH on Reconstruction

- Because the Sinc function does not have unity gain from 0 to Fs/2, it creates distortion in the signal.
- To compensation for this, a reconstruction filter with a 1/sinc(x) characteristic can be used to cancel out the distortion.
- This reconstruction compensation can be done in analog, digitally or by using a multirate method to minimize its effect.

Example: Sketching the Spectrum of Signal

- Signal X(t)=2 sin(30 t)
- Example of spectrum of base band signal.
- Mirror symmetry of spectrum around zero frequency.

- Sampling Process.
- Ws = 200 Rad/sec
- Place copies of spectrum centered an N=1*Ws, N=2*Ws, etc. for Integer N.

In Class Team Problem

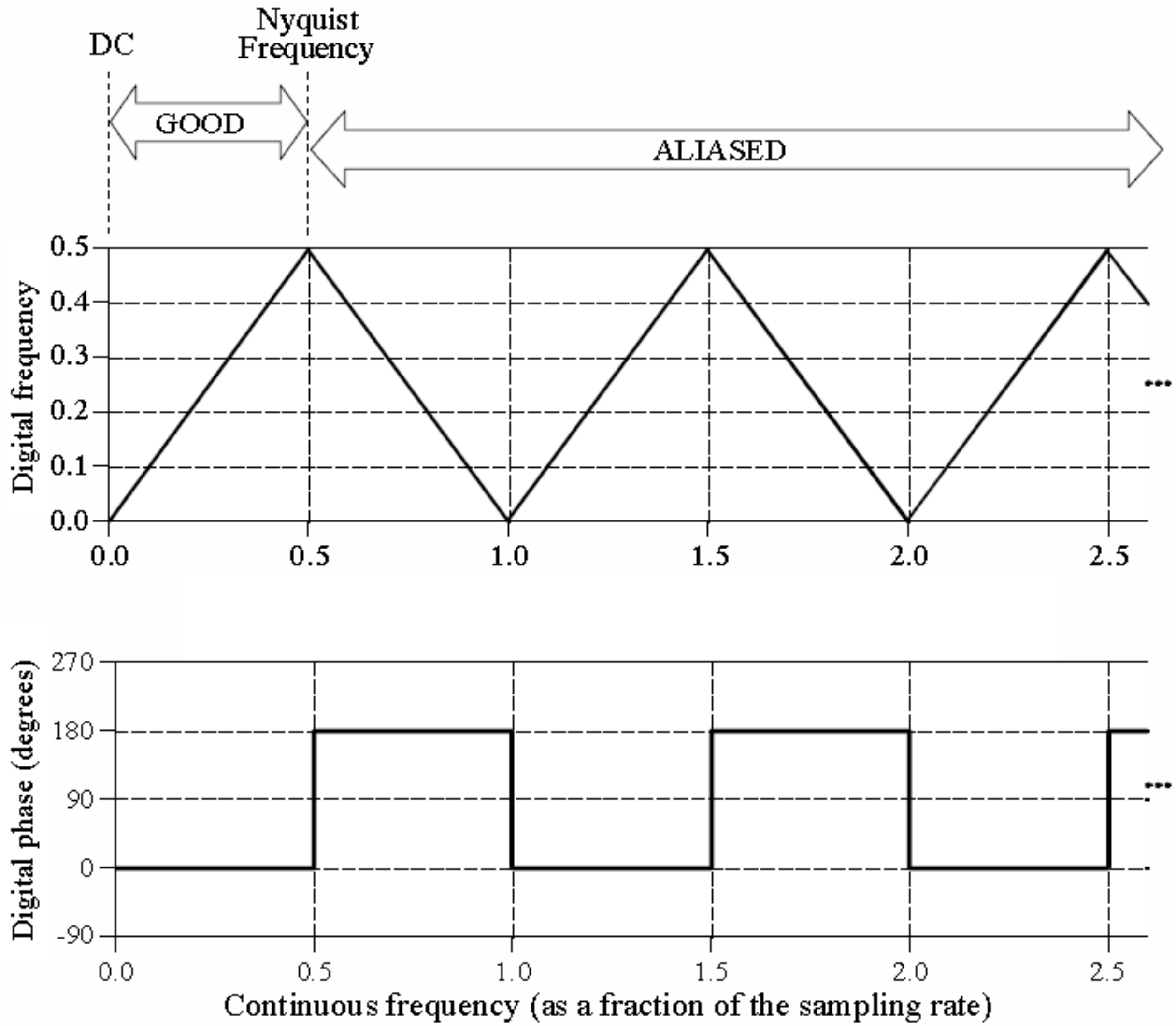
- $X(t)=2\sin(2t)+3\sin(3t)+\sin(4t)$ is sampled every $Ts=1.2$ seconds
- To do:
  - Draw the spectrum of the original signal before any sampling.
  - Find Ws, the sampling frequency in radian/s
  - Find the baseband region (radian/s)
  - Find the baseband sinusoids that result from the sampling process. (Think of copies of the spectrum repeated at integer multiples of Ws)

Team Problem - Solution

- Ws = 2*pi*fs=2*pi*(1/Ts) = 5.24 r/s
- Baseband = 0 to Ws/2 = 0 to 2.62 r/s
- 2sin(2t) => 2 sin(2t)
-
-

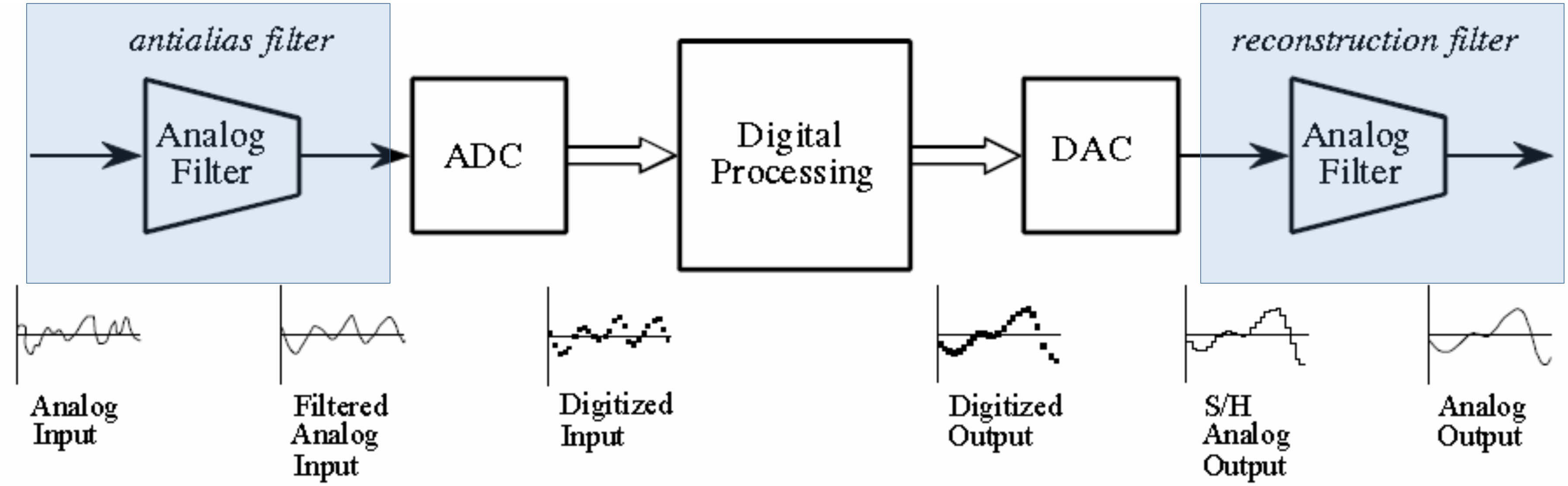
Aliasing – Another View

- The digital frequency domain can only describe signals as having frequencies from 0 to 0.5 times the sampling frequency. However, the continuous frequency domain can have signal content that is outside this range. Ultimately, every continuous domain frequency gets mapped down into the digital range of 0 to 0.5.



Conversion of analog frequency into digital frequency during sampling. Continuous signals with a frequency less than one-half of the sampling rate are directly converted into the corresponding digital frequency. Above one-half of the sampling rate, aliasing takes place, resulting in the frequency being misrepresented in the digital data. Aliasing always changes a higher frequency into a lower frequency between 0 and 0.5. In addition, aliasing may also change the phase of the signal by 180 degrees.

Overall A/D->DSP->D/A System

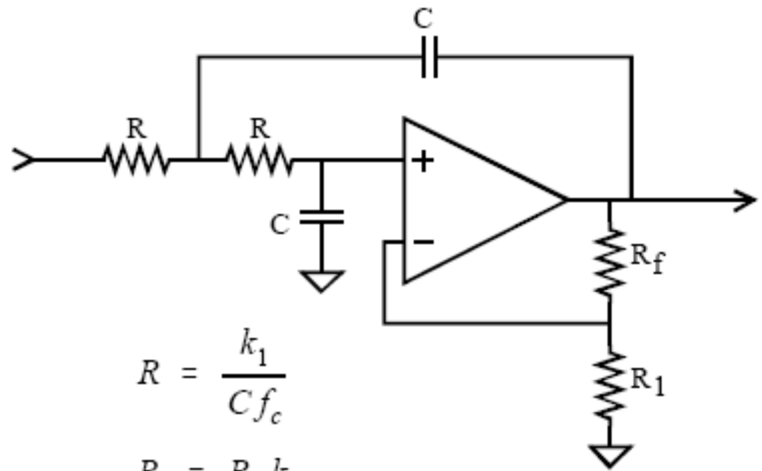


- Three basic types of filters:
  - Chebyshev
    - fastest roll-off in frequency, frequency domain
  - Butterworth
    - maximally flat, frequency domain
  - Bessel
    - Best step response, time domain

Modified Sallen-Key Circuit

2-Pole filter building block

FIGURE 3-8
The modified Sallen-Key circuit, a building block for active filter design. The circuit shown implements a 2 pole low-pass filter. Higher order filters (more poles) can be formed by cascading stages. Find k_1 and k_2 from Table 3-1, arbitrarily select R_1 and C (try 10K and 0.01μF), and then calculate R and R_f from the equations in the figure. The parameter, f_c, is the cutoff frequency of the filter, in hertz.



$$R = \frac{k_1}{C f_c}$$

$$R_f = R_1 k_2$$

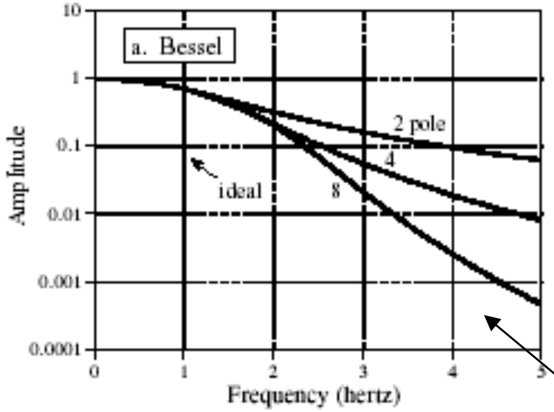
Can cascade sections to increase the filter order

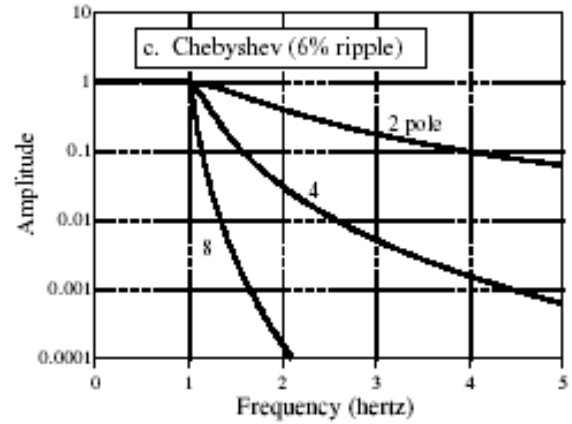
TABLE 3-1
Parameters for designing Bessel, Butterworth, and Chebyshev (6% ripple) filters.

# poles		Bessel k_1	Bessel k_2	Butterworth k_1	Butterworth k_2	Chebyshev k_1	Chebyshev k_2
2	stage 1	0.1251	0.268	0.1592	0.586	0.1293	0.842
4	stage 1	0.1111	0.084	0.1592	0.152	0.2666	0.582
	stage 2	0.0991	0.759	0.1592	1.235	0.1544	1.660
6	stage 1	0.0990	0.040	0.1592	0.068	0.4019	0.537
	stage 2	0.0941	0.364	0.1592	0.586	0.2072	1.448
	stage 3	0.0834	1.023	0.1592	1.483	0.1574	1.846
8	stage 1	0.0894	0.024	0.1592	0.038	0.5359	0.522
	stage 2	0.0867	0.213	0.1592	0.337	0.2657	1.379
	stage 3	0.0814	0.593	0.1592	0.889	0.1848	1.711
	stage 4	0.0726	1.184	0.1592	1.610	0.1582	1.913

Filter Frequency Response

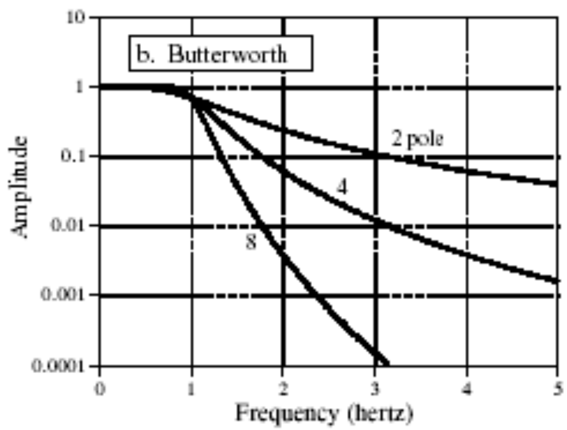
Log scale





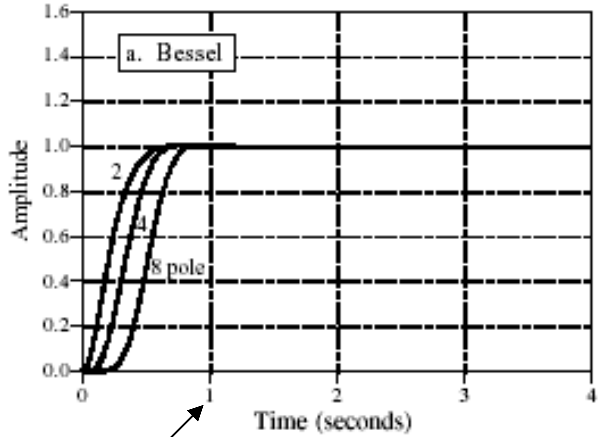
There must be a reason
For this one…

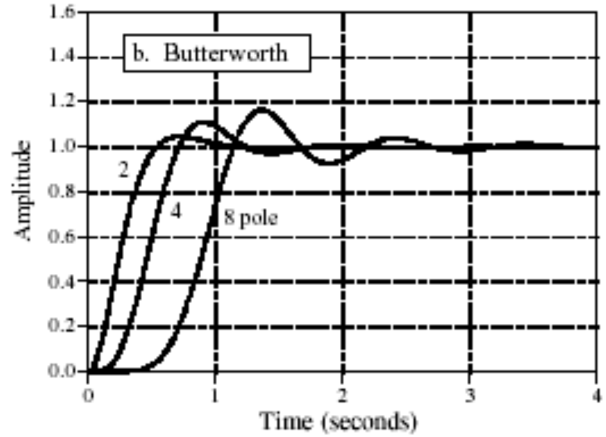
Best rolloff rate
but at the cost of
passband ripple



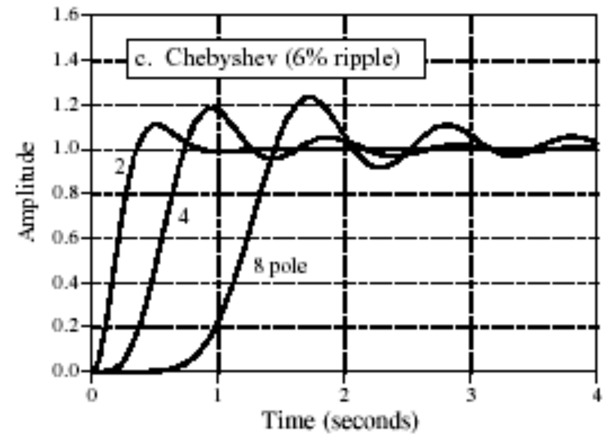
Maximally flat in
The passband but “slow”
rolloff in the stopband

Comparison of Filter Step Response





Excellent step response – No significant ringing or overshoot!



Pulse Response

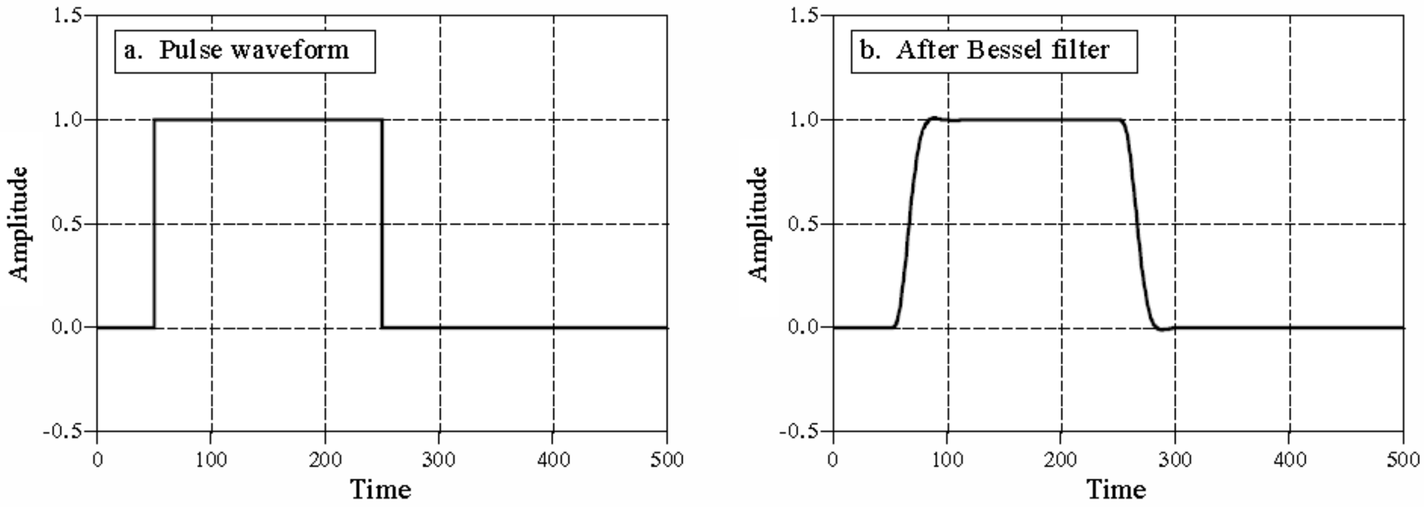
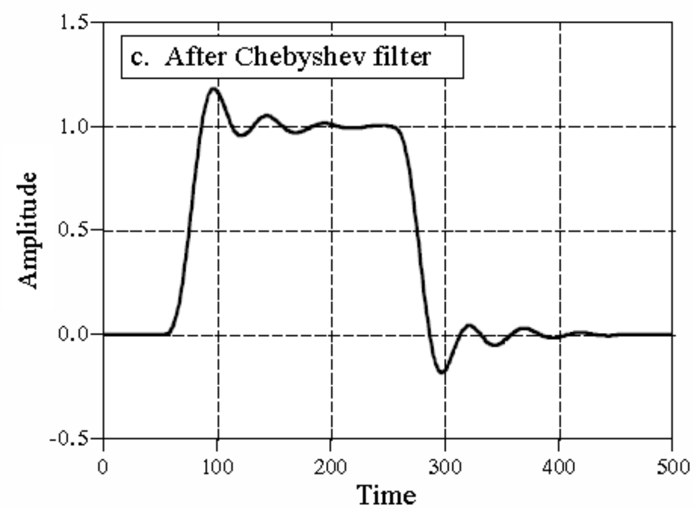


FIGURE 3-14
Pulse response of the Bessel and Chebyshev filters. A key property of the Bessel filter is that the rising and falling edges in the filter's output looking similar. In the jargon of the field, this is called *linear phase*. Figure (b) shows the result of passing the pulse waveform in (a) through a 4 pole Bessel filter. Both edges are smoothed in a similar manner. Figure (c) shows the result of passing (a) through a 4 pole Chebyshev filter. The left edge overshoots on the *top*, while the right edge overshoots on the *bottom*. Many applications cannot tolerate this distortion.



Multirate Methods

- Multirate methods use high sample rates to reduce the demand on the analog filters of the ADC/DAC system.
  - Analog signal is filtered by a simple RC circuit, then sampled at a very high rate with aliasing in part of the band.
  - A high performance digital filter is used to remove portion of the spectrum where aliasing could have occurred,
  - The data is then decimated (e.g. take every 1 out of 10 samples) to get a lower but un-aliased set of data. Then what ever processing is needed is applied.
  - On the DAC side, data is interpolated (e.g. add 9 zero values for every 1 data point) and then filtered with a simple RC circuit to get back to analog data.
- Multi-rate puts more of the work in the digital domain and less in the analog domain.

Example Multirate Device – ADC/DAC Codec Used in DSP Lab

TEXAS INSTRUMENTS

TLV320AIC23B

Stereo Audio CODEC, 8- to 96-kHz, With Integrated Headphone Amplifier

1 Introduction

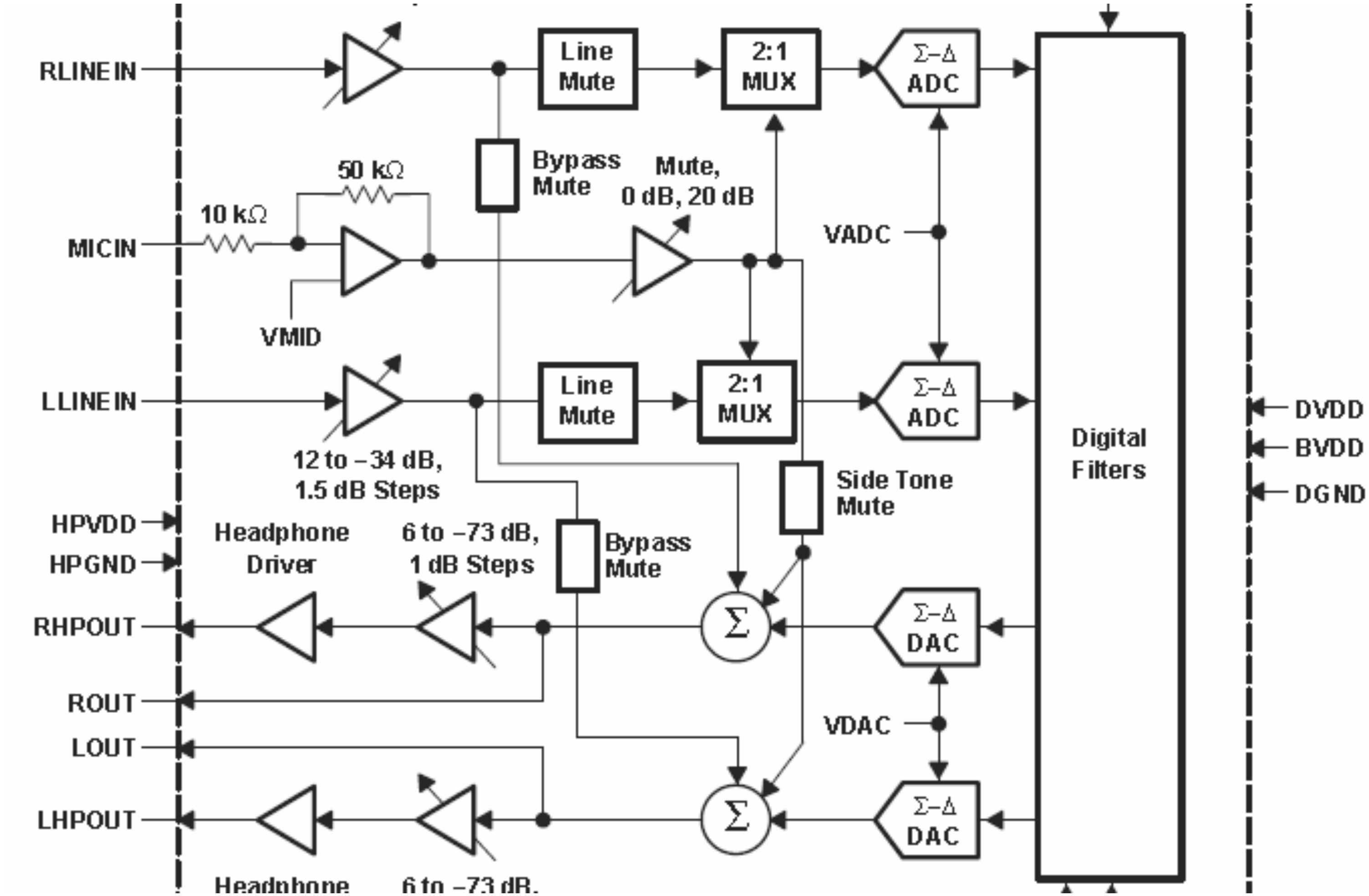
The TLV320AIC23B is a high-performance stereo audio codec with highly integrated analog functionality. The analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) within the TLV320AIC23B use multibit sigma-delta technology with integrated oversampling digital interpolation filters. Data-transfer word lengths of 16, 20, 24, and 32 bits, with sample rates from 8 kHz to 96 kHz, are supported. The ADC sigma-delta modulator features third-order multibit architecture with up to 90-dBA signal-to-noise ratio (SNR) at audio sampling rates up to 96 kHz, enabling high-fidelity audio recording in a compact, power-saving design. The DAC sigma-delta modulator features a second-order multibit architecture with up to 100-dBA SNR at audio sampling rates up to 96 kHz, enabling high-quality digital audio-playback capability, while consuming less than 23 mW during playback only. The

Codec Oversampling and Performance

- While the TLV320AIC23B supports the industry-standard oversampling rates of 256 fs and 384 fs, unique oversampling rates of 250 fs and 272 fs are provided, which optimize interface considerations in designs using TI C54x digital signal processors (DSPs) and universal serial bus (USB) data interfaces.

- High-Performance Stereo *Codec*
  - 90-dB SNR Multibit Sigma-Delta ADC (A-weighted at 48 kHz)
  - 100-dB SNR Multibit Sigma-Delta DAC (A-weighted at 48 kHz)

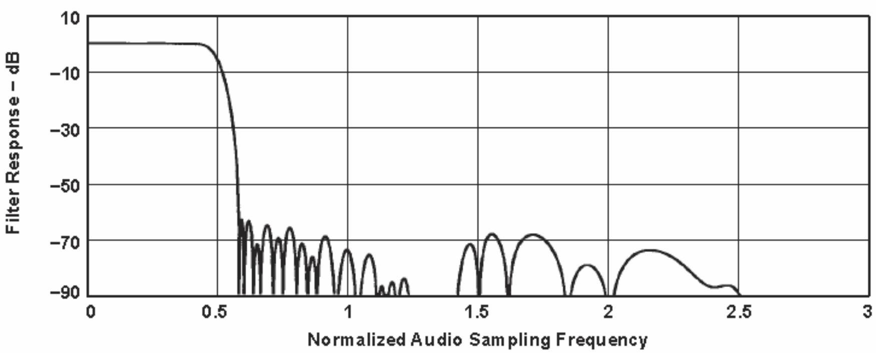
Internal Architecture of Codec

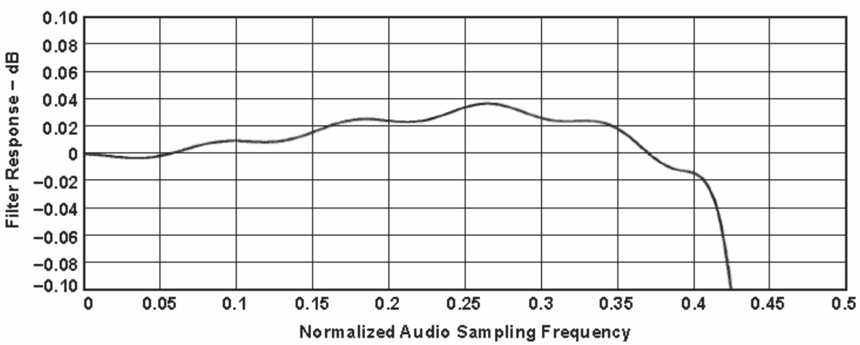


Digital Filter Performance

3.3.3 Digital Filter Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter Characteristics (TI DSP 250 f_S Mode Operation)					
Passband	±0.05 dB	0.416 f_S			Hz
Stopband	−6 dB		0.5 f_S		Hz
Passband ripple				±0.05	dB
Stopband attenuation	f > 0.584 f_S		−60		dB





Summary of Today's Lecture (1/2)

- The ADC process
  - Can be viewed as two steps: 1) sampling and holding followed by 2) quantization
- Quantization
  - Is modeled as adding uniform random noise with σ=~0.29 LSB. The quantization noise affects how many bits should be used in the ADC if oversampling is to be avoided.
  - Adding <u>dithering</u> noise can help to get enhanced resolution from averaging many samples. It is required when there is insufficient analog noise in the system compared to the quantization step size.

Summary of Today's Lecture (2/2)

- Sampling
  - Can lead to aliasing and loss of information if the sample rate and anti-aliasing filter are not properly matched.
  - All continuous frequencies are mapped into the digital frequencies range of 0 to 0.5 times the sample rate.
- Filtering for anti-aliasing and reconstruction
  - Each filter type (Cheb, Butter, Bessel) has specific advantages (e.g. frequency selectivity, uniform amplitude response, or time domain step response).
  - Choosing which one to use comes down to understanding how the information is represented in the signals you intend to process (e.g. time domain shape, frequency amplitude, frequency content).
  - Multi-rate methods use a high sample rate external to the DSP and low sample rate in the DSP