CAST CPET-563 Embedded Systems Design II **Dr. Kaputa**
Spring 2020
Lab 2

Student Name: _____ Section #:_____

Introduction:

You are to create a PWM module in VHDL that accepts a period and duty cycle and generates a PWM pulse train output. The module shall be fully verified via simulation in Modelsim. Verify the module for all corner cases. Assume the input clock frequency is 50 MHz.

Requirements for the PWM module:

- shall have an enable pulse.
- shall be able to control both the duty cycle and the period of the PWM pulse train.
- shall use basic entity inputs and not use 'generics' for the period and duty inputs.

Tech Memo:

Create a tech memo describing the hierarchy and organization of your code base. Include block diagrams, flow charts, screen shots, background information, and anything else that would be helpful for someone receiving your code base.

Due Date:

You will have roughly 7 days to work on each lab. Labs are due at midnight either on Mon or Wed one week after your scheduled lab time. You are expected to put in 2-4 hours of work outside of scheduled lab time as there are no other homework assignments, quizzes, or tests during the first 6 labs.

Lab Submission:

1. Submission Link
   https://my.pcloud.com/#page=puplink&code=seQ7Zrrf873e53sYzMK2XApcYf79qXvby
2. Submit a single zip file with all code, tech memo, and demonstration video showing basic functionality
3. Sample folder structure
   a. src
   b. doc
   c. vid

Grading:

Labs will be graded against the below rubric. Late labs will get a 0.

Grade	Description
0	Lab handed in late, or not handed in
1	Poor quality or no demonstration video
2	Average quality
3	High quality